

**STUDY OF SYNCHRO AND DEVELOPMENT OF
SYNCHRO-TO-DIGITAL CONVERTER FOR
INSTRUMENTATION & CONTROL APPLICATIONS**

By

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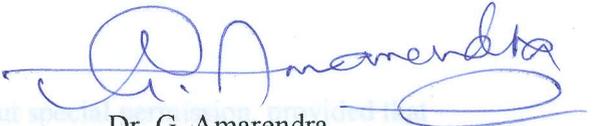
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List of Publications in the thesis **DECLARATION**

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Abstract

1. Context

The rotary angular position and speed of a motor shaft are important to sense and control various motor drive systems. Positional sensors and their associated converters are used to extract these parameters. The standard control systems mainly use optical and magnetic encoders for position and speed measurements. The optical encoders are expensive compared to the magnetic based sensors such as synchros and resolvers. In case of synchros, the electrical outputs are transmitted over distances upto 10 meters over three wires. The conversion of mechanical angular information to the electrical signals will be ratio-metric in principle; hence a high degree of noise immunity is achieved. Traditionally, synchros have been used in harsh environments involving noise, high temperature and vibration. Synchro has one primary winding and three secondary windings with each secondary winding mechanically oriented 120° apart.

At present Synchro-to-Digital Converter (SDC) is increasingly used for precise measurement of rotary position, such as control rod, guide tube, gripper assembly etc. in fast reactor programme. A detailed literature survey indicates that the SDC/RDC is more expensive than positional sensors. Therefore, an investigation has been carried out for SDC to achieve a cost-effective converter with acceptable performance. In addition, all the earlier converters do not have the feature of digital readout for rotor shaft position and speed as a single solution. Hence, a method is presented here which computes both position and speed of the shaft in digital form.

2. Methods

A model for SDC is developed in MATLAB/Simulink environment. It consists of scott-T circuit, comparators, monoshot circuits, Sample & Hold (S&H) circuits, quadrant detector and an absolute angle estimator. The scott-T circuit converts three signals of synchro into two

signals format and denoted as V_S and V_C . The position information of synchro shaft present in peak amplitudes of scott-T outputs. Here, the monoshot and S&H circuit act as demodulator to extract the angle information of the shaft. The basic idea of this method is to extract the instantaneous peak amplitudes of scott-T outputs using demodulators and division of these values followed by inverse tangent operation. Then the absolute shaft angle is calculated using the quadrant detector bits. The quadrant detector bits give the information of quadrant in which shaft angle falls. In the process of demodulation, the monoshot employs a resistor and capacitor as external components to generate sampling signal for S&H circuit. Due to temperature variation and drift in resistance, it is difficult to generate sampling pulses exactly at peak amplitudes of V_S and V_C . So a digital approach is adopted to extract the peak amplitudes of synchro.

In this method the synchro signals are demodulated using digital peak detectors to extract the rotor angle information. There are two digital peak detectors used to get peak amplitudes of scott-T signals. The digital peak detector consists of a comparator, 10-bit counter and 10-bit Digital-to-Analog Converter (DAC). Here, the comparator enables the counter, which starts counting until peak value of the input signal is reached. Now the counter provides digital output corresponding to the peak amplitude information and fed to latching circuit. This method requires stringent and high speed DACs to implement digital peak detectors. Further, the DAC is operated with a fixed reference voltage; it cannot give good resolution for output shaft angle because the signals V_S and V_C (which are the inputs to the digital peak detectors) are continuously time varying signals from small to high voltage swing. Therefore, a new approach is presented to compute the synchro shaft angle using the concept of Pulse Width Modulation (PWM).

The basic idea of the scheme is the linear evaluation of peak amplitudes of synchro signals using Time Duration Windows (TDW) and division of TDWs followed by the inverse

tangent operation to get rotor shaft angle. The linear evaluation of TDW, quadrant detection and shaft angle in digital form demonstrates the effectiveness of the proposed converter.

Finally, an investigation is also taken up for diagnostic features of the SDC. Diagnostic features such as Loss Of Signal (LOS) detection and stator terminal reversal connection detection between synchro and SDC are implemented. The LOS detection and reversal connection detection are useful during commissioning stage of systems where the synchro is deployed as positional sensor.

3. Results

The effects of the non-ideal characteristics of synchro such as amplitude imbalance, imperfect quadrature, reference signal phase shift and excitation signal distortion are studied using the Simulink model of SDC. These cause the synchro output deviation from the ideal behavior. From analysis, it is noted that as long as the imbalance and imperfect values are of equal amounts, the angular error is zero. It is also observed that the algorithm offers the robustness to reference signal phase shift and excitation signal distortion.

From experimental results, the implemented converter exhibits good linearity over 0° - 360° range and a maximum error of 0.16° is observed between actual and measured angles. The present converter experimented with a 50 Hz synchro. This converter finds an application in position measurement, where motor driven mechanisms rotate at low speeds. The tracking rate of the converter can be improved by using high frequency synchros. The EDA tools used in the process of development are Max+plus II (to fuse digital logics into CPLD) and Custom Computer Services (CCS) C compiler (for PIC microcontroller).

4. Contributions

The thesis makes the following research contributions:

- The present work highlights the functional simulation of synchro and SDC. It is useful in the quantification of non-ideal characteristics of synchro.

- A novel approach based on PWM is presented to compute angular position and speed of synchro shaft. It replaces the usage of ADCs unlike previous approaches.
- The present method utilizes simple components and the computation of speed of rotor shaft doesn't require any separate circuit since the sine quadrant bit of quadrant detector itself provides speed information. Hence, it is cost-effective.
- The present converter is incorporated with LOS and stator terminal reversal connection detectors.

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List of acronyms

ADC	Analog-to-Digital Converter
API	Angle Position Indicator
ATO	Angle Tracking Observer
BAM	Binary Angular Measurement
BOM	Bill Of Materials
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CSR	Control and Safety Rod
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DSR	Diverse Safety Rod
EMF	Electro Motive Force
EPROM	Erasable Programmable Read Only Memory
HCR	Handling Control Room
I ² C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LOS	Loss Of Signal
LRP	Large Rotatable Plug
LSB	Least Significant Bit
LUT	Look Up Table
MDAC	Multiplying Digital-to-Analog Converter
NPP	Nuclear Power Plant
PFBR	Prototype Fast Breeder Reactor
PI	Proportional Integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
RDC	Resolver-to-Digital Converter
ROM	Read Only Memory

RPM	Revolutions Per Minute
RTC	Real Time Computer
S&H	Sample & Hold
SDC	Synchro-to-Digital Converter
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SRP	Small Rotatable Plug
SS	Sampling Signal
TA	Transfer Arm
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TDW	Time Duration Window
TMS	Test Mode Select
VCO	Voltage Control Oscillator

CHAPTER 1

INTRODUCTION

CONTENTS:

1.1 Foreword

1.2 Fuel handling mechanisms of nuclear reactor

1.3 Motivation

1.4 Organization of thesis

References

1.1 Foreword

Motor shaft angle and speed are the most important parameters in motion control systems. These parameters are important to sense and control the systems associated with satellite antennas, radar antennas, aircraft, instrumentation and control systems of nuclear reactor etc. Thus, shaft angle positional sensors are the key elements in modern control systems. The position information and speed can be extracted from the synchro/resolver-to-digital converters through positional sensors.

Various shaft angle position sensors are available in market. The standard control systems mainly use optical and magnetic encoders for position and speed measurements [1]. Optical encoders provide digital outputs corresponding to the position of its shaft. This digital output is compatible with various digital circuits. But the associated electronics such as light sources, light detectors etc inside the optical encoders are sensitive to temperatures, vulnerable to radiation and aging.

Traditionally, synchros have been used in harsh environments involving noise, high temperature and vibration. The optical encoders are expensive compared to the magnetic based sensors such as synchros and resolvers. In case of synchros, the electrical outputs are transmitted over distance upto 10 meters over three wires [2]. The conversion of mechanical angular information to the electrical signals will be ratio-metric in principle; hence a high degree of noise immunity is achieved. In addition, synchro has inherent properties like mechanical ruggedness, robustness to vibration and immune to temperature variations. It is mounted on the shaft of a motor and converts the angular position of the rotating shaft to electrical signals.

Synchros have been used in military for fire control systems to transmit the angular information from guns to control computer and to transmit the desired gun position back to the gun location. The synchros are mainly used in aircraft applications due to their small size

and reliable operation for a long time [3]. The mechatronic flight servosystem integrates electromechanical motion devices (stepper motor and synchro/resolver), the power amplifier (PWM driver), transducer and controllers. The synchros are used to know antenna elevation angles in satellite applications. Industrial applications such as automated steel carriage system uses synchro for position detection of molten steel container during transporting it from one location to other location. A brief background about fuel handling mechanisms of nuclear reactor is also given to illustrate the scope for the use of synchro in reactor applications.

1.2 Fuel handling mechanisms of nuclear reactor

The synchro is used as positioning sensor in many nuclear reactors such as Vogtle Electric Generating Plant, US and Rapsode reactor, France etc. The instrumentation and control systems of nuclear reactor, which employ synchro as positional sensor, are discussed in this thesis. These systems are useful to monitor various parameters in order to guide the operator, control certain parameters within the limits and initiate automatic safety actions. Two systems, Small Rotatable Plug (SRP) and Large Rotatable Plug (LRP) control systems and Transfer Arm (TA) of nuclear reactor are taken up as case studies in the present thesis. The in-vessel component handling is done with the help of two rotatable plugs and a transfer arm. A brief description of each system is given below.

1.2.1 Small Rotatable Plug and Large Rotatable Plug (SRP and LRP) system

The arrangement of two rotatable plugs and TA (shown in figure 1.1) is designed such that the rotation of SRP along with that of TA will enable in positioning the TA gripper at any radius whereas, the rotation of LRP will enable in positioning of the gripper at any desired angular location [4]. The accurate alignment of TA over any subassembly is required during fuel handling. This can be achieved only by accurate angular positioning of the plugs and hence, the drives should ensure good positioning accuracy of the plugs. By rotating TA top structure and rotatable plugs, the TA gripper is aligned over the required grid location for the

fuel handling operations. The Real Time Computer (RTC) system shall receive input commands from HCR, which continuously monitors the control signals from the rotatable plugs and from the external RTC systems and gives the appropriate output to the drive motor.

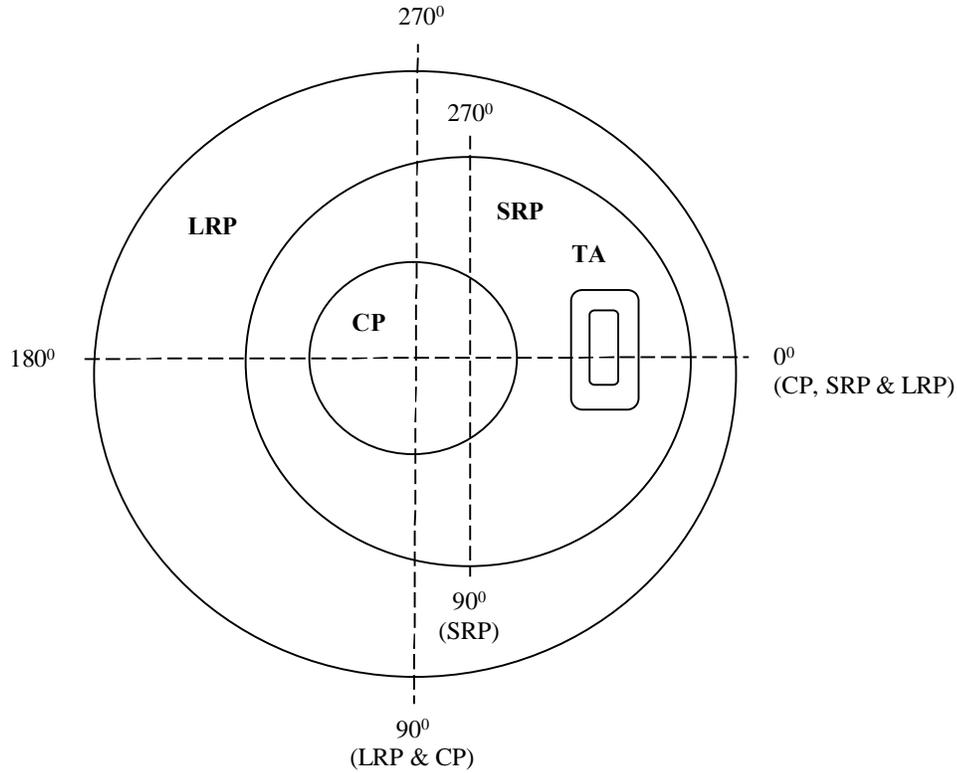


Figure 1.1: The arrangement of rotatable plugs and transfer arm. The rotatable plugs (SRP-LRP) are eccentric while the Control Plug (CP) and Transfer Arm (TA) supported on Small Rotatable Plug (SRP).

An indicating mechanism is required to provide the angular position of the plugs and help the operator to drive them to their correct positions. To achieve this, two drive mechanisms, one each for SRP and LRP are provided. The SRP drive along with the speed reducing gear unit is located on LRP and LRP drive along with gear unit is located on roof slab. It is proposed to have a system with position indicating sensors, which will be used to monitor, control and indicate accurately the angular position of the plugs. Remote positioning of plugs is possible using synchros and optical encoders. Each rotatable plug is provided with two speeds of rotation (fast speed and slow speed) to reduce fuel handling time and for better positioning.

Figure 1.2 shows the arrangement of a large diameter gear fixed to the plug, which meshes with a pinion. The pinion is connected to the motor through a gear box. The optical encoders and synchros are coupled to motor-gear drive unit to monitor the continuous positioning of the rotating plugs. The optical encoder is used as the primary sensor while synchro is used as the redundant continuous position sensor [5]. The SDC has capability for converting the synchro output to digital form.

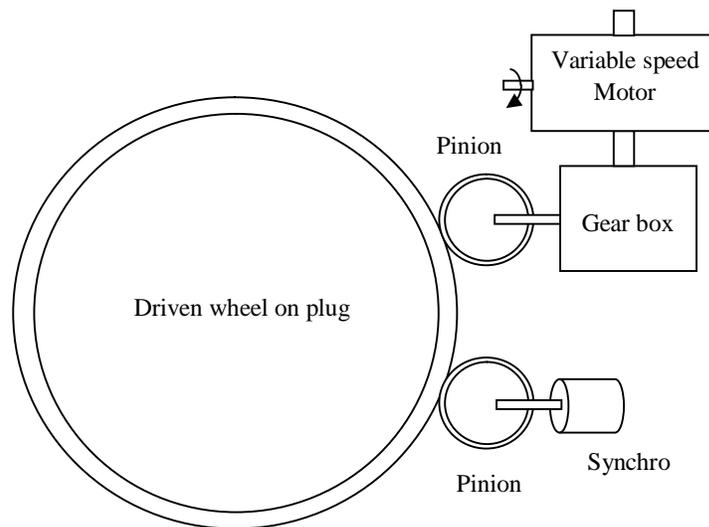


Figure 1.2: Schematic arrangement of synchro for position monitoring and control of rotatable plug. The pinion arrangement provided separately for motor and synchro to avoid backlash.

1.2.2 Transfer arm system

TA consists of a hollow cylindrical body and a top structure. The top structure supports hoist mechanism for gripper and the guide tube [6].

TA is provided with the diverse continuous position monitoring systems for indicating the position of gripper hoist, guide tube and top structure rotation. Synchros are provided as the primary sensor for all the three drives and wire type potentiometers are provided as secondary sensor for gripper hoist, guide tube [7]. Optical encoder is provided as the secondary sensor for top structure rotation angle measurement. In each control action, the primary sensor

outputs are converted into digital form to represent angular position of shaft and the same is validated with the outputs of secondary sensor's output.

1.3 Motivation

The rotary angular position and speed information of rotor shaft of a motor are important in many position and speed control systems. These two parameters can be extracted from SDC through synchro, a positional sensor. SDC is increasingly being used for precise measurement of rotary position such as that of control rod, guide tube, gripper assembly of a nuclear reactor. A detailed literature survey reveals that the cost of SDC/RDC is higher than that of positional sensors. Various converter schemes have been reported to improve the simplicity and the accuracy of the measured shaft angle. In addition, converters reported in literature do possess digital readout feature for rotor shaft position and speed in a single solution. In this research work, an attempt has been made to study the existing methods and develop a new method to compute both position and speed of the shaft in digital form. This methodology offers an advantage that it does not require any extra hardware to compute the speed of the shaft. Further, an investigation is also taken up for incorporating the diagnostic features of SDC to detect cable disconnection and reverse connection between synchro and SDC. A mathematical study is carried out to estimate angular error caused by non-ideal behavior of synchro.

1.4 Organization of thesis

The thesis is organized as follows

Chapter 1 Presents brief scope of synchro & SDC in nuclear reactor systems, and motivation of the present thesis.

Chapter 2 Introduces synchro, SDC and review on implementation of schemes for SDC.

Chapter 3 Presents mathematical study of synchro and modeling of SDC using MATLAB/Simulink.

Chapter 4 Describes the digital peak detection based design of SDC.

Chapter 5 Gives hardware implementation of SDC.

Chapter 6 Describes the diagnostic features: loss of signal detection and stator terminal reversal connection detection between the synchro and SDC.

Chapter 7 Summarizes the thesis and highlights future directions.

References

- [1] Ralph M. Kennel, "Encoders for simultaneous sensing of position and speed in electrical drives with digital control," IEEE Transactions on Industry Applications, vol. 43, no. 6, pp.1572- 1577, 2007.
- [2] H. Loge, L. Angerpointner, "The best way how to use resolvers," International Electric Drives Production Conference, Nuremberg, Germany, pp. 208-213, September 2011.
- [3] Application note for Aircraft/Aerospace, www.spaceagecontrol.com
- [4] IGCAR Internal Report, "Control note on rotatable plugs," PFBR/63130/CN/1005/Rev 0, Kalpakkam, India, 2007.
- [5] IGCAR Internal Report, "System Requirements Specification for Rotatable Plugs Control System," PFBR/63130/SP/1007/Rev B, Kalpakkam, India, 2010.
- [6] IGCAR Internal Report, "Control & Operation note on transfer arm," PFBR/63522/CN/1006/Rev 1, Kalpakkam, India, 2007.
- [7] IGCAR Internal Report, "System Requirements Specification for Transfer Arm Control System," PFBR/63522/SP/1005/Rev C, Kalpakkam, India, 2009.

CHAPTER 2

SYNCHRO & SYNCHRO-TO-DIGITAL CONVERTER

CONTENTS:

2.1 Synchro

2.2 Synchro parameters

2.3 Handling of synchros

2.4 Synchro-to-Digital Converter (SDC)

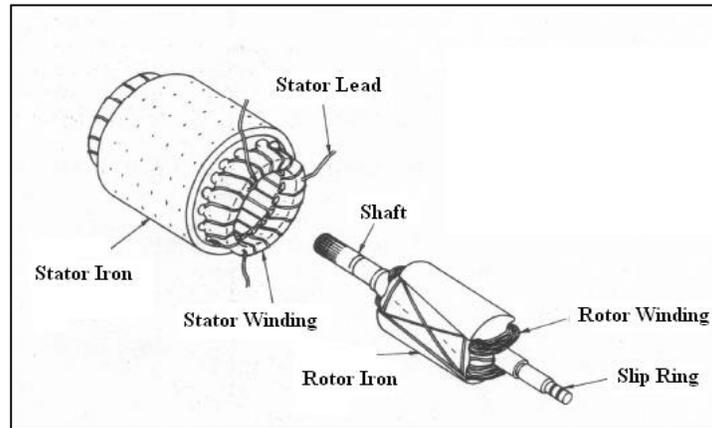
2.5 Literature review of synchro/resolver-to-digital conversion methods

References

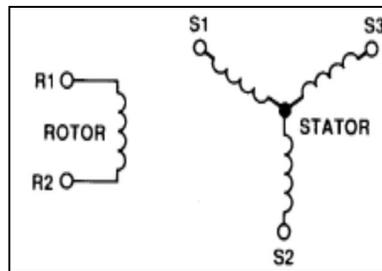
This chapter introduces synchro, Synchro-to-Digital Converter and presents literature review on synchro/resolver-to-digital converters.

2.1 Synchro

Synchro is a sensor, which converts the angular position of a rotary shaft to electrical signals [1]. It has one primary winding and three secondary windings with each secondary winding mechanically oriented 120° apart. Synchro is excited by an AC voltage at rotor and it generates three phase voltages at the stator based on the principle of electromagnetic induction. The internal structure and schematic symbol of synchro is shown in figure 2.1.



(a) Internal structure



(b) Schematic symbol: R1, R2 corresponds to the rotor terminals and S1, S2 and S3 corresponds to the stator terminals.

Figure 2.1: Synchro positional sensor (Courtesy: Memory Devices Ltd, United Kingdom)

The winding of rotor is supplied with a sinusoidal carrier signal, V_{Ref}

$$V_{Ref}(t) = V_{R1-R2}(t) = V \sin\omega t \tag{2.1}$$

where V is the peak amplitude and ω is the frequency of the excitation signal to the rotor.

Then the magnetically induced signals on three stator windings of the synchro are given as

$$V_{S3 - S1}(t, \theta) = V \sin \omega t \sin(\theta) \quad (2.2)$$

$$V_{S2 - S3}(t, \theta) = V \sin \omega t \sin(\theta + 120^\circ) \quad (2.3)$$

$$V_{S1 - S2}(t, \theta) = V \sin \omega t \sin(\theta + 240^\circ) \quad (2.4)$$

Where, θ is the angular position of the shaft of the synchro.

2.1.2 Principle of synchro

Ideal transformer

The schematic structure of ideal transformer is shown in figure 2.2. Transformer is an electrical device which transforms electrical energy from one circuit to another through mutual induction between two windings. It works on the principle of Faraday's law of electromagnetic induction. According to Faraday's law the rate of change of flux linkage with respect to time is directly proportional to the induced Electro Motive Force (EMF) in a conductor.

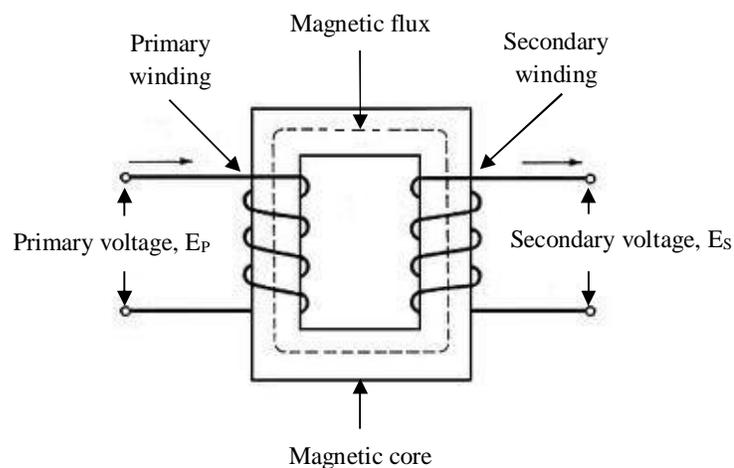
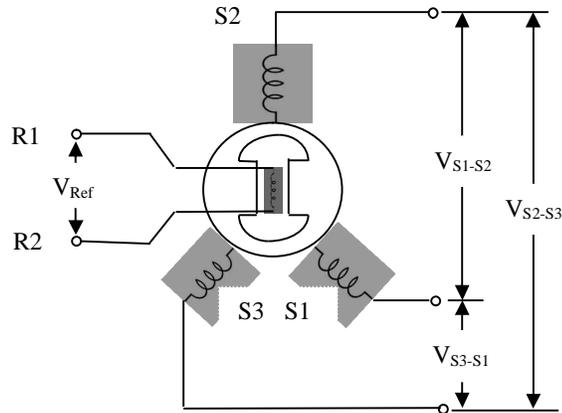


Figure 2.2: Schematic of transformer

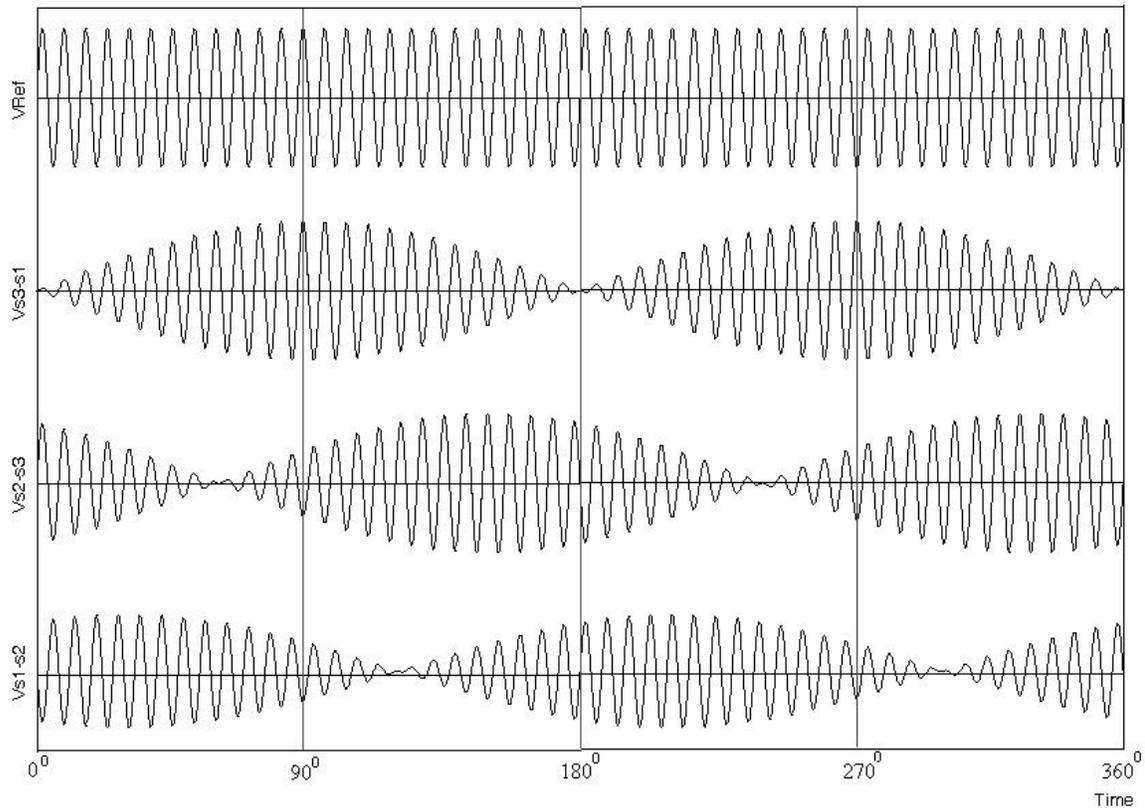
The induced secondary voltage of transformer is given by $E_S = \frac{N_S}{N_P} E_P$. Here, N_P and N_S are the number of primary and secondary turns of the transformer; and E_P is the primary voltage of the transformer.

Synchro

Synchro consists of rotor and stator. The rotor consists of one single winding, while the stator consists of three windings mechanically placed at 120° apart. The principle of operation of a synchro is based on a variable transformer i.e. the voltage induced in each stator winding varies as per the rotation of the rotor. The rotor winding receives the excitation voltage from external voltage source and the stator windings receive their voltage from rotor by electromagnetic coupling. The excitation signal is modulated by the angular rotation of synchro shaft and produces three modulated signals. The schematic structure and input-output signals of synchro are shown in figure 2.3.



(a) Schematic structure of synchro



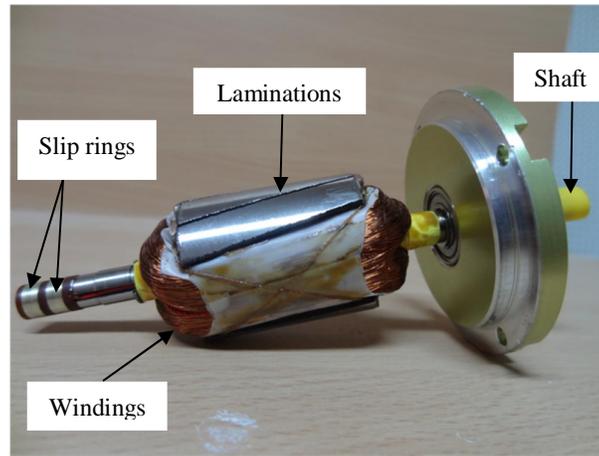
(b) Synchro excitation is V_{Ref} and output signals are V_{S3-S1} , V_{S2-S3} , V_{S1-S2}

Figure 2.3: Principle of operation of synchro

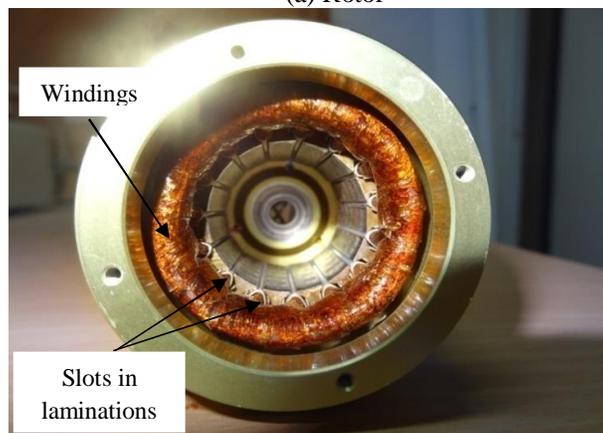
2.1.3 Construction of synchro

The constructional view of rotor and stator of synchro is shown in figure 2.4. The rotor has a single coil wound on a core. The excitation voltage is applied to the two slip rings through brushes. The two slip rings are mounted on one end of the shaft and insulated from the shaft. An insulated terminal board, houses the brushes, which ride on slip rings.

The stator is a cylindrical structure, made of laminated silicon steel and slotted on the inner periphery to accommodate a three phase winding. The stator winding is concentric type with the axis of the three coils 120° apart.



(a) Rotor



(b) Stator

Figure 2.4: Constructional view of synchro, consisting of rotor, stator and the important components are marked in the figure.

2.1.4 Types of synchro

Synchros are basically divided into two categories based on the loads to be driven by them.

2.1.4.1 Torque synchros

These synchros are concerned with the torque required to move light loads such as dials, pointers or similar indicators. There are four types of torque synchros and the electrical equivalent circuits are shown in figure 2.5.

- Torque transmitter (TX)
- Torque receiver (TR)
- Torque differential transmitter (TDX)

➤ Torque differential receiver (TDR)

The electrical representation of torque transmitter (TX) is shown in figure 2.5 (a). It has one rotor winding and three stator windings. When an ac excitation voltage is applied to the rotor of a torque transmitter, the resultant current produces an ac magnetic field. The magnetic flux lines induce voltage into the stator windings. The effective voltage induced into a stator winding depends on the angular position of that coil axis with respect to the rotor axis.

The electrical representation of torque receiver (TR) is shown in figure 2.5 (b). It has one rotor winding and three stator windings. It is applied with an electrical voltage to its stator winding and a mechanical output generated from the rotor. The torque receiver converts the electrical data supplied to its stator from torque transmitter, to a mechanical angular position. Hence the rotor of torque receiver moves accordingly. A typical synchro system consists of a torque transmitter connected to a torque receiver (TX-TR).

The electrical representation of torque differential transmitter (TDX) is shown in figure 2.5 (c). It has three rotor windings and three stator windings. It takes one electrical input and one mechanical input and produces one electrical output.

The electrical representation of torque differential receiver (TDR) is shown in figure 2.5 (d). It has three rotor windings and three stator windings. It takes two electrical inputs and produces one mechanical output. The differential synchro system consists either of a torque transmitter, a torque differential transmitter and a torque receiver (TX-TDX-TR); or two torque transmitters and a torque differential receiver (TX-TX-TDR).

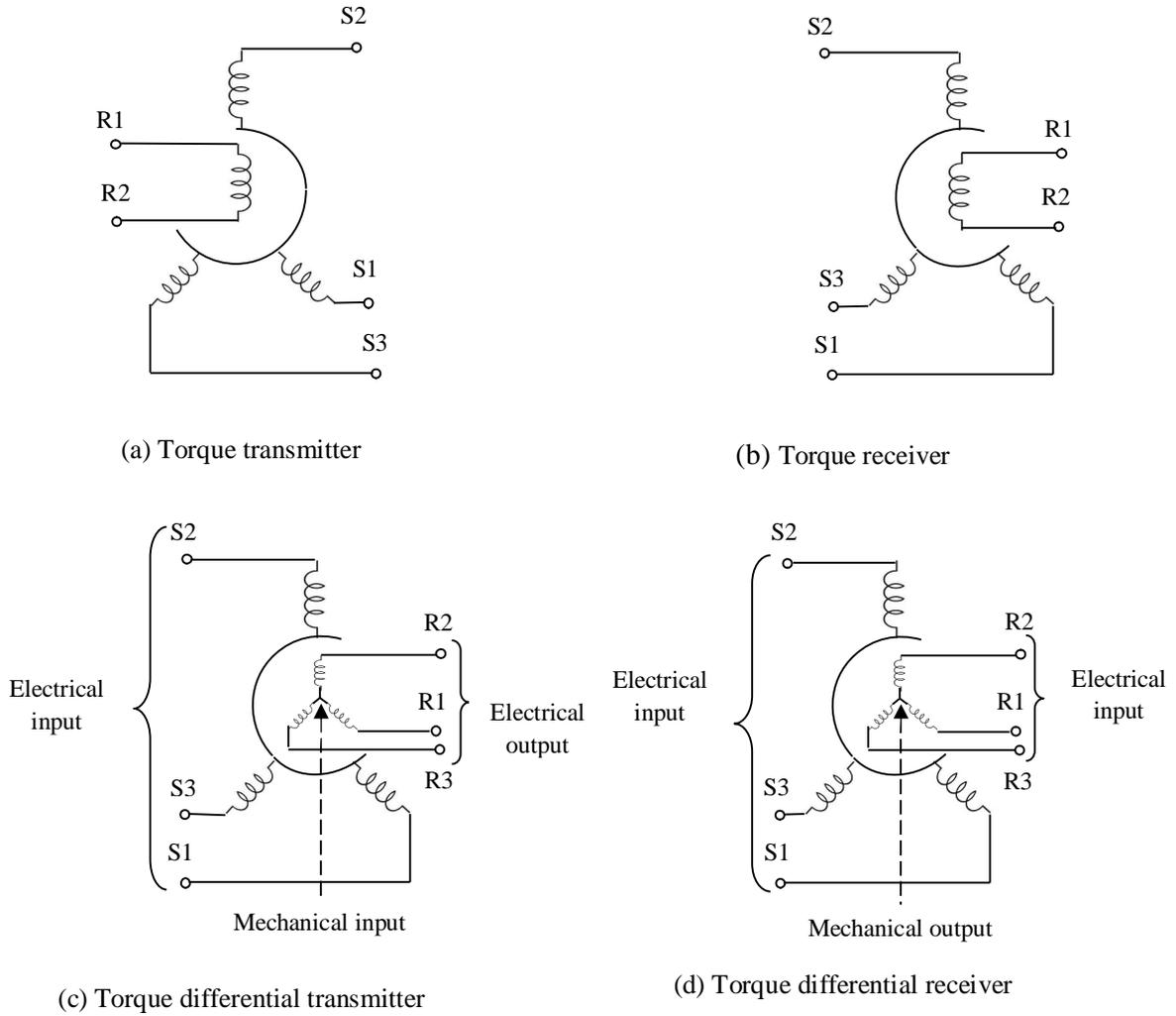


Figure 2.5: Electrical equivalent circuits of synchro

2.1.4.2 Control synchros

These are used in systems that are designed to move heavy loads such as gun directors, radar antennas and missile launchers. There are three types of control synchros.

- Control transmitter (CX)
- Control transformer (CT)
- Control differential transmitter (CDX)

The control transmitter (CX) has one rotor winding and three stator windings. The control differential transmitter (CDX) has three rotor windings and three stator windings. The CX

and CDX are similar to the TX and TDX except for their higher impedance. The higher impedance windings give a necessary voltage to the control system which drives a large load. The control transformer (CT) has one rotor winding and three stator windings. The CT provides a difference signal between the electrical signal applied to its stator and the mechanical signal applied to its rotor. The output of CT governs a power amplifying device for moving heavy load.

The rotor of CT is not connected to an ac supply, thus induces no voltage in stator windings. So the stator currents purely dependent on voltages applied to the high-impedance stator windings. There is no appreciable current flowing through rotor because its output voltage is always applied to a high-impedance load. Hence, the CT rotor does not try to follow the magnetic field of its stator and must be turned by external force. Since the electrical signals are applied to the stator, there is voltage induced into the rotor windings and the output is taken from the rotor leads. The amplitude and phase of the output voltage depend on the angular position of the rotor with respect to the magnetic field of the stator.

2.2 Synchro parameters

The important parameters of the synchro are reference voltage, reference frequency, accuracy, transformation ratio, impedances, input current, input power and part number.

2.2.1 Reference voltage and reference frequency

The synchros, which are available in the market operate at frequencies of 50 Hz and 400 Hz. The 50 Hz units operate with 115 V_{rms} , while the 400 Hz units operate with either with 26 V_{rms} or 115 V_{rms} references.

2.2.2 Accuracy

The accuracy of synchro is the ability to give output voltages to define the rotor angle. It is measured in arc minutes or arc seconds. The synchro error is defined as the difference

between the true mechanical position angle of synchro shaft and the angle indicated by the stator voltages as its outputs.

2.2.3 Transformation ratio

The transformation ratio is defined as the ratio of output voltage to input voltage when the output is at maximum coupling. Usually the range of transformation ratio is in between 0.1 to 1.0.

2.2.4 Impedances

Impedances are usually specified in rectangular form as $R+jX$, where R is the sum of the AC and DC resistances and X is the reactance. It is expressed in ohms. The impedances applicable to synchro are

Z_{RO} : Rotor impedance with stator open circuit

Z_{RS} : Rotor impedance with stator short circuit

Z_{SO} : Stator impedance with rotor open circuit

Z_{SS} : Stator impedance with rotor short circuit

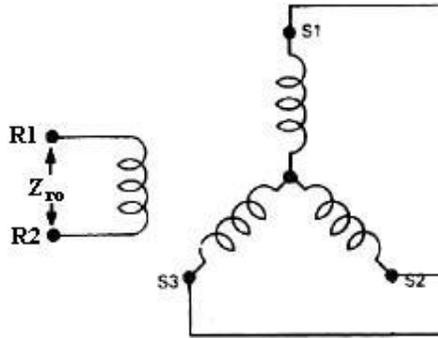
It is assumed that the above impedances are at zero position of the rotor. The impedances Z_{RO} , Z_{RS} are measured between the rotor terminals when the stator terminals are open and short circuited respectively. The impedances Z_{SO} , Z_{SS} are measured between the stator terminals when rotor terminals are open and short circuited respectively. In case of Z_{SO} and Z_{SS} , the impedance is measured between one terminal and the other two shorted together. The calculations of the impedances of synchro are shown in figure 2.6.

2.2.5 Input current

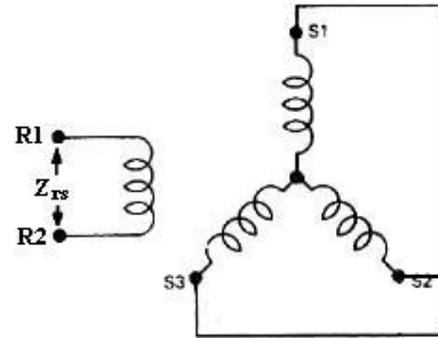
Input current is the current flowing through the rotor winding at rated voltage and frequency and it is expressed in Amp. For synchros, input current is typically less than 100 milliamps.

2.2.6 Input power

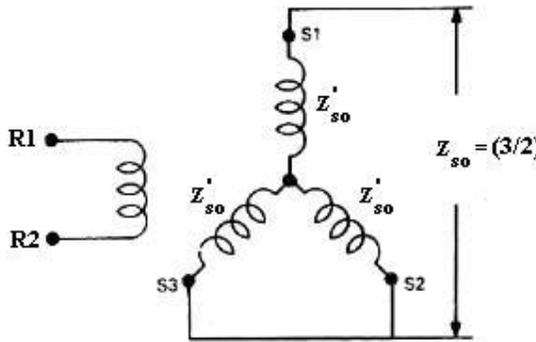
Input power is calculated from input current and input impedance and it is expressed in Watts. For synchros input power is typically less than 1 Watt.



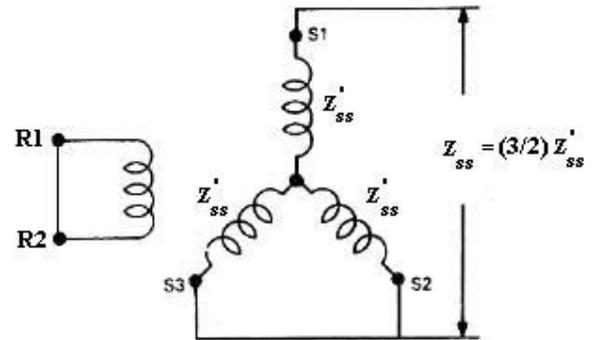
(a) Equivalent circuit to measure Z_{RO}



(b) Equivalent circuit to measure Z_{RS}



(c) Equivalent circuit to measure Z_{SO}



(d) Equivalent circuit to measure Z_{SS}

Figure 2.6: Calculation of rotor impedances (Z_{RO} , Z_{RS}) and stator impedances (Z_{SO} , Z_{SS}) of synchro

2.2.7 Part number

The synchro manufacturers have standardized the following designation:

(Size) (Type) (Reference frequency) (Modification state)

If the synchro accepts 26 V_{rms} reference signal, then 26V precedes the part number otherwise it can be operated at 115 V_{rms} reference signal. There are five modification states known as a, b, c, d or e. For example 23CX5b refers to a synchro with 2.3 inches diameter 115 volt, 50 Hz Control transmitter to mod state b.

2.3 Handling of synchros

The performance of any converter is mainly dependent on the input signals fed to it from the position sensor. But the actual signals generated by the sensor may not be available at the input of converter due to many external factors. This results in angular error at the output of converters. There are many external sources which introduce interference to the sensor outputs. The following section briefs possible interferences to sensor outputs and precautions to be taken for handling of synchros.

The magnetic interference caused by nearby motor's stray magnetic field and prefers to take the path through the shaft to the synchro. Hence providing a good housing structure to the resolver will be better option to avoid this interference. The electrical interference is mainly caused by cabling when the power lines and signal lines run close to the synchro. So it is suggested to maintain sufficient physical spacing between the same. It is also possible to avoid electrical interference by the usage of twisted pair cables for input and output signals of synchro. The pairs of cables for line voltages of synchro should have matched impedances because the usage of cables with un-matched impedances will lead to angular error. It is recommended to operate differential signal processing instead of single ended signal processing in order to reduce the cross talk between phase voltages of synchro. Moreover, the quality of excitation signal of synchro and design of first stage of converter to achieve impedance matching between synchro and converter play an important role to achieve good accuracy of the system. The mechanical position deviation between rotor and stator affects the reluctance of air gap that accounts for angular accuracy. The mounting and installation of resolver onto the motor also causes angular error. The axial screws are preferably used for installation.

2.4 Synchro-to-Digital Converter

The SDC converts three phase stator voltages of synchro into equivalent digital angle corresponding to the angle of synchro shaft. It takes R1, R2, S1, S2 and S3 as inputs and gives a 12-bit digital angle of synchro shaft as output. The representation of shaft angle in binary is implemented using Binary Angular Measurement (BAM) notation [2]. The value of least significant bit (LSB) is responsible for the resolution of a converter and the resolution is dependent on the word length of the digital output.

The synchro outputs V_{S1} , V_{S2} and V_{S3} are amplitude modulated signals. These signals are demodulated by the following approaches to obtain the shaft angle position.

- Tracking based approach
- Inverse tangent based approach

These methods provide a digital output corresponding to the angular position of the rotor shaft. The performance of the converters differs in their resolution, speed of rotation of the mechanism and the sensitivity towards non-ideal characteristics of the synchro.

2.4.1 Tracking based approach

In this method, the rotor winding of synchro is excited by an alternating signal, V_{Ref} and the three stator windings generate the amplitude modulated signals. The block diagram of angle determination using tracking approach is shown in figure 2.7. The three signals of synchro are converted into two signals using a scott-T transformer. The output signals of scott-T are called as resolver format signals. The amplitude of these signals is function of SINE and COSINE of the rotor shaft angle θ . The outputs of scott-T are denoted as V_S and V_C . The V_S of scott-T is applied as one of the input to cosine multiplier and the V_C of scott-T is applied as one of the input to sine multiplier. These multipliers act as Multiplying Digital-to-Analog Converters (MDAC).

The equations (2.2), (2.3) and (2.4) are converted to two signal format using scott-T transformer (Appendix A) and represented as

$$\left. \begin{aligned} V_s &= V \sin \omega t [\sin \theta] \\ V_c &= V \sin \omega t [\cos \theta] \end{aligned} \right\} \quad (2.5)$$

An estimated angle $\hat{\theta}$ is applied to the cosine multiplier and multiplied by V_s gives

$$V \sin \omega t [\sin \theta] \cos \hat{\theta} \quad (2.6)$$

Similarly, $\hat{\theta}$ is applied to the sine multiplier and multiplied by V_c gives

$$V \sin \omega t [\cos \theta] \sin \hat{\theta} \quad (2.7)$$

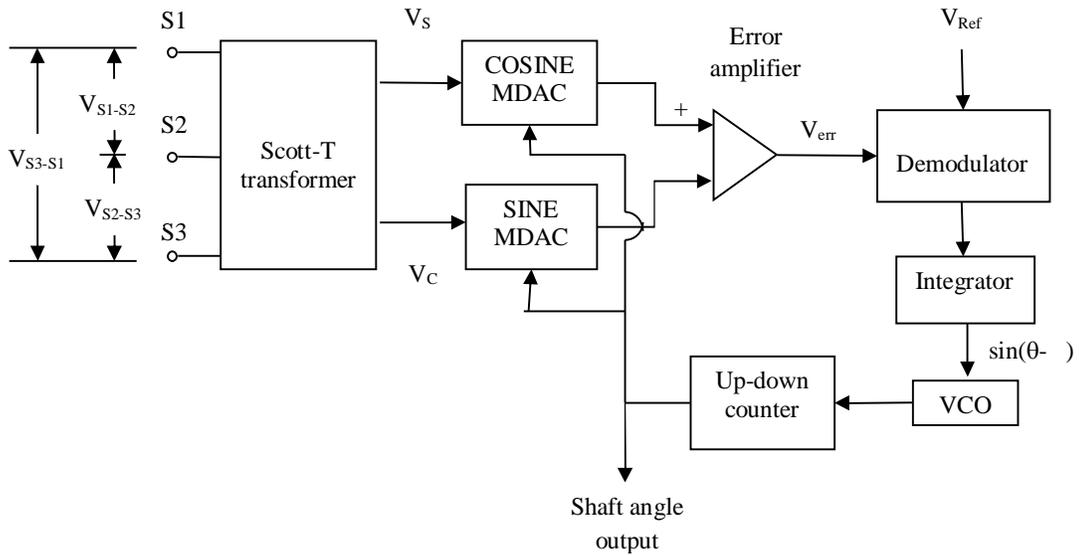


Figure 2.7: A tracking based Synchro-to-Digital Converter. The estimated shaft angle, $\hat{\theta}$ tracks actual mechanical shaft angle, θ until $\sin(\theta - \hat{\theta}) = 0$.

These two signals (2.6) and (2.7) are applied to the error amplifier to obtain an AC error signal of the form

$$\begin{aligned} V_{err} &= V \sin \omega t (\sin \theta \cos \hat{\theta} - \cos \theta \sin \hat{\theta}) \\ V_{err} &= V \sin \omega t \sin(\theta - \hat{\theta}) \end{aligned} \quad (2.8)$$

Equation (2.8) is the product of the excitation signal and sinusoidal function of shaft angle.

Here, the excitation signal needs to be suppressed to extract the shaft angle. Hence, a

demodulator which utilizes the synchro excitation voltage is used. It gives a DC error signal and proportional to $\sin(\theta - \theta_c)$. This error signal is then applied to an integrator. The integrator output drives a Voltage Control Oscillator (VCO), which in turn drives an up-down counter. The counter either increments or decrements depending on the value of error signal until $\sin(\theta - \theta_c) = 0$. Thus the DC error signal becomes zero.

For small values of $(\theta - \theta_c)$, $\sin(\theta - \theta_c) \approx (\theta - \theta_c)$ (2.9)

Then, $\theta - \theta_c = 0$

Therefore, $\theta = \theta_c$ (2.10)

Hence, the digital output of the counter, N represents the rotor shaft angle θ . The digital output automatically follows the input without any external convert command instruction. Thus, tracking based SDC provides a DC output signal directly proportional to the rotor shaft speed.

2.4.2 Inverse tangent based approach

In this method, the rotor winding of synchro is excited by an alternating signal and the three stator windings generate the amplitude modulated signals. The block diagram of angle determination using inverse tangent approach is shown in figure 2.8. The three signals of synchro are converted into two signal format using an electronic scott-T circuit. The amplitude of these signals is a function of SINE and COSINE of the rotor shaft angle θ . The outputs of scott-T are denoted as V_s and V_c . The ratio of scott-T signals amplitude is the tangent of rotor angle. Therefore, the arctangent of ratio of V_s and V_c gives rotor angle.

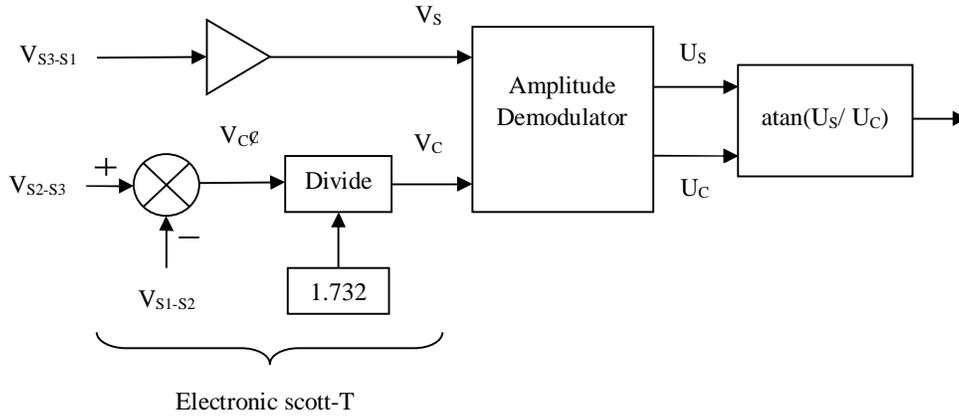


Figure 2.8: An inverse tangent based Synchro-to-Digital Converter. The demodulated signals of synchro are applied with inverse tangent trigonometric operation to measure shaft angle of synchro.

From equation (2.2), it can be noticed that the voltage between S3 to S1 directly gives V_s

$$V_s = V \sin \theta \tag{2.11}$$

Consider (2.3) & (2.4)

$$\begin{aligned} V_c &= V \sin \theta [\sin(\theta + 120^\circ) - \sin(\theta + 240^\circ)] \\ &= V \sin \theta [-0.5 \sin \theta + 0.866 \cos \theta + 0.5 \sin \theta + 0.866 \cos \theta] \\ &= V \sin \theta [1.732 \cos \theta] \end{aligned}$$

Dividing by 1.732,

$$V_c = V \sin \theta \cos \theta \tag{2.12}$$

Equations (2.11) and (2.12) are called as two signal format of synchro signals. These signals are applied to an amplitude demodulator to obtain amplitude portion of V_s and V_c .

$$\left. \begin{aligned} U_s &= V \sin \theta \\ U_c &= V \cos \theta \end{aligned} \right\} \tag{2.13}$$

Applying inverse of tangent operation to equation (2.13) and the result denoted by

$$\begin{aligned} &= \arctan (U_s / U_c) \\ &= \arctan (V \sin \theta / V \cos \theta) \end{aligned} \tag{2.14}$$

The arctangent operation results in an angle between 0° to 90° . An absolute angle estimator gives the actual shaft angle, using the quadrant information. The quadrant detector gives the quadrant information in which rotor shaft angle falls using two digital bits. Based on the digital bits the actual angle is calculated in the following way

$$= \begin{cases} & \text{for I quadrant} \\ 180^{\circ}- & \text{for II quadrant} \\ 180^{\circ}+ & \text{for III quadrant} \\ 360^{\circ}- & \text{for IV quadrant} \end{cases}$$

2.5 Literature review of synchro/resolver-to-digital conversion methods

This section comprehensively presents the literature review on synchro/resolver-to-digital converters. The rotor displacement of the synchro using six unique states was introduced [3]. Using these states, the octant in which the corresponding angle can be known rather than estimating the absolute angle.

The AC encoded synchro signals are converted to DC values using the synchronous demodulators [4]. These DC values are coupled to an ADC through an analog multiplexer. The ADC converts the DC values to a digital value. A processor is programmed to extract the shaft angle from the three digital equivalents of synchro signals.

Resolver is another sensor used for positional measurements, having one rotating excitation winding and two stator windings oriented at 90° to each other. The output voltage of a resolver when it is excited by an ac supply is called as reference voltage, V_{Ref} . As resolver shaft rotates, different voltages are induced into two stator windings. The voltage induced in one stator winding is proportional to the SINE of the shaft angle; while the voltage induced into the other stator windings is proportional to the COSINE of the shaft angle [5].

John Pezzlo and Chong Loh Tsiang [6] mentioned the disadvantages of contacting transducers to measure the angular position of rotating equipment, which can be overcome by

using non-contacting devices like resolver. According to this method, comparison of the voltage induced in the rotor with the one of the stator voltage gives pulse width signal which is proportional to resolver shaft angle.

George W. Miller and Larry A. Meyer [7] presented a Resolver-to-Digital Converter (RDC) which is controlled by digital excitation signals. In this technique, an oscillator and a phase shifter supply multi-phase AC voltages to the stator windings and induce an AC voltage in the rotor winding. The phase of AC voltage in rotor winding varies with the angular position of the rotor. Therefore, the angular position of the rotor can be computed by measuring phase difference between voltage induced in rotor winding and the reference voltage. This time gap can be expressed as a digital representation of rotor shaft angle. But aging of the components may cause a change in phase difference resulting in inaccuracies in the measured angle.

Edward L. Denham and Michael J. Tusso [8] proposed a method to monitor the position of a controlled machine using the feedback information provided by the resolver. Here, the true position of monitored system represents the amount of phase shift between the resolver output signal and the reference signal after passing through the entire circuit path. This technique compensates the systematic phase shift errors produced by signal conditioning circuitry.

The control of programmable limit switch system by a microcomputer using the digital resolver shaft angle is introduced by Peter G. Serev and Roger M. Bogin [9]. The digital shaft angle of resolver is represented by an 11-bit binary word. The first three most significant bits are obtained using polarity and amplitude comparisons of sine and cosine voltages of the resolver. The resolver outputs are converted to the absolute values and processed using a look-up table to obtain least significant 8-bits. The microcomputer appends 3 bits from logic converter to the 8 bits from table to get an 11-bit binary word of resolver shaft.

Peter G. Serev proposed a microcontroller based RDC to extract the shaft angle of the resolver [10]. The resolver outputs are demodulated using the synchronous sample-and-hold approach, in which they are sampled at their peaks in synchronous with the reference voltage. Then the absolute peak values are processed using digital signal processing technique and trigonometric identities to represent the shaft angle in digital fashion.

Bruce N. Eyerly and Donald R. Cargille [11] discussed the effect of phase shift between input and output signals of the resolver. They introduced a digital computer multiplexer (MUX) based circuit to compensate for resolver angle error without the use of special compensation windings on the resolver.

A novel method [12, 13] to determine the resolver shaft angle by concatenating the octant and linear position tangent values was proposed. The octant provides 3-bit code as the three most significant bits and the linearized values as the least significant bits to obtain the angle.

Martin Staebler [14] presented a TMS320F240 DSP solution for obtaining the angular position and speed of a resolver. This method adopts under-sampling and an inverse tangent algorithm to decode the resolver output signals. For achieving a higher angular resolution, an oversampling technique is used.

Martin Piedl et al. [15] designed a low cost resolver system using a DSP. The advantages of resolver over Hall Effect sensors are discussed for determining rotor position and velocity control of the motor. The processor demodulates resolver signals and provides the sampled version. The sampled values are converted to digital values which are used to calculate the shaft angular position.

Aengus Murray et al. [16] described a new resolver position sensing system for automotive applications. A variable reluctance resolver is chosen as position sensor and a tracking loop based RDC is developed. The designed RDC accuracy achieved is 11 arc minute. This work

also focuses on resolver and RDC faults of the system. However, this paper has not provided the location of interconnection faults between resolver and RDC.

Low cost software based RDC was proposed by A.O.Di Tommaso and R. Miceli [17]. This RDC mainly needs DAC, two ADCs, digital filters and a proportional integral (PI) controller and are implemented in a DSP. The comparison between the proposed RDC and a commercial encoder is also presented in the paper.

An approach for Resolver-to-DC conversion [18, 20] is reported. This method is based on processing of the difference between absolute values of the demodulated stator signals. A linearization principle was established to introduce a compensation term. Hence by adding the compensation term to the absolute difference term results in linearized output for the resolver shaft angle.

The rotary orientation of a motor using the resolver is described by Robert Herb [19]. This system comprises of a microcontroller that is used for triggering and evaluating the resolver signals. A tracking procedure is executed on resolver signals for evaluating the actual rotor angle.

Reza Hoseinnezhad [21] presented a novel angle tracking observer for position and speed measurement. The finite gain stability of the proposed closed loop observer was analyzed and the simulation results of linear time invariant angle tracking observer (LTI-ATO) and Kalman filter methods shows instability of the system at high speed and acceleration. But the proposed closed loop observer possesses stability at high speed and acceleration with finite tracking errors.

The resolver-to-digital conversion method needs an accurate clock unit and associative conditioning blocks to excite the resolver [22]. The resolver output signals are then demodulated followed by analog to digital conversion. The Erasable Programmable Read Only Memory (EPROM) based arctangent function gives shaft angle. Two 8-bit Analog-to-

Digital Converters (ADC) have been used for resolver output signals and hence a resolution angle of 1.4° is achieved. For improving the accuracy of the RDC, the size of EPROM needs to be increased.

A technique for Resolver-to-DC converter is presented by Anucha Kaewpoonsuk et al. [23]. The demodulator is implemented using two full wave rectifiers; two sinusoidal amplitude detectors and control signal generator [24]. These signals are processed by the inverse-sine function and Triangular-to-Sawtooth waveform converter provides an output voltage proportional to the resolver shaft angle.

A digital signal processor (DSP) based RDC is presented [25]. In this method, the sample and hold circuits are employed to demodulate resolver output signals. The obtained envelopes are used to extract shaft rotation using a lookup table (LUT). The precision of the digital technique depends on the resolution of ADC and digital-to-analog converters (DAC) external to the DSP processor.

The resolver angle estimation [26-27] is based on comparison between excitation and resolver output signals. This method does not require LUT or processor but for converter operation, a separate signal generator is necessary to excite the resolver and to generate the signals for demodulation.

A fully integrated Field Programmable Gate Array (FPGA) board is used to control the motor by extracting the rotor position and speed [28]. Here, the resolver signals are sampled and converted to digital signals using ADC module. The resolver processing unit adopts an algorithm called Angle Tracking Observer (ATO), which extracts position and speed of the resolver shaft. This method is more suitable to low speed applications.

Lazhar Ben-Brahim and Mohieddine Benemmar [29] presented a novel implementation of Phase locked loop (PLL). In this design, the extraction circuit replaces the LUT. It provides the equivalent demodulated resolver signals (also called as feedback signals). The extraction

circuit composed of two comparators, few logic circuits and two Sample & Hold circuits (S&H). Then the resolver shaft angle is computed using the demodulated signals of resolver and feedback signals.

Joan Bergas-Jane et al. [30] presented high accuracy all digital RDC. The basic blocks of conventional tracking RDC, the phase detector and the loop filter are implemented in software by frequency shifting techniques and a decoupled synchronous reference frame based phase lock loop is presented. This PLL approach gives both the angular position and speed of the resolver shaft.

A RDC based on synchronous demodulation is presented [31]. Here, two ADCs of 10-bit are used to sample and demodulate the resolver output signals. Then the angle is computed using an ATO.

The design of RDC using an inverse tangent method is described [32]. The synchronous demodulated resolver signals are applied to the S&H circuits separately. The absolute values of S&H outputs are applied with an inverse tangent operation to extract the rotor angle of the resolver. The simulation environment gives accurate measurement of shaft angle under the assumption of ideal operation of the system.

The demodulation of resolver signals for rotor position measurement is proposed using the synchronous integration method [33]. Here, the demodulation is achieved by multiplying integrated values of resolver outputs with the sign of the delayed carrier signal. The tracking observer based control loop provides the actual angle for the demodulated resolver outputs.

The DSP implementation of controller area network (CAN) bus for angle measurement system was introduced [34]. This paper mainly discuss CAN interface circuits and communication module for transmission of the angle data. For computation of the resolver shaft angle, a standard Resolver-to-Digital Converter AD2S83 is used.

Jakub Szymczak et al. [35] introduced AD2S1210 tracking RDC. The authors discussed the angular error caused by amplitude mismatch and differential phase between resolver output signals. This RDC designed based on type-II tracking loop to perform position and velocity calculations. There are special care is taken for input and output signals of resolver using low pass filters and the AD8397 high current operational amplifier respectively to achieve good performance.

In the literature, various schemes have been proposed for SDC/RDC to measure the rotor shaft position and speed. The design methods are based on tracking approach and inverse tangent approach. The researchers focused their efforts to reduce the hardware complexity and cost in addition to improving the linearity and accuracy of the converter.

References

- [1] Geoffrey S Boyes, "Synchro and Resolver conversion", Memory Devices Ltd, UK, 1980.
- [2] Philip A. Laplante, "Real Time Systems Design and Analysis", Wiley-India edition, New Delhi, 2005.
- [3] J.C. Rice, T.A. Tucker, "Synchro-to-digital converter", U.S. Patent 4031531, June 21, 1977.
- [4] James G. Deppe, Joseph R. Biel, "AC encoded signal to digital converter", U.S. Patent 5034743, July 23, 1991.
- [5] Understanding resolvers and Resolver-to-Digital Conversion, Admotec Inc., Lebanon, NH, USA, 1998.
- [6] J. Pezzlo, C.L. Tsiang, "Resolver to pulse width converter", US Patent 3803567, April 9, 1974.
- [7] G.W. Miller, L.A. Meyer, "Resolver to digital converter", US Patent 3990062, November 2, 1976.
- [8] E.L. Denham, M.J. Tusio, "Compensated resolver feedback", US Patent 4472669,

September 18, 1984.

- [9] Peter G. Serev, Roger M. Bogin, "Programmable limit switch system using resolver-to-digital angle converter," US Patent 4511884, April 16, 1985.
- [10] Peter G. Serev, "Microcontroller based resolver-to-digital converter," US Patent 4989001, January 29, 1991.
- [11] B. N. Eyerly, D.R. Cargille, "Phase compensation for electromagnetic resolvers," US Patent 5134397, July 28, 1992.
- [12] S.P. Vlahu, "Direct resolver to digital converter," U.S. Patent 5912638, June 15, 1999.
- [13] S.P. Vlahu, "Variable reluctance resolver to digital converter," U.S. Patent 5949359, September 7, 1999.
- [14] Martin Staebler, "TMS320F240 DSP Solution for Obtaining Resolver Angular Position and Speed," Texas Instruments Application Report, SPRA605, February 2000.
- [15] M. Piedl, M. Barani, R. Flanary, "Low cost resolver system," US Patent 6084376, July 4, 2000.
- [16] Aengus Murray, Bruce Hare and Akihiro Hirao, "Resolver position sensing system with integrated fault detection for automotive applications," IEEE Proceedings of Sensors, Orlando, USA, pp. 864-869, 2002.
- [17] A.O. Di Tommaso and R. Miceli, "A new high accuracy software based resolver-to-digital converter," The 29th annual conference of the IEEE Industrial Electronics Society, Roanoke, USA, pp. 2345-2440, 2003.
- [18] M. Benammar, L. Ben-Brahim, and Mohd.A. Alhamadi, "A novel resolver-to-360^o linearized converter," IEEE Sensors Journal, vol. 4, no. 1, pp. 96-101, 2004.
- [19] Robert Herb, "Device and method for determining the rotary orientation of a motor through use of a resolver signal derived from the rotary orientation," US Patent 6931918 B2, August 23, 2005.

- [20] M. Benammar, L. Ben-Brahim and Mohd.A. Alhamadi, "A high precision resolver-to-DC Converter," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 6, pp. 2289-2296, 2005.
- [21] Reza Hoseinnezhad, "Position Sensing in Brake-By-Wire Callipers Using Resolvers," *IEEE Transactions on Vehicular Technology*, vol. 55, no.3, pp. 924-932, 2006.
- [22] C. Attaianese and G. Tomasso, "Position measurement in industrial drives by means of low-Cost resolver-to-digital converter," *IEEE Transactions on Instrumentation and Measurement*, vol. 56, no. 6, pp. 2155-2159, 2007.
- [23] Anucha K., W. Petchmaneelumka, A. Rerkratn, S. Tammaruckwattana, and V. Riewruja, "A Novel Resolver-to-DC Converter Based on OTA based Inverse Sine Function Circuit," *SICE Annual Conference, Japan*, pp. 609-614, August 2008,.
- [24] Anucha Kaewpoonsuk, Ratchanoo Katman, Thawatchai Kamsri, Apinai Rerkratn and Vanchai Riewruja, "A Simple Amplitude Detector-based Demodulator for Resolver Converters," *IEEE International Conference on Control, Automation and Systems*, Gyeonggi-do, Korea, pp. 370-373, October 2010.
- [25] S. Sarma, V. Agarwal, and K. Udupa, "Software-based resolver-to-digital conversion using DSP," *IEEE Transaction on Industrial Electronics*, vol. 55, no. 1, pp. 371-379, 2008.
- [26] L. Ben-Brahim, M. Benammar, M.Alhamadi, N.Alemadi, and M. Alhitmi, "A new low cost linear resolver converter," *IEEE Sensors Journal*, vol. 8, no. 10, pp. 1620-1627, 2008.
- [27] L. Ben-Brahim, M. Benammar, M.Alhamadi, "A Resolver Angle Estimator Based on its Excitation signal," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 574-580, 2009.
- [28] L. Idkhajine, E. Monmasson, M.W. Naouar, A. Prata, and K. Bouallaga, "Fully

- integrated FPGA- based controller for synchronous motor drive,ö IEEE Transactions on Industrial Electronics, vol. 56, no. 10, pp. 4006- 4017, 2009.
- [29] Lazhar Ben-Brahim and Mohieddine Benammar, öA new PLL method for resolvers,ö IEEE International Power Electronics Conference, Sapporo, pp. 299-305, June 2010.
- [30] J. Bergas-Jane, C. Ferrater-Simon, G. Gross, R. Ramirez-Pisco, S. Galceran-Arellano, and J. Rull-Duran, öHigh Accuracy All Digital Rsolver-to-Digital Conversion, IEEE Transactions on Industrial Electronics,ö vol. 59, no. 1, pp. 326-333, 2012.
- [31] D. A. Khaburi, öSoftware-based resolver-to-digital converter for DSP-Based drives using an improved angle-tracking observer,ö IEEE Transactions on Instrumentation and Measurement, vol. 61, no. 4, pp. 922-929, 2012.
- [32] S.C.M. Reddy, K.N. Raju, öInverse Tangent Based Resolver to Digital Converter ó A Software Approach,ö International Journal of Advances in Engineering & Technology, vol. 4, issue. 2, pp. 228-235, 2012.
- [33] Nay Lin Htun Aung, Chao Bi, Abdullah Al Mamun, Cheng Su Soh, and Yu YinQuan, öA Demodulation Technique for Spindle Rotor Position Detection with Resolver,ö IEEE Transactions on Magnetics, vol. 49, no. 6, pp. 2614-2619, 2013.
- [34] Yifei Wu, Zhihang Wang and Qingwei Chen, öA Novel Integrated Angle Measurement System,ö Applied Mechanics and Materials, Vols. 373- 375, pp. 838-843, 2013.
- [35] J. Szymczak, S. O'Meara, J.S. Gealon and C.N. De La Rama, öPrecision Resolver-to-Digital Converter Measures Angular Position and Velocity,ö March, 2014.

CHAPTER 3

MATHEMATICAL STUDY OF SYNCHRO AND

MODELING OF SYNCHRO-TO-DIGITAL

CONVERTER

CONTENTS:

3.1 Derivation of synchro transmitter's electrical signals

3.2 Methodology to model SDC

3.3 Simulation results

3.4 Study of non-ideal characteristics

3.5 Conclusion

References

This chapter deals with the mathematical study of synchro, which is useful to emulate the functional behavior and to predict the effect of input excitation signal on the output of the synchro. As the shaft angle information is present in the peak amplitudes of synchro outputs, a method has been introduced to extract the peak amplitude levels. This approach employs a dual stage monoshot and Sample & Hold circuit (S&H) to get the peak amplitude information. A novel way of finding the speed of motor shaft using Synchro-to-Digital Converter (SDC) through synchro is proposed. In this scheme the computation of the speed of motor doesn't require any separate circuit. The quadrant detector which is used to know the quadrant in which shaft angle falls itself gives the speed output of the motor. The complete block level model of SDC is presented using MATLAB/Simulink environment.

There are some undesirable characteristics such as amplitude imbalance, imperfect quadrature, reference signal phase shift and excitation signal distortion, which affects the ideal nature of synchro. As a result, the synchro cannot generate correct electrical signals in terms of amplitudes and phases. Hence, these characteristics give rise to inaccuracies in the functioning of the synchro/resolver-to-digital converters. In this chapter, a study is carried out on causes of non-ideal characteristics and its effects on measured angle of SDC.

3.1 Derivation of synchro transmitter's electrical signals

The equivalent circuit of a synchro along with the winding parameters is shown in figure 3.1. The resistance and self-inductance of the synchro rotor coil are R_r , L_r ; the resistance and self-inductance of the synchro stator coil are R_s , L_s .

The current flowing through the rotor winding is i_r and current flowing through stator windings are i_{s1} , i_{s2} and i_{s3} . Considering $R_{s1}=R_{s2}=R_{s3}=R_s$ and $L_{s1}=L_{s2}=L_{s3}=L_s$ then the voltages induced in stator windings are given by

$$V_{Ref} = R_r i_r + L_r \frac{di_r}{dt} \tag{3.1}$$

$$V_{S1} = R_s i_{s1} + L_s \frac{di_{s1}}{dt} + L_{sm} \cos(+120^\circ) \frac{di_r}{dt} \tag{3.2}$$

$$V_{S2} = R_s i_{s2} + L_s \frac{d}{dt} i_{s2} + L_{srm} \cos(\theta) \frac{d}{dt} i_r \quad (3.3)$$

$$V_{S3} = R_s i_{s3} + L_s \frac{d}{dt} i_{s3} + L_{srm} \cos(\theta + 240^\circ) \frac{d}{dt} i_r \quad (3.4)$$

where, L_{srm} is mutual inductance between the stator and rotor of synchro; θ - angular position of the shaft

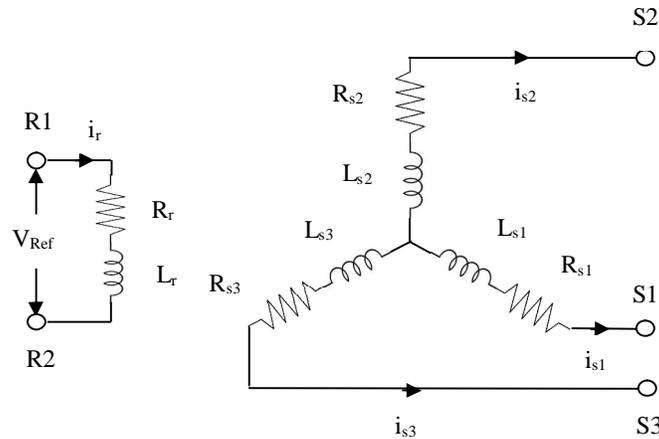


Figure 3.1: Equivalent circuit of synchro with rotor coil resistance R_r and inductance L_r ; stator coil resistances R_{s1} , R_{s2} , R_{s3} and inductances L_{s1} , L_{s2} , L_{s3} .

The synchro is excited by an AC signal and given as

$$V_{Ref} = V \sin \omega t \quad (3.5)$$

where V is the peak amplitude and ω is the angular frequency of the excitation signal.

Solving equation (3.1) to get expression for the excitation current $i_r(t)$,

$$L \frac{d}{dt} (V \sin \omega t) = L (R_r i_r + L_r \frac{d}{dt} i_r)$$

$$\frac{d}{dt} \sin \omega t = I_r(s) (R_r + sL_r)$$

$$I_r(s) = \frac{V \sin \omega t}{R_r + sL_r}$$

$$= \frac{V}{R_r} \frac{\sin \omega t}{1 + s \frac{L_r}{R_r}} + \frac{V}{R_r} \frac{\cos \omega t}{1 + s \frac{L_r}{R_r}}$$

$$\begin{aligned}
 &= \frac{2}{\omega} \left[\frac{2}{2\omega} \sin 2\omega t + \frac{2}{2\omega} \sin 2\omega t \right] + \frac{2}{\omega} \left[\frac{2}{2\omega} \sin 2\omega t + \frac{2}{2\omega} \sin 2\omega t \right] \\
 &= \frac{2}{\omega} \left[\frac{2}{2\omega} \sin 2\omega t - \frac{2}{2\omega} \sin 2\omega t \right] + \frac{2}{\omega} \left[\frac{2}{2\omega} \sin 2\omega t + \frac{2}{2\omega} \sin 2\omega t \right] \\
 I_r(t) &= \frac{2}{\omega} \left[R \sin \omega t - \omega L \cos \omega t + \omega L e^{j\omega t} \right] \\
 \text{Under steady state, } I_r(t) &= \frac{2}{\omega} \left[R \sin \omega t - \omega L \cos \omega t \right] \quad (3.6)
 \end{aligned}$$

Because the voltage developed in secondary coils is mainly due to the mutual inductance and hence, the current in the synchro stator coils is assumed as negligible. Substituting $I_r(t)$ into equations (3.2), (3.3) and (3.4) gives the expressions for synchro output signals

$$\begin{aligned}
 V_{S1} &= L_{sr1} \cos(+120^\circ) \dot{i}_r \\
 &= L_{sr1} \cos 120^\circ \left[\frac{2}{\omega} \left[R \sin \omega t - \omega L \cos \omega t \right] \right] \\
 &= \frac{2 L_{sr1} \cos 120^\circ}{\omega} \left[R \omega \cos \omega t + \omega^2 L \sin \omega t \right]
 \end{aligned}$$

In the ideal case when the resistance of the excitation coil is zero, the phase of the output voltage is same as that of the excitation voltage. Hence the approximated phase voltages of synchro are given as

$$\left. \begin{aligned}
 V_{S1} &= V \sin t \cos(+120^\circ) \\
 V_{S2} &= V \sin t \cos() \\
 V_{S3} &= V \sin t \cos(+240^\circ)
 \end{aligned} \right\} \quad (3.7)$$

3.2 Methodology

The block diagram of Synchro-to-Digital Converter is shown in figure 3.2. In this method, the synchro excited with a sinusoidal signal, V_{Ref} of peak-to-peak amplitude of 20 V with a frequency of 50 Hz. The mathematical expression for the excitation signal is given as

$V_{Ref}(t) = V \sin \omega t$. The reference signal is modulated by the angular rotation of synchro shaft and produces three modulated signals. To eliminate the quadrature components generated by the speed voltage, the angular velocity $d\theta/dt$ of the rotor should be lower than excitation frequency (ω) [1]. Therefore, the modulated signals are given as

$$V_{S1}(t, \theta) = V \sin t \cos(\theta + 120^\circ)$$

$$V_{S2}(t, \theta) = V \sin t \cos(\theta)$$

$$V_{S3}(t, \theta) = V \sin t \cos(\theta + 240^\circ)$$

Where k is the synchro transformation ratio and it is assumed as unity.

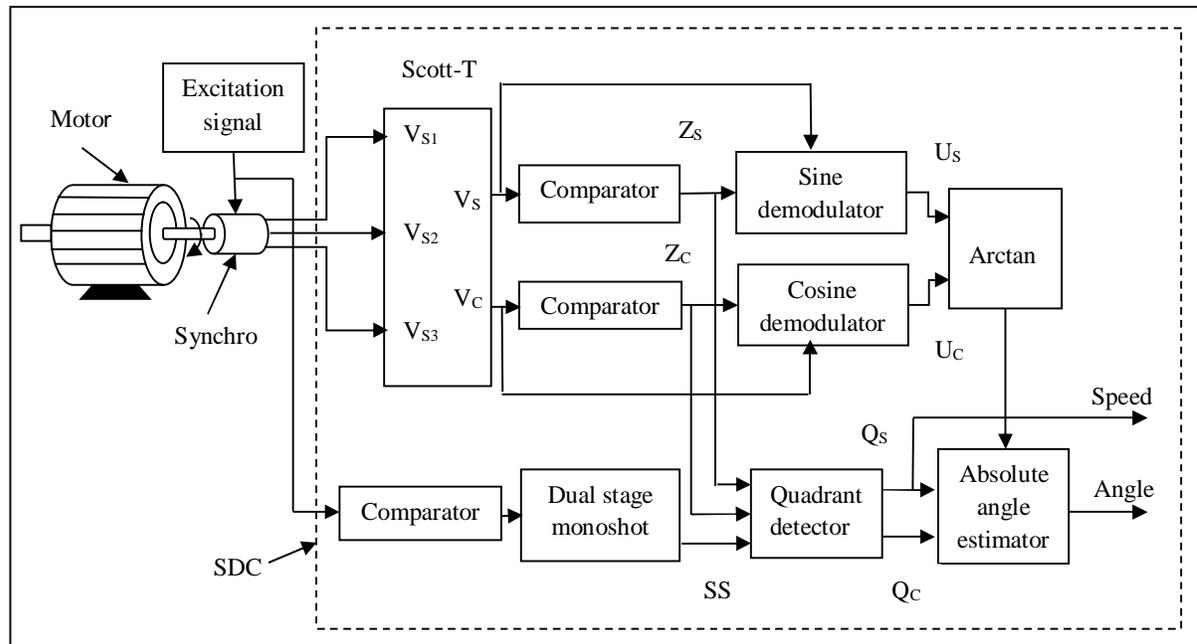


Figure 3.2: Block diagram of Synchro-to-Digital Converter (enclosed with dotted lines). The synchro is mounted on shaft of the motor and generated outputs are connected to Synchro-to-Digital Converter.

The above equations are called as the phase voltages of the synchro and these can be made as line voltages by considering voltage between the terminals S3 and S1; S2 and S3; S1 and S2.

The trigonometric simplification to obtain the line voltages of synchro is as follows

$$\begin{aligned} V_{S3-S1} &= V \sin t \cos(\theta + 240^\circ) - V \sin t \cos(\theta + 120^\circ) \\ &= V \sin t \{[\cos \theta \cos 240^\circ - \sin \theta \sin 240^\circ] - [\cos \theta \cos 120^\circ - \sin \theta \sin 120^\circ]\} \end{aligned}$$

$$= \zeta 3V \sin t \sin \quad (3.8)$$

$$\begin{aligned} V_{S2-S3} &= V \sin t \cos - V \sin t \cos(+240^0) \\ &= V \sin t \{ \cos - [\cos \cos 240^0 \sin \sin 240^0] \} \\ &= V \sin t [1.5 \cos - 0.866 \sin] \\ &= \zeta 3V \sin t \sin(+120^0) \end{aligned} \quad (3.9)$$

$$\begin{aligned} V_{S1-S2} &= V \sin t \cos(+120^0) - V \sin t \cos \\ &= V \sin t \{ [\cos \cos 120^0 \sin \sin 120^0] - \cos \} \\ &= -V \sin t [1.5 \cos + 0.866 \sin] \\ &= \zeta 3V \sin t \sin(+240^0) \end{aligned} \quad (3.10)$$

Hence, the scaling of $1/\sqrt{3}$ is done for the equations (3.8), (3.9) and (3.10) implies to

$$\left. \begin{aligned} V_{S3-S1}(t, \theta) &= V \sin t \sin \\ V_{S2-S3}(t, \theta) &= V \sin t \sin(+120^0) \\ V_{S1-S2}(t, \theta) &= V \sin t \sin(+240^0) \end{aligned} \right\} \quad (3.11)$$

From equation (3.11), it is difficult to estimate the rotor shaft angle because the amplitude variations of the line voltages are varying sinusoidally and the quadrant in which shaft angle falls cannot be determined. In order to find the actual shaft angle there is a need of quadrature signals whose amplitude variations are in 90^0 phase shift. So the synchro three signals format is converted into two signals format using scott-T circuit. The mathematical simplification for the scott-T output signals is given in Appendix A. So the expressions for scott-T output signals are given as

$$\left. \begin{aligned} V_S(t, \theta) &= V[\sin(\theta)] \sin \omega t \\ V_C(t, \theta) &= V[\cos(\theta)] \sin \omega t \end{aligned} \right\} \quad (3.12)$$

From equation (3.12), it is inferred that angular information of synchro shaft is contained in amplitudes of $V_S(t, \theta)$ and $V_C(t, \theta)$. The basic idea of this method is to extract the instantaneous peak amplitudes of scott-T outputs using demodulators and division of these

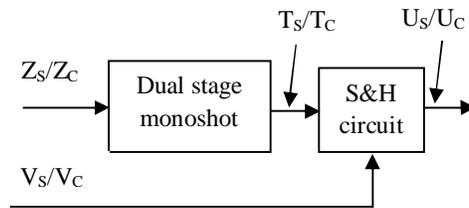
values followed by inverse tangent operation. Finally, the absolute shaft angle is calculated using the quadrant detector bits.

The outputs of the scott-T circuit are amplitude modulated signals. The process of extraction of the positive peak amplitudes of scott-T outputs is called as demodulation. So a demodulator is designed using a dual stage monoshot and S&H circuit. Figure 3.3 demonstrates the internal blocks and the operation of the demodulators with associated waveforms to extract the positive peak amplitudes of V_S and V_C . In this demodulation, the scott-T output signals and its zero crossing outputs are used to extract the rotation angle information of the shaft. The zero crossing outputs for scott-T signals can be generated by comparators and denoted as Z_S and Z_C . Since the signals V_S has a frequency of 50 Hz, the positive peak amplitudes occurs at 5 ms for every cycle. So a triggering signal should be generated at 5 ms. The triggering signal can be achieved by using dual stage monoshot. The dual stage monoshot generation of triggering signals T_S and T_C is shown in figure 3.3.

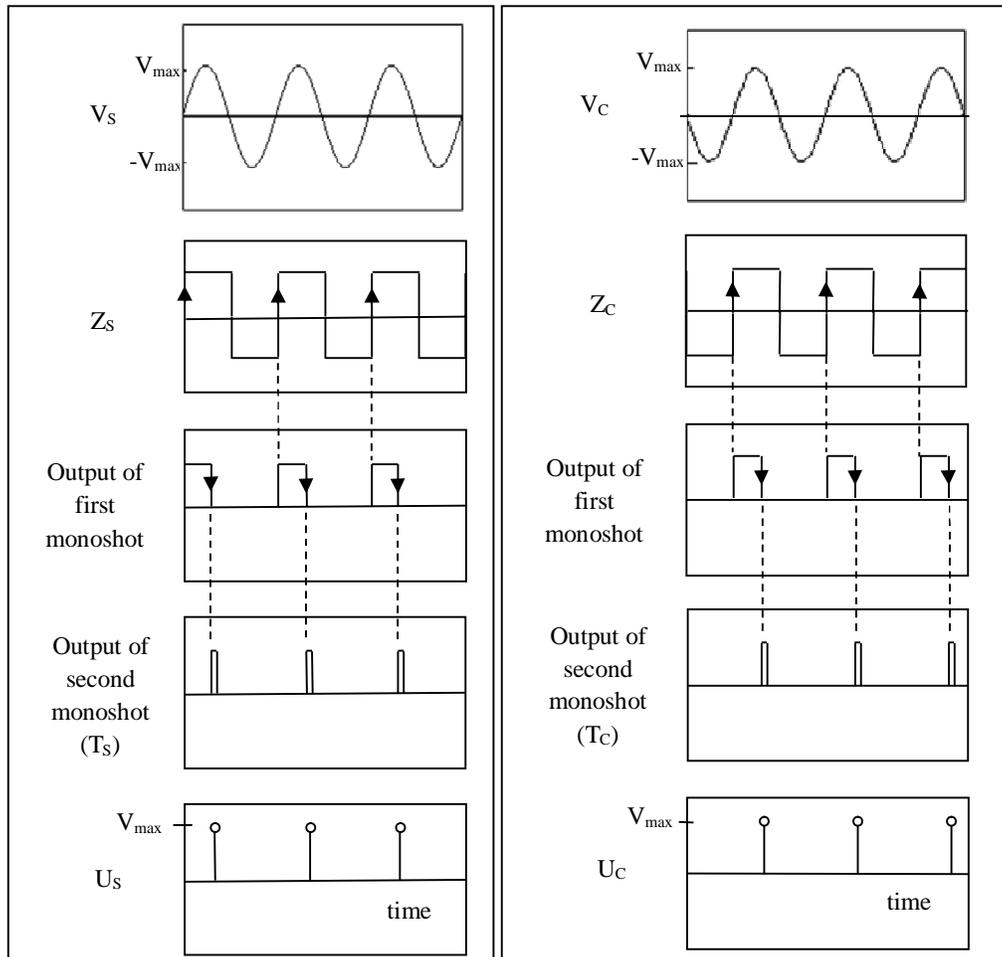
A single monoshot, which outputs pulses of desired width when a change in the logical input is detected. The first monoshot triggered to detect a rising edge of the input and the generated output is connected to the second monoshot. The second monoshot triggered to detect a falling edge of the input. The output of second monoshot is used as triggering signal for the S&H circuit to sample the positive peak amplitude levels.

There are two demodulators called sine and cosine demodulator to extract the positive peak amplitude levels of scott-T outputs. In figure 3.3, the scott-T outputs are 180° out of phase with each other because in II quadrant, V_S amplitude is positive and V_C amplitude is negative. The signals U_S and U_C are sample & hold outputs of the signals V_S and V_C respectively. The sampled outputs are given as

$$\left. \begin{aligned} U_S &= V \sin(\theta) \\ U_C &= V \cos(\theta) \end{aligned} \right\} \quad (3.13)$$



(a) Internal blocks of the demodulator. It comprises of dual stage monoshot to generate triggering signal and S&H circuit to give peak amplitude levels



(b) Input and outputs of sine demodulator

(c) Input and outputs of cosine demodulator

Figure 3.3: Internal operation of the demodulators. The signals V_s and V_c are 180° out of phase under the assumption of the rotor shaft is at rest and is in II quadrant.

From the equation (3.13), the signals U_s and U_c contains only angular information. The positive peak amplitude signals of scott-T outputs are divided and applied with inverse tangent operation to get the rotor shaft angle in the range 0° to 90° .

$$\begin{aligned}\theta &= \arctan(U_S / U_C) \\ &= \arctan [V_S \sin(\theta) / V_C \cos(\theta)]\end{aligned}\quad (3.14)$$

The harmonic interference [2] exists in the three phase synchro voltage signals. The harmonic components still continue in electronic scott-T output signals V_S and V_C . These components can be cancelled ratio-metrically (from equation 3.14) such that the conversion error in the angle measurement is minimized. The full 360° rotation of shaft angles can be obtained by selection of quadrant detection logic. The following phenomenon gives the logic to the design the quadrant detector.

The variation of V_S and V_C signals with respect to reference signal V_{Ref} is described using the equations (3.5) and (3.12). It is evident that in I quadrant both V_S and V_C are in phase with V_{Ref} . In the II quadrant, V_S is in phase and V_C becomes out of phase with V_{Ref} . In the III quadrant both V_S and V_C are out of phase with V_{Ref} . In the IV quadrant, V_S is out of phase and V_C becomes in phase with V_{Ref} . So a quadrant detector block is required to determine the quadrant in which the synchro shaft angle falls. The table 3.1 is used to determine the quadrant of shaft angle.

Table 3.1: Analysis of the quadrant detector

Quadrant	Q_S	Q_C	Absolute
			angle (degrees)
I (0° - 90°)	1	1	
II (90° - 180°)	1	0	180° -
III (180° - 270°)	0	0	180° +
IV (270° - 360°)	0	1	360° -

Based on above analysis, the absolute angle estimator is modeled and described using a flowchart shown in figure 3.4. It takes θ , Q_S and Q_C as the inputs and gives actual rotor

position of shaft. The rotor shaft angle also can be represented in binary using the Binary Angular Measurement (BAM) notation [3].

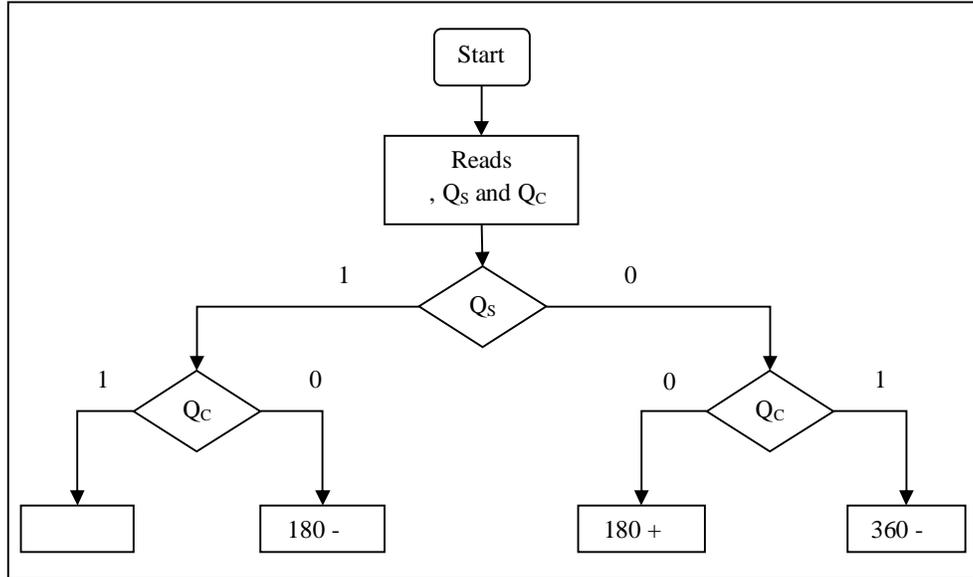


Figure 3.4: Flowchart of the absolute angle estimator block. The absolute angle is determined based on sine quadrant bit (Q_s) and cosine quadrant bit (Q_c).

The computation of rotor shaft angle based on the proposed methodology is described in the following way. Let us consider the rotor shaft is stationary at 135° , then the scott-T outputs becomes

$$V_s = [0.707] V \sin \omega t$$

$$V_c = [-0.707] V \sin \omega t$$

The sine and cosine demodulator outputs are given by

$$U_s = 0.707V$$

$$U_c = 0.707V$$

Applying inverse tangent operation, $\theta = \arctan (0.707V/0.707V) = 45^\circ$

Since rotor shaft is in II quadrant and according to concept of the quadrant detector, the absolute shaft angle can be obtained by subtracting θ from 180° .

Hence rotor shaft angle = $180^0 - 45^0 = 135^0$. From the table 3.1 it is observed that, the logical value of Q_s is changing from logic 0 to logic 1 whenever the rotor shaft completes 360^0 rotation. In otherwords, a complete cycle of Q_s corresponds to 360^0 rotation of shaft; hence the number of cycles of Q_s per one minute of time is called as revolutions per minute (rpm). Figure 3.5 illustrates nature of Q_s for multiple rotations of rotor shaft. Therefore Q_s can be considered as the speed signal to estimate the speed of rotation of rotor shaft.

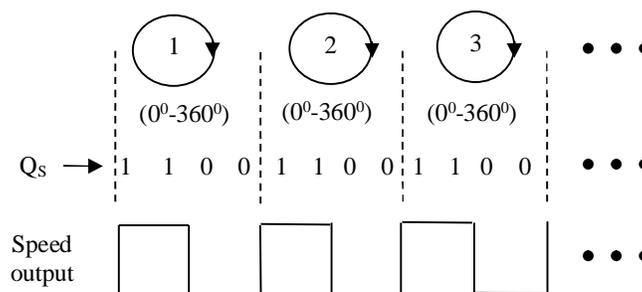


Figure 3.5: Transitions of sine quadrant bit Q_s for multiple rotations of rotor shaft

3.3 Simulation results

The simulation blocks of synchro and the proposed SDC are shown in figure 3.6. The synchro block is modeled using the mathematical expressions obtained in section 3.1. Considering a sinusoidal signal with amplitude of 10 V and frequency of 50 Hz is used to excite the synchro and the model simulated at rotor shaft speed of 10 rpm.

The transformation ratio between stator and rotor windings of the synchro is assumed to be unity. As a result, the stator signals from the synchro have maximum amplitude of 10 V and the signals simulated signals are shown in figure 3.7. These signals are called as phase voltage signals and are denoted as V_{S1} , V_{S2} and V_{S3} .

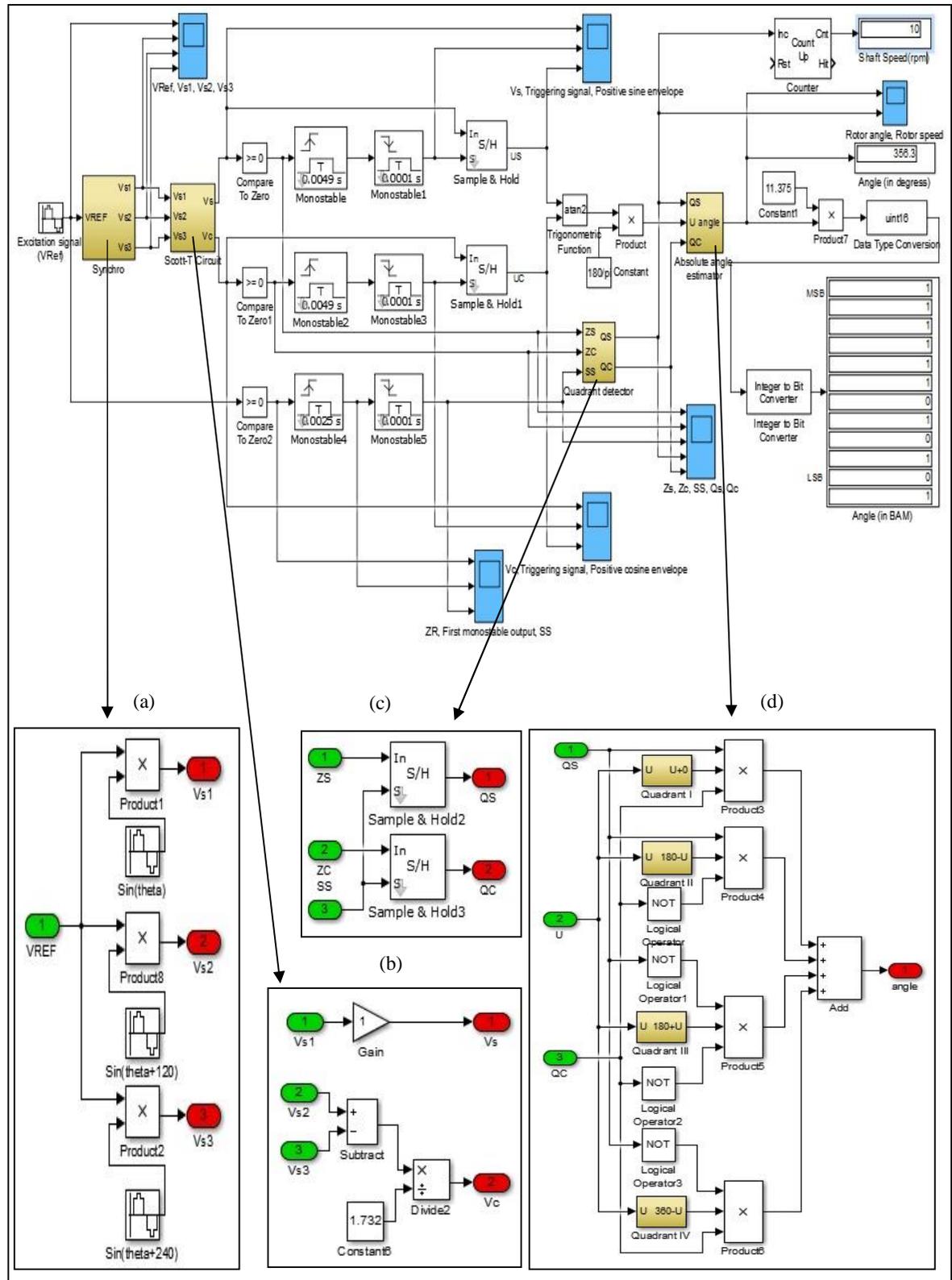


Figure 3.6: MATLAB/Simulink model of Synchro-to-Digital Converter system. (a) synchro (b) scott-T circuit (c) quadrant detector (d) absolute angle estimator.

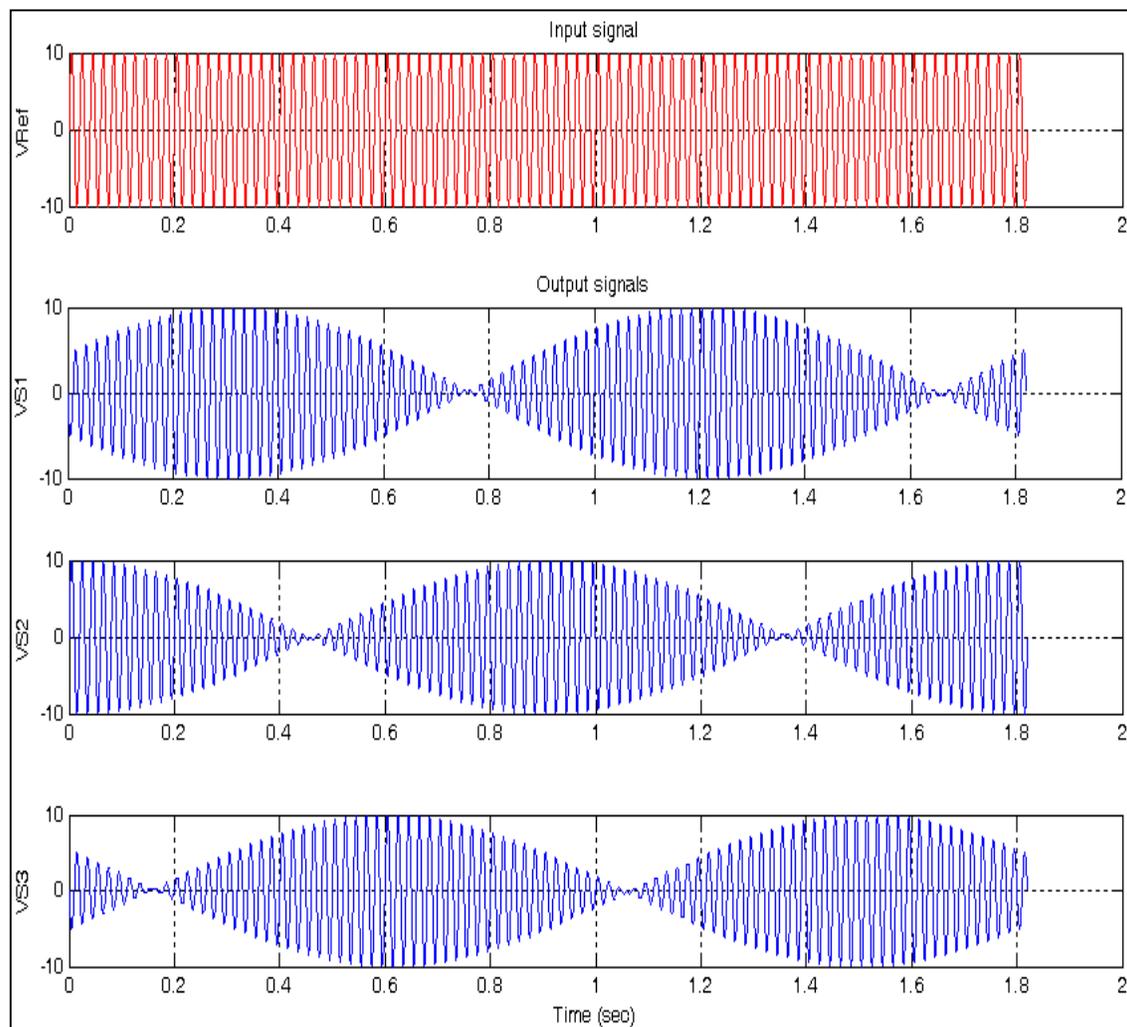


Figure 3.7: Synchro input: V_{Ref} and output signals: V_{S1} , V_{S2} and V_{S3}

The SDC model consists of scott-T circuit, comparators, monoshot circuits, S&H circuits, quadrant detector and an absolute angle estimator. The output signals obtained by the synchro are demodulated by SDC to compute the rotor shaft angle and its speed of rotation. The synchro outputs are connected to the scott-T circuit of SDC. The scott-T circuit responsible for generation of the line voltages (V_{S3-S1} , V_{S2-S3} , V_{S1-S2}) and followed by conversion operation. Based on the simplification in Appendix A, the line voltage signals converted into two equivalent signals using the basic library blocks. The output signals obtained by the scott-T circuit are denoted as V_s , V_c and are shown in figure 3.8.

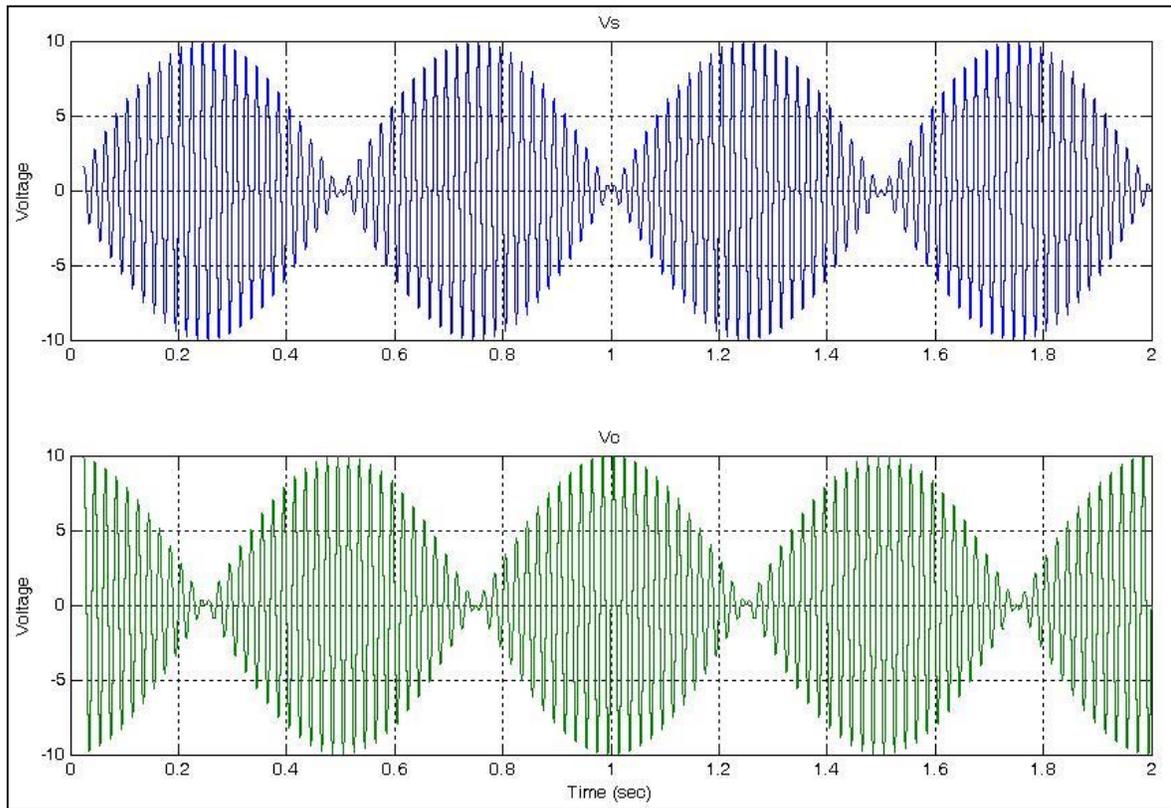
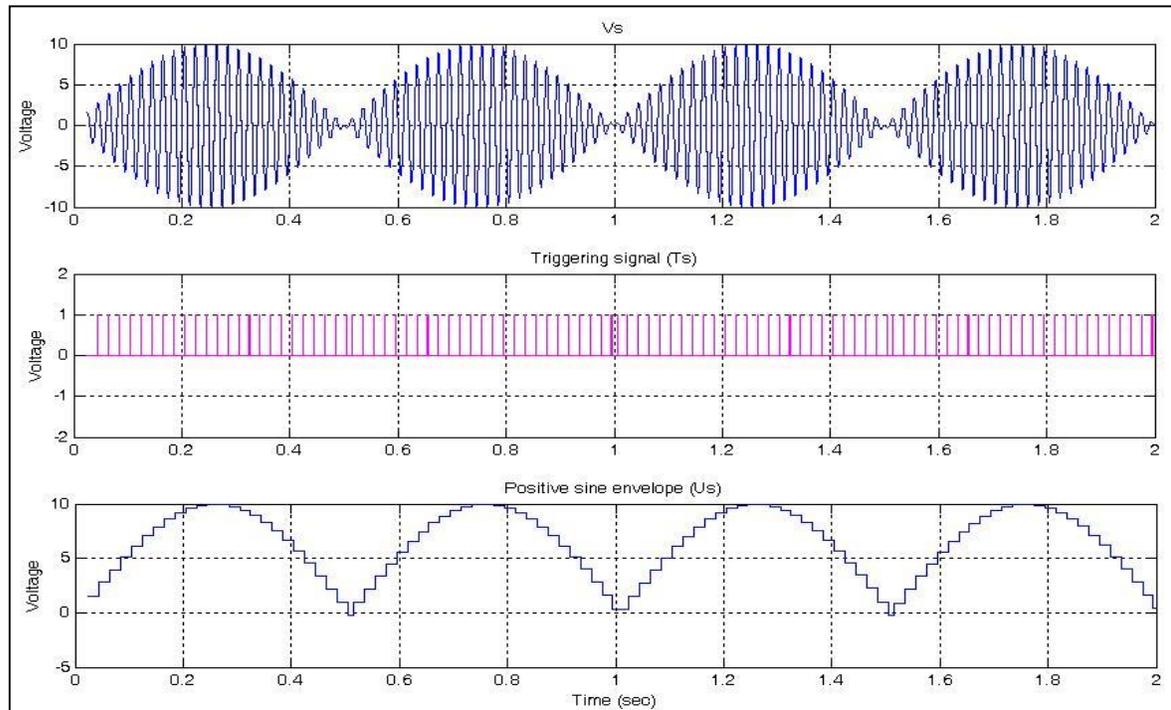
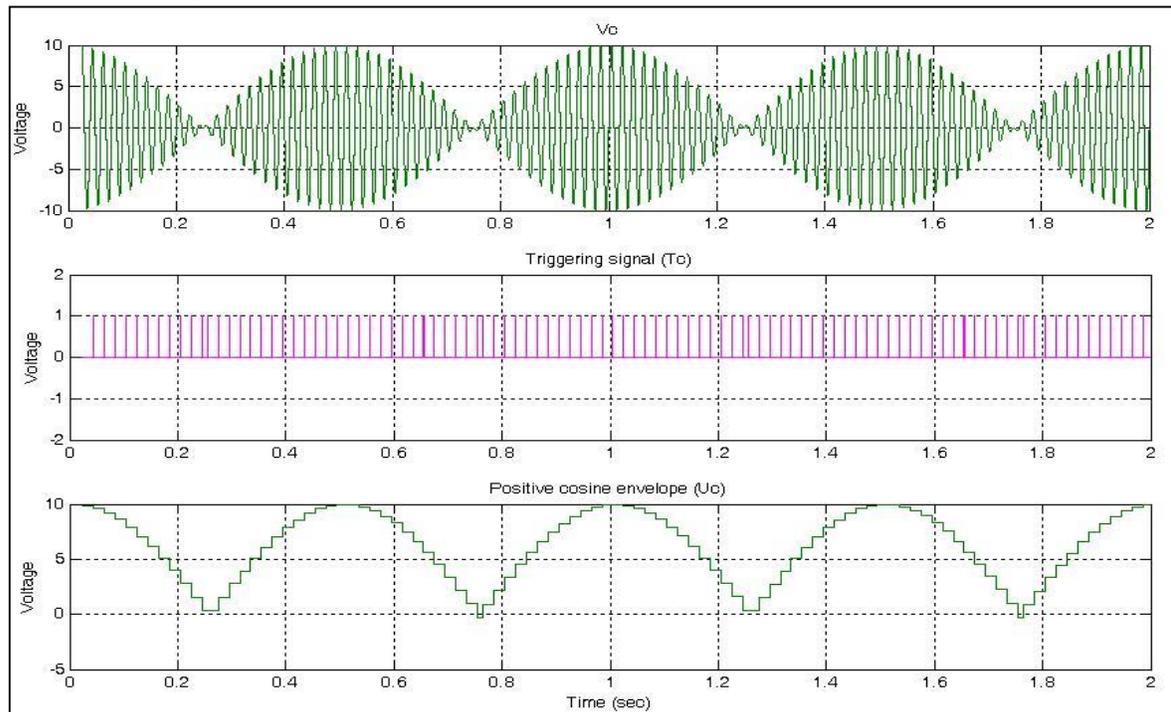


Figure 3.8: Scott-T circuit output signals: V_S and V_C .

The scott-T output signals (V_S , V_C) are sent to two separate demodulators to extract positive sine and cosine envelopes. This is achieved by triggering the scott-T outputs at peak amplitude levels. So the detection of these levels plays an important role in computation of the rotor shaft angle. The operation of demodulator using dual stage monoshot and S&H circuit is explained in section 3.2. Since the scott-T outputs V_S and V_C have the time period of 20 ms, the peak amplitudes occurs at 5 ms. The dual stage monoshot provides a triggering signal at 5 ms in every cycle of V_S . This is achieved by programming first monoshot for the rising edge of the zero crossing output of V_S and has to generate a pulse of duration 4.9 ms. Then the second monoshot is programmed for the falling edge of first monoshot output and generates a pulse of duration 0.1 ms. The S&H block takes V_S and triggering signal as inputs and holds the peak amplitudes whenever it receives a triggering input. In this way the S&H block outputs peak amplitude levels of V_S and these instantaneous



(a) Positive sine envelope detection of V_s . The pulses of the triggering signal, T_s are occurring at positive peak amplitudes of V_s .



(b) Positive cosine envelope detection of V_c . The pulses of the triggering signal, T_c are occurring at positive peak amplitudes of V_c .

Figure 3.9: Demodulation of scott-T signals using triggering signals.

levels are called as positive sine envelope. Similarly the positive cosine envelope also extracted. The process of extraction of positive sine envelope and cosine envelope is called as demodulation. This process is shown in figure 3.9. These instantaneous envelope values are given to atan2 block. The absolute shaft angle is calculated based on the bits provided by quadrant detector.

The quadrant detector block inputs are Sampling Signal (SS), zero crossing signals of V_S and V_C and the outputs are quadrant bits Q_S and Q_C . Quadrant detector block outputs the level of inputs based on the rising edge of sampling signal. The sampling signal for the quadrant detector is derived such a way that a pulse is generated in each positive half cycle of zero crossing signal of V_{Ref} . The required sampling signal is generated using the dual stage monoshot and is shown in figure 3.10.

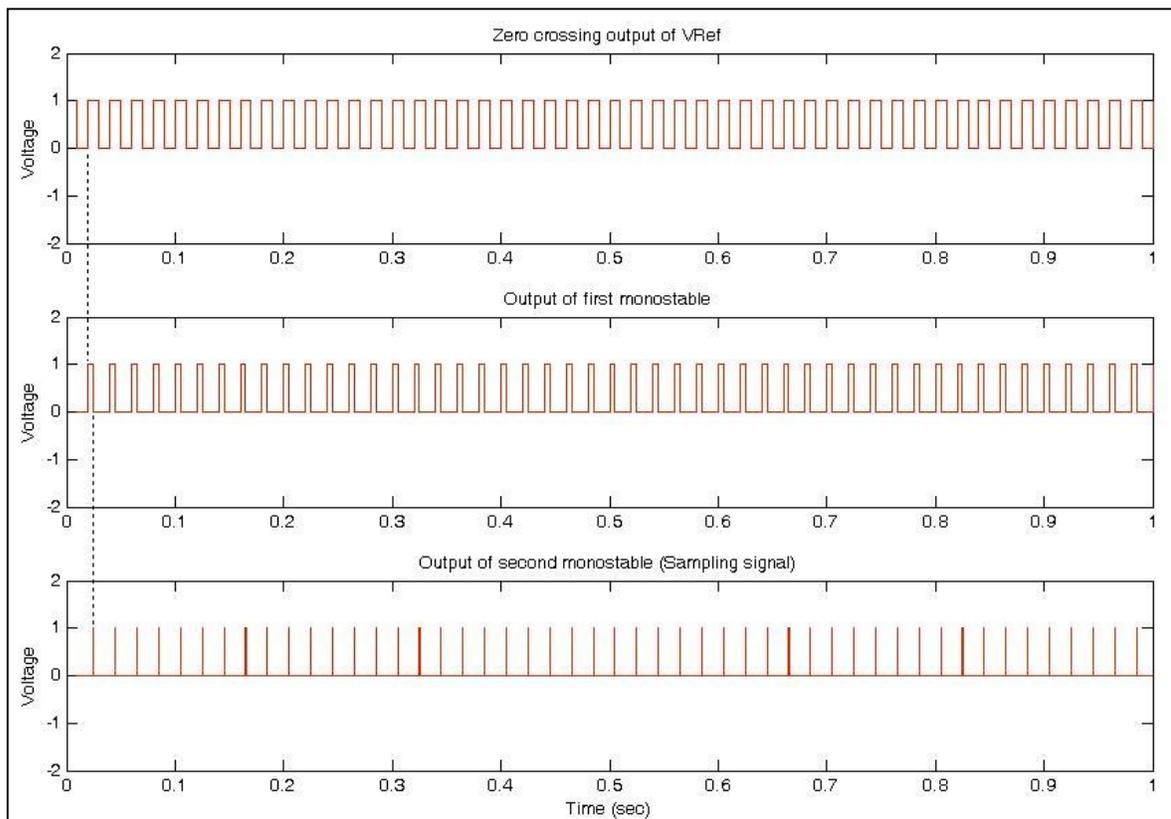


Figure 3.10: Dual stage monoshot generation of sampling signal. The first monoshot is sensitive to rising edge of V_{Ref} and the second monoshot is sensitive to falling edge of first monoshot output. Thereby, the sampling signal is occurring at every 5 ms of V_{Ref} .

Figure 3.11 illustrates the results of quadrant detector when the synchro shaft rotating at 60 rpm i.e, 1 rps. The quadrant detector outputs are either high or low based on the quadrant. It is noted that the Q_S , Q_C bits are high in I quadrant; Q_S is high and Q_C bit is low in II quadrant; Q_S , Q_C bits are low in III quadrant; Q_S bit is low and Q_C bit is high in IV quadrant.

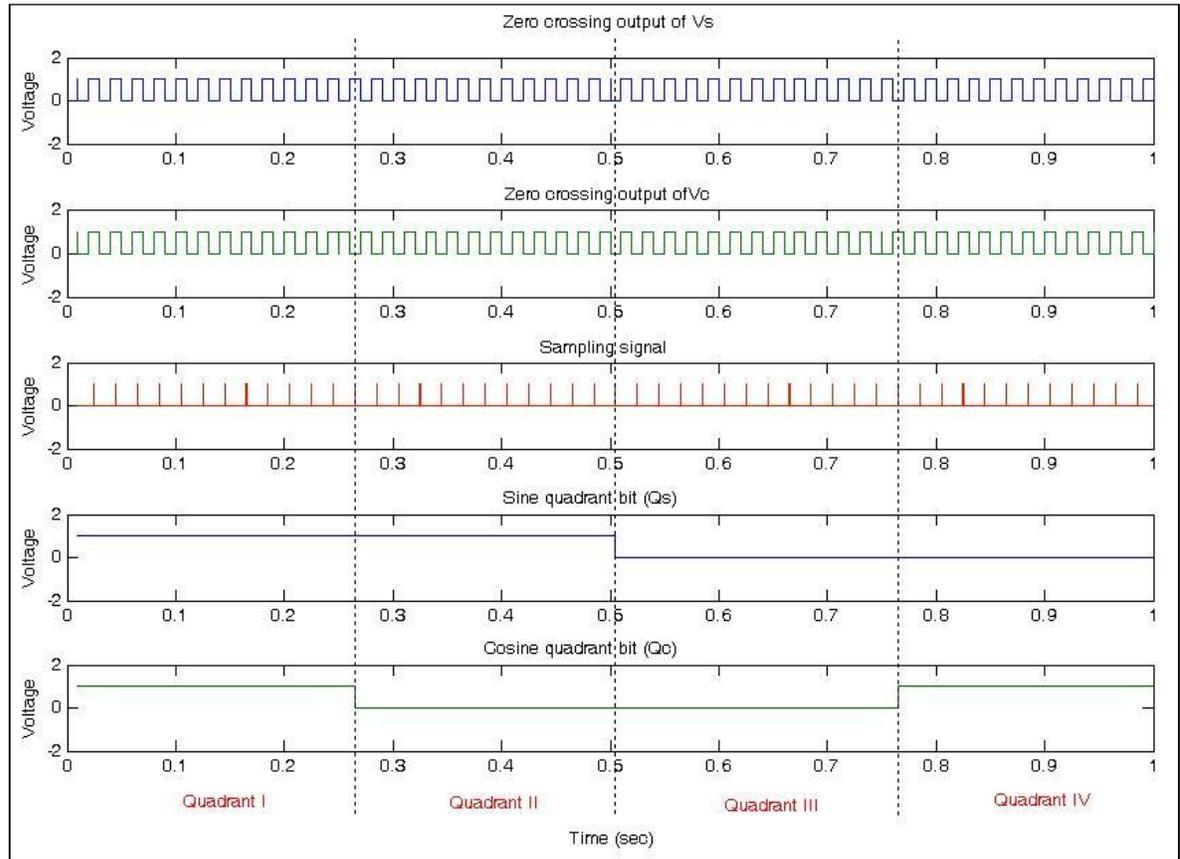
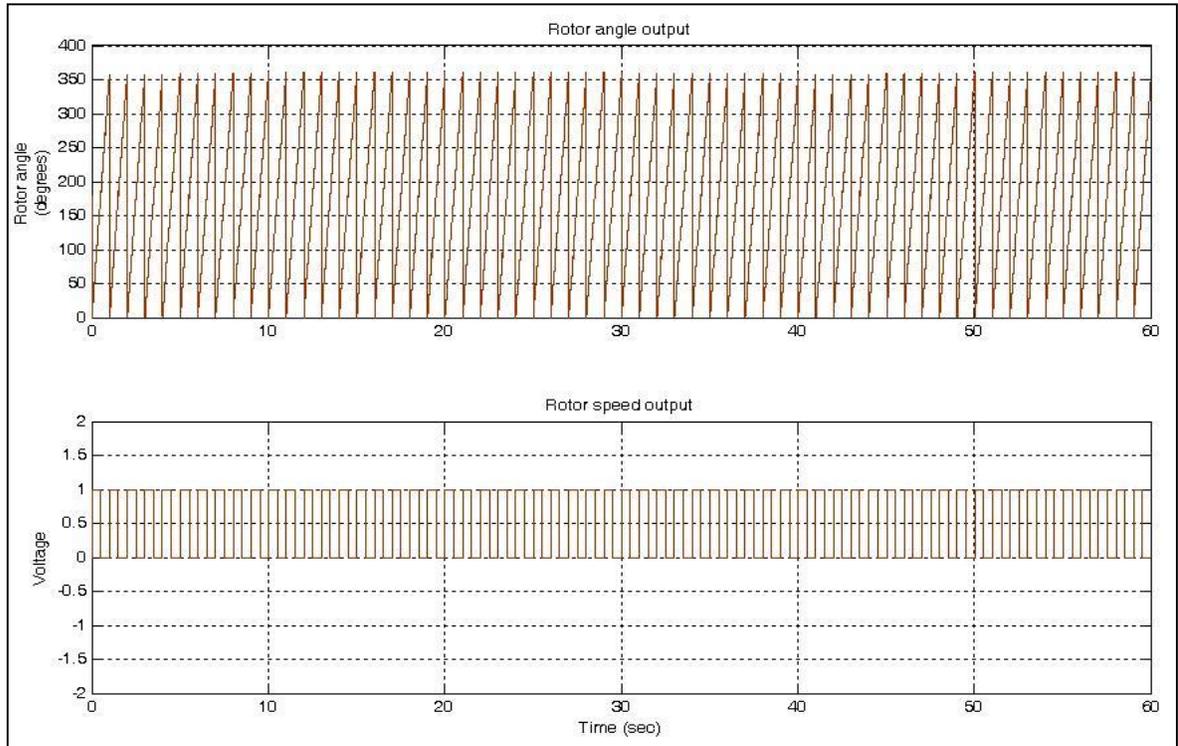
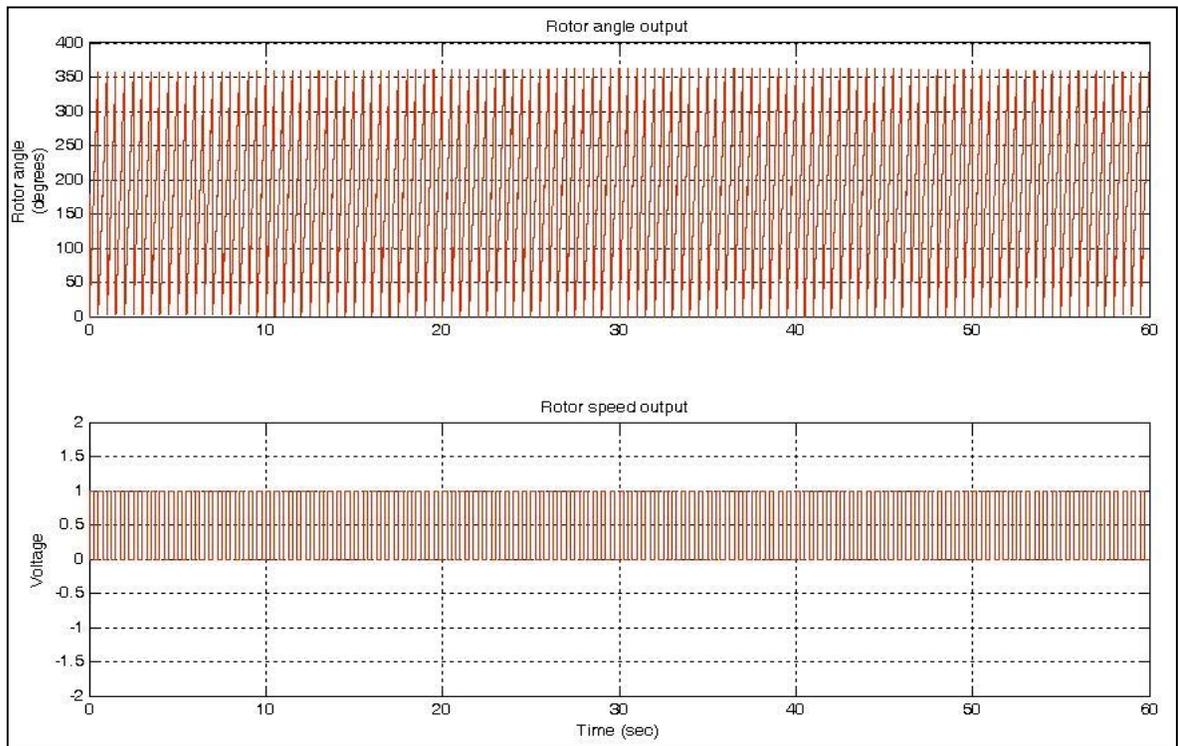


Figure 3.11: Quadrant detector inputs are V_s , V_c , sampling signal and outputs are Q_S , Q_C . The sine quadrant bit, Q_S is ± 1 in quadrant I and II; ∓ 1 in quadrant III and IV. The cosine quadrant bit, Q_C is ± 1 in quadrant I and IV; ∓ 1 in quadrant II and III.

The quadrant detector block gives quadrant in which the rotor shaft angle falls using Q_S and Q_C bits. The outputs of atan2 block and quadrant bits (Q_S , Q_C) are sent to the angle estimator. Based on table 3.1 the angle estimator gives the absolute shaft angle. Furthermore, the rate computation for shaft rotation can be done by using sine quadrant bit Q_S . The SDC model simulated and verified for various shaft speeds. The speed outputs at 60 rpm and 120 rpm are shown in figure 3.12.



(a) The output profiles of angle and speed of rotor when shaft is rotating at 60 rpm.



(b) The output profiles of angle and speed of rotor when shaft is rotating at 120 rpm.

Figure 3.12: Rotor positional angle and speed output waveforms.

3.4 Study of non-ideal characteristics

Practical synchro is not perfect and suffers with non-ideal characteristics. Therefore, synchro outputs deviates considerably from the ideal behavior. The common non-ideal characteristics are amplitude imbalance, imperfect quadrature, reference signal phase shift and excitation signal distortion.

The above characteristics cause severe inaccuracy at converters output in position measurement applications. It is therefore important to study the effect of these characteristics on the converters. The flow of computation of shaft angle measurement is shown in figure 3.13. This diagram is used to study the effects of non-ideal characteristics on SDC.

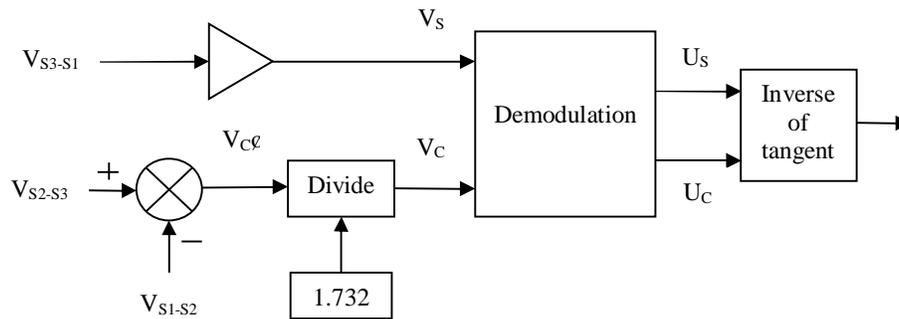


Figure 3.13: Computation flow diagram to estimate the shaft angle between $0^\circ - 90^\circ$. The line voltages V_{S3-S1} , V_{S2-S3} and V_{S1-S2} are considered to the study of non-ideal characteristics of synchro.

3.4.1 Amplitude imbalance

Amplitude imbalance refers to the occurrence of amplitude difference between the stator signals of the synchro. Amplitude imbalance occurs either from unbalanced excitation of the synchro or from the existence of unequal inductances in the phases and it is represented as

$$V_{S3-S1} = (1 + \alpha_1) V \sin \sin t \quad (3.15)$$

$$V_{S2-S3} = (1 + \alpha_2) V \sin(+120^\circ) \sin t \quad (3.16)$$

$$V_{S1-S2} = (1 + \alpha_3) V \sin(+240^\circ) \sin t \quad (3.17)$$

where α_1 , α_2 and α_3 represents the amount of amplitude imbalances.

From equation (3.15), it can be noticed that the voltage between S3 to S1 directly gives V_s

$$V_S = (1 + \epsilon_1) V \sin \omega t$$

Consider (3.16) & (3.17)

$$\begin{aligned} V_C \phi &= V \sin \omega t [(1 + \epsilon_2) \sin(\omega t + 120^\circ) - (1 + \epsilon_3) \sin(\omega t + 240^\circ)] \\ &= V \sin \omega t [\sin(\omega t + 120^\circ) + \epsilon_2 \sin(\omega t + 120^\circ) - \sin(\omega t + 240^\circ) - \\ &\quad \epsilon_3 \sin(\omega t + 240^\circ)] \\ &= V \sin \omega t [-0.5 \sin \omega t + 0.866 \cos \omega t - 0.5 \epsilon_2 \sin \omega t + 0.866 \epsilon_2 \cos \omega t + \\ &\quad 0.5 \sin \omega t + 0.866 \cos \omega t + 0.5 \epsilon_3 \sin \omega t + 0.866 \epsilon_3 \cos \omega t] \\ &= V \sin \omega t [1.732 \cos \omega t + 0.5 (\epsilon_3 - \epsilon_2) \sin \omega t + 0.866 (\epsilon_2 + \epsilon_3) \cos \omega t] \end{aligned}$$

Dividing by 1.732, $V_C = V \sin \omega t [\cos \omega t + 0.288 (\epsilon_3 - \epsilon_2) \sin \omega t + 0.5 (\epsilon_2 + \epsilon_3) \cos \omega t]$

After demodulation, $U_S = (1 + \epsilon_1) V \sin \omega t$

$$U_C = V [\cos \omega t + 0.288 (\epsilon_3 - \epsilon_2) \sin \omega t + 0.5 (\epsilon_2 + \epsilon_3) \cos \omega t]$$

Applying inverse of tangent operation and the result denoted by ϕ

$$\begin{aligned} \phi &= \arctan (U_S / U_C) \\ &= \arctan ((1 + \epsilon_1) \sin \omega t / [\cos \omega t + 0.288 (\epsilon_3 - \epsilon_2) \sin \omega t + 0.5 (\epsilon_2 + \epsilon_3) \cos \omega t]) \end{aligned} \quad (3.18)$$

According to absolute angle estimation

$$\phi = \begin{cases} & \text{for I quadrant} \\ 180^\circ - & \text{for II quadrant} \\ 180^\circ + & \text{for III quadrant} \\ 360^\circ - & \text{for IV quadrant} \end{cases}$$

$$\text{Position error} = \phi - \theta$$

The amplitude imbalances were applied on synchro and corresponding affect of converter's resolutions of 10-bit, 11-bit and 12-bit are observed. The maximum angular errors for the imbalance values of $\epsilon = 0.003, 0.005, 0.015$ is given in table 3.2. Figure 3.14 shows the angular error variation for the combinations enclosed with dotted lines of table 3.2. It is noted

that, as long as the imbalance values (α_1 , α_2 , α_3) are of equal amounts, the angular error is zero. Further, it is observed that as the imbalance values are increasing the inaccuracy between actual mechanical angle and measured angle is increasing.

Table 3.2: Quantitative analysis of amplitude imbalance

Amplitude imbalance	Amplitude imbalance values			Maximum Angular error (degrees)	Resolution (approximately)
	α_1	α_2	α_3		
0.3%	0	0	0	0	12-bit
	0	0	0.003	0.074	
	0	0.003	0	0.074	
	0	0.003	0.003	0.085	
	0.003	0	0	0.085	
	0.003	0	0.003	0.074	
	0.003	0.003	0	0.074	
	0.003	0.003	0.003	0	
0.5%	0	0	0	0	11-bit
	0	0	0.005	0.123	
	0	0.005	0	0.123	
	0	0.005	0.005	0.143	
	0.005	0	0	0.143	
	0.005	0	0.005	0.123	
	0.005	0.005	0	0.123	
1.5%	0	0	0	0	10-bit
	0	0	0.015	0.37	
	0	0.015	0	0.37	
	0	0.015	0.015	0.42	
	0.015	0	0	0.42	
	0.015	0	0.015	0.36	
	0.015	0.015	0	0.36	
0.015	0.015	0.015	0		

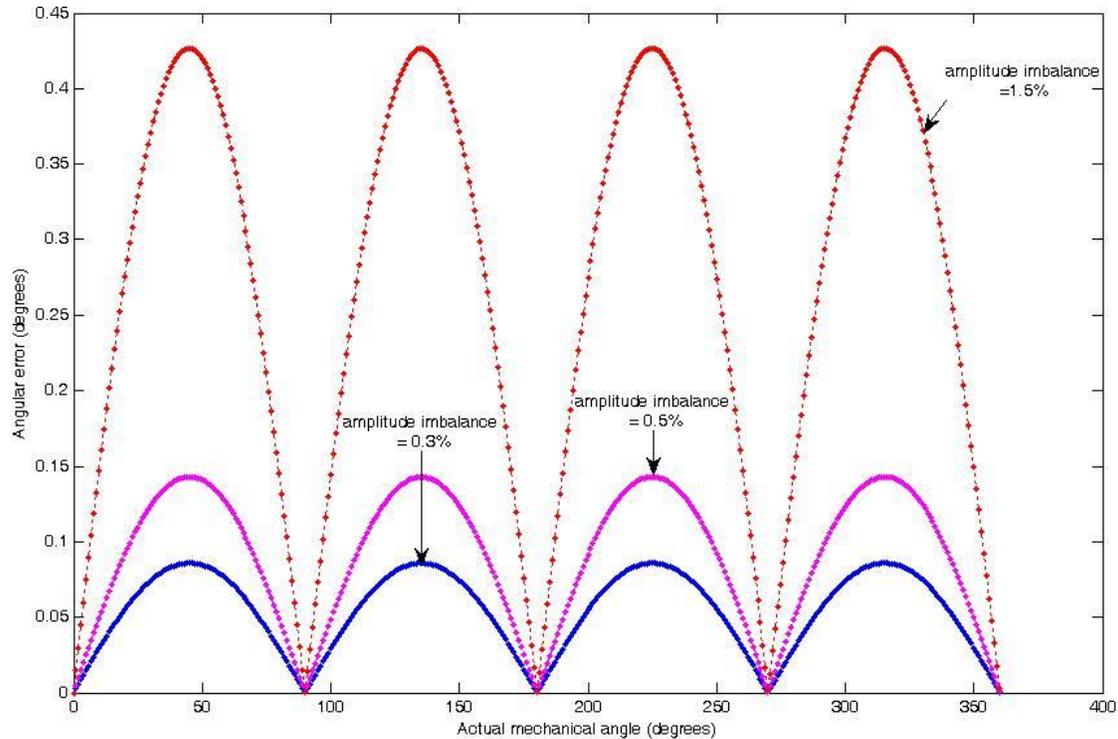


Figure 3.14: Plot of actual mechanical angle of synchro versus angular error of the converter for amplitude imbalance of 0.3%, 0.5% and 1.5%.

3.4.2 Imperfect quadrature

Imperfect quadrature occurs due to a spacial misalignment between the synchro phases. That is when the three inductance profiles of synchro are not exactly 120° phase with one another.

Then the synchro signals are represented as

$$V_{S3-S1} = V \sin(\theta + \alpha_1) \sin \omega t \quad (3.19)$$

$$V_{S2-S3} = V \sin(\theta + 120^\circ + \alpha_2) \sin \omega t \quad (3.20)$$

$$V_{S1-S2} = V \sin(\theta + 240^\circ + \alpha_3) \sin \omega t \quad (3.21)$$

where α_1 , α_2 and α_3 represents the amount of imperfect quadrature.

Consider (3.20) \ominus (3.21)

$$\begin{aligned} V_C \phi &= V \sin \omega t [\sin(\theta + \alpha_2 + 120^\circ) - \sin(\theta + \alpha_3 + 240^\circ)] \\ &= V \sin \omega t [\sin(\theta + \alpha_2) \cos 120^\circ + \cos(\theta + \alpha_2) \sin 120^\circ - \\ &\quad \sin(\theta + \alpha_3) \cos(240^\circ) \ominus \cos(\theta + \alpha_3) \sin 240^\circ] \end{aligned}$$

$$= V \sin t [-0.5 \sin(\theta + \alpha_2) + 0.866 \cos(\theta + \alpha_2) + 0.5 \sin(\theta + \alpha_3) + 0.866 \cos(\theta + \alpha_3)]$$

Dividing by 1.732,

$$V_C = V \sin t [-0.288 \sin(\theta + \alpha_2) + 0.5 \cos(\theta + \alpha_2) + 0.288 \sin(\theta + \alpha_3) + 0.5 \cos(\theta + \alpha_3)]$$

After demodulation,

$$U_S = V \sin(\theta + \alpha_1)$$

$$U_C = V [-0.288 \sin(\theta + \alpha_2) + 0.5 \cos(\theta + \alpha_2) + 0.288 \sin(\theta + \alpha_3) + 0.5 \cos(\theta + \alpha_3)]$$

Applying inverse of tangent operation and the result denoted by ϕ

$$\begin{aligned} &= \arctan (U_S / U_C) \\ &= \arctan (\sin(\theta + \alpha_1) / [-0.288 \sin(\theta + \alpha_2) + 0.5 \cos(\theta + \alpha_2) + 0.288 \sin(\theta + \alpha_3) + 0.5 \cos(\theta + \alpha_3)]) \end{aligned} \quad (3.22)$$

According to absolute angle estimation

$$\phi = \begin{cases} & \text{for I quadrant} \\ 180^\circ - & \text{for II quadrant} \\ 180^\circ + & \text{for III quadrant} \\ 360^\circ - & \text{for IV quadrant} \end{cases}$$

$$\text{Position error} = -\phi$$

The imperfect quadratures were applied on synchro and corresponding affect of converter's resolutions of 10-bit, 11-bit and 12-bit are observed. The maximum angular errors for the imperfect values of $\alpha = 0.09^\circ, 0.18^\circ, 0.36^\circ$ is given in table 3.3. Figure 3.15 shows the angular error variation for the combinations enclosed with dotted lines of table 3.3. It is noted that, as long as the imperfect values ($\alpha_1, \alpha_2, \alpha_3$) are of equal amounts, the angular error is zero.

Further, it is observed that as the imperfect values are increasing the inaccuracy between actual mechanical angle and measured angle is increasing.

Table 3.3: Quantitative analysis of imperfect quadrature

Imperfect quadrature (degrees)	Imperfect quadrature values			Maximum Angular error (degrees)	Resolution (approximately)
	β_1	β_2	β_3		
0.025% of 360=0.09	0	0	0	0	12-bit
	0	0	0.09	0.048	
	0	0.09	0	0.048	
	0	0.09	0.09	0.09	
	0.09	0	0	0.09	
	0.09	0	0.09	0.093	
	0.09	0.09	0	0.093	
	0.09	0.09	0.09	0	
0.05% of 360=0.18	0	0	0	0	11-bit
	0	0	0.18	0.096	
	0	0.18	0	0.096	
	0	0.18	0.18	0.18	
	0.18	0	0	0.18	
	0.18	0	0.18	0.186	
	0.18	0.18	0	0.187	
	0.18	0.18	0.18	0	
0.1% of 360=0.36	0	0	0	0	10-bit
	0	0	0.36	0.193	
	0	0.36	0	0.193	
	0	0.36	0.36	0.36	
	0.36	0	0	0.36	
	0.36	0	0.36	0.373	
	0.36	0.36	0	0.374	
	0.36	0.36	0.36	0	

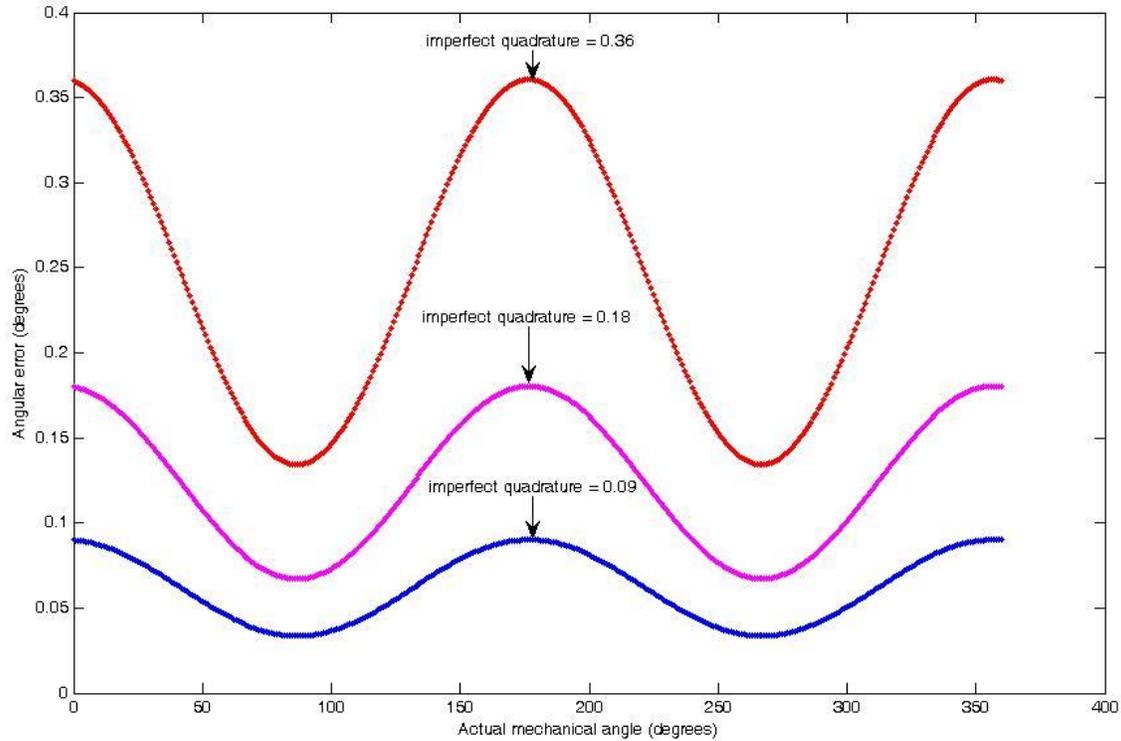


Figure 3.15: Plot of actual mechanical angle of synchro versus angular error of the converter for imperfect quadrature of 0.09° , 0.18° and 0.36° .

3.4.3 Reference signal phase shift

The resistance of the synchro excitation windings causes a phase shift between the synchro outputs and excitation signal. The reference signal phase shift in synchro outputs is represented as

$$V_{S3-S1} = V \sin(\omega t + \phi) \quad (3.23)$$

$$V_{S2-S3} = V \sin(\omega t + 120^\circ + \phi) \quad (3.24)$$

$$V_{S1-S2} = V \sin(\omega t + 240^\circ + \phi) \quad (3.25)$$

where ϕ is the phase shift between input and output signals of synchro.

From equation (3.23),

$$V_{S3-S1} = V \sin(\omega t + \phi) [\sin \omega t \cos \phi + \cos \omega t \sin \phi]$$

Consider (3.24) & (3.25)

$$V_C \phi = V \sin(\omega t + \phi) [\sin(\omega t + 120^\circ) - \sin(\omega t + 240^\circ)]$$

$$\begin{aligned}
 &= V \sin(\omega t + \theta) [1.732 \cos \Phi] \\
 &= 1.732 V (\sin \omega t \cos \Phi \cos \theta + \cos \omega t \sin \Phi \cos \theta)
 \end{aligned}$$

Dividing by 1.732,

$$V_C = V \sin \omega t \cos \Phi \cos \theta + V \cos \omega t \sin \Phi \cos \theta$$

After demodulation,

$$U_S = \sqrt{2} V \cos \Phi \sin \theta \sqrt{2} + \sqrt{2} V \sin \Phi \sin \theta \sqrt{2}$$

$$U_C = \sqrt{2} (V \cos \Phi \cos \theta) \sqrt{2} + (V \sin \Phi \cos \theta) \sqrt{2}$$

Applying inverse of tangent operation and the result denoted by ϕ

$$\begin{aligned}
 &= \arctan (U_S / U_C) \\
 &= \arctan \left(\frac{\sqrt{2} \sqrt{2} \cos \Phi \sin \theta \sqrt{2} + \sqrt{2} \sin \Phi \sin \theta \sqrt{2}}{\sqrt{2} (\cos \Phi \cos \theta) \sqrt{2} + (V \sin \Phi \cos \theta) \sqrt{2}} \right) \\
 &= \arctan (\sin \theta / \cos \theta) \\
 &= \theta
 \end{aligned} \tag{3.26}$$

According to absolute angle estimation

$$\phi = \begin{cases} \theta & \text{for I quadrant} \\ 180^\circ - \theta & \text{for II quadrant} \\ 180^\circ + \theta & \text{for III quadrant} \\ 360^\circ - \theta & \text{for IV quadrant} \end{cases}$$

$$\text{Position error} = \theta - \phi$$

From equation (3.26), it is evident that the computation of shaft angle measurement is independent of various phase shifts in reference signal. Hence, this method offers the robustness to the reference signal phase shift of the synchro.

3.4.4 Excitation signal distortion

Ideally the excitation signal is sinusoidal and does not contain any additional harmonics. In general, the excitation signal does contain harmonics and the synchro outputs represented as

$$V_{S3-S1} = \sin \sum_{n=1}^{\infty} V_n \sin(n \omega t) \tag{3.27}$$

$$V_{S2-S3} = \sin(+120^\circ) \sum_{n=1}^{\infty} V_n \sin(n \ t) \quad (3.28)$$

$$V_{S1-S2} = \sin(+240^\circ) \sum_{n=1}^{\infty} V_n \sin(n \ t) \quad (3.29)$$

Consider (3.28) ó (3.29)

$$\begin{aligned} V_C \phi &= \sum_{n=1}^{\infty} V_n \sin(n \ t) [\sin(+120^\circ) - \sin(+240^\circ)] \\ &= \sum_{n=1}^{\infty} V_n \sin(n \ t) [1.732 \cos \] \end{aligned}$$

Dividing by 1.732,

$$V_C = \sum_{n=1}^{\infty} V_n \sin(n \ t) \cos$$

After demodulation,

$$U_S = \sum_{n=1}^{\infty} V_n \sin$$

$$U_C = \sum_{n=1}^{\infty} V_n \cos$$

Applying inverse of tangent operation and the result denoted by ϕ

$$\begin{aligned} &= \arctan (U_S / U_C) \\ &= \arctan (\sin / \cos) \\ &= \end{aligned} \quad (3.30)$$

According to absolute angle estimation

$$\phi = \begin{cases} & \text{for I quadrant} \\ 180^\circ - & \text{for II quadrant} \\ 180^\circ + & \text{for III quadrant} \\ 360^\circ - & \text{for IV quadrant} \end{cases}$$

$$\text{Position error} = - \phi$$

From equation (3.30), it is evident that the harmonic components present in demodulation signals U_S and U_C are cancelled out ratio-metrically. Hence, this method offers the robustness to the excitation signal distortion of the synchro.

3.5 Conclusion

In this study, MATLAB/Simulink based modeling and simulation of both synchro and SDC is presented. The realization of present converter needs simple electronic components like comparators, dual stage monoshots, S&H circuits, and some user defined blocks. The user defined blocks: scott-T, quadrant detector and absolute angle estimator are also uses basic components like adder, subtractor and logical inverter gates. Hence, it is a cost-effective converter for motor shaft angular position and speed measurement. The utilization of sine quadrant bit of quadrant detector for rotor shaft speed estimation shows the novelty of this work. The effects of the non-ideal characteristics of synchro such as amplitude imbalance, imperfect quadrature, reference signal phase shift and excitation signal distortion are studied using the Simulink model of SDC. In the process of demodulation, the monoshot employs a resistor and capacitor as external components to generate sampling signal for S&H circuit. It is difficult to generate sampling pulses exactly at peak amplitude instances due to temperature variations and drifts in resistance. Hence, an approach is introduced in next chapter which eliminates analog component in extraction of peak amplitude levels of scott-T signals.

References

- [1] D.C. Hanselman, "Techniques for improving resolver-to-digital conversion accuracy," IEEE Transactions on Industrial Electronics, Vol.38, No.6, pp. 501-504, 1991.
- [2] Yan Liu, Zegang Ye, "Study on harmonic analysis and error correction in synchro to digital conversion," Advanced Materials Research, Vols. 225- 226, pp. 334-337, 2011.
- [3] Philip A. Laplante, "Real Time Systems Design and Analysis," Wiley-India edition, New Delhi, 2005.
- [4] Jain, "Modeling & Simulation using MATLAB & Simulink," Wiley-India edition, New Delhi, 2011.

CHAPTER 4

SYNCHRO-TO-DIGITAL CONVERTER USING DIGITAL PEAK DETECTION APPROACH

CONTENTS:

4.1 Methodology

4.2 Simulation

4.3 Conclusion

References

This chapter describes the design of Synchro-to-Digital Converter (SDC) using digital peak detection method. In this method, the synchro signals are demodulated using digital peak detector. The designed SDC is a combined analog and digital circuit, which gives the synchro shaft angle in a digital form. The theory of operation, circuit details, and simulation results are presented as follows.

4.1 Methodology

The rotor winding of synchro is supplied with a sinusoidal carrier signal and is given as

$$V_{\text{Ref}}(t) = V_{\text{REF1-REF2}}(t) = V \sin(\omega t) \quad (4.1)$$

where V is the peak amplitude, ω is the frequency of the excitation signal to the rotor.

Then the magnetically induced signals on three stator windings of the synchro are given as

$$\left. \begin{aligned} V_{S3-S1}(t, \theta) &= V \sin \omega t \sin(\theta) \\ V_{S2-S3}(t, \theta) &= V \sin \omega t \sin(\theta + 120^\circ) \\ V_{S1-S2}(t, \theta) &= V \sin \omega t \sin(\theta + 240^\circ) \end{aligned} \right\} \quad (4.2)$$

where θ is the angular position of the synchro shaft.

is the transformation ratio between rotor and stator windings, assumed as unity.

The block diagram of the SDC based on digital peak detection is shown in figure 4.1. In this scheme, the synchro signals in three signals format is converted to two signal format using electronic scott-T circuit. The electronic scott-T simplification and the output signals evaluation is explained in Appendix A. The output signals of electronic scott-T are denoted as V_S and V_C and given by

$$\left. \begin{aligned} V_S &= V \sin(\omega t) \sin \theta \\ V_C &= V \sin(\omega t) \cos \theta \end{aligned} \right\} \quad (4.3)$$

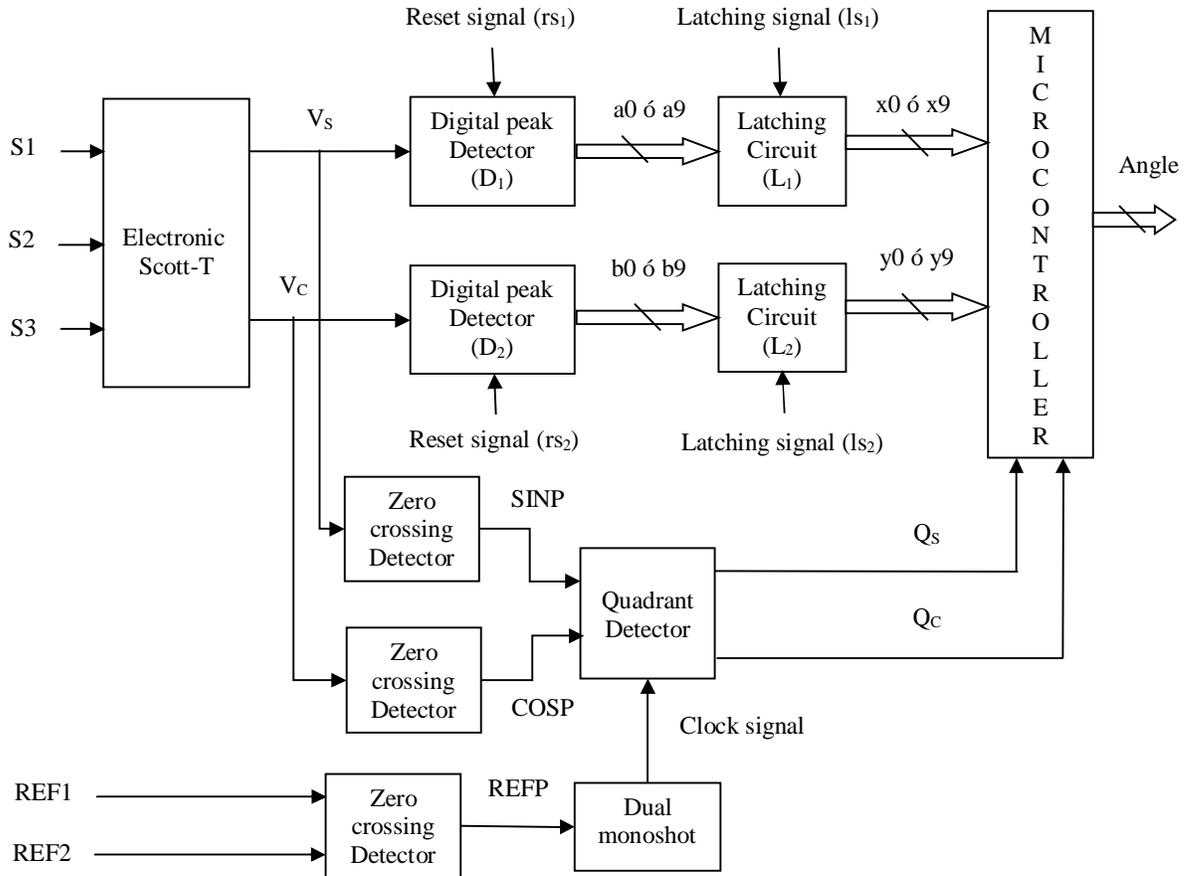


Figure 4.1: Block diagram of Synchro-to-Digital Converter using digital peak detection method. The stator terminals of synchro: S1, S2, S3 and excitation terminals: REF1, REF2 are inputs to the converter.

The output signals of scott-T circuit are applied to the corresponding digital peak detectors (D_1 and D_2). The outputs of detectors are 10-bit digital data which corresponds to peak values of V_s and V_c . The peak amplitudes $V \sin\theta$, $V \cos\theta$ converted to digital value and are fed to a microcontroller via latching circuits (L_1 and L_2). The quadrant detector determines the quadrant in which the shaft angle falls.

The following subsections describe a method of digital peak detection logic for demodulation, generation of latching & reset signals for updating the contents of latching circuits, flip flops based quadrant detector and arctangent implementation for synchro shaft angle.

4.1.1 Digital peak detection logic

There are two digital peak detectors D_1 and D_2 to demodulate the scott-T output signals V_S , V_C and the logic circuit for peak detection is shown in figure 4.2. As the synchro rotor angles are converted as the amplitude of V_S , V_C signals, it is required to extract peak amplitude levels to find the shaft angle. These digital peak detection circuits D_1 , D_2 give instantaneous peak amplitudes of V_S , V_C . The digital peak detection logic consists of comparator, 10-bit counter and 10-bit Digital-to-Analog Converter (DAC). The comparator enables the counter which starts counting until peak value of the input signal is reached, and it stops counting when the peak of input signal is reached. The digital outputs corresponding to the peak amplitude of inputs are fed to the latching circuits.

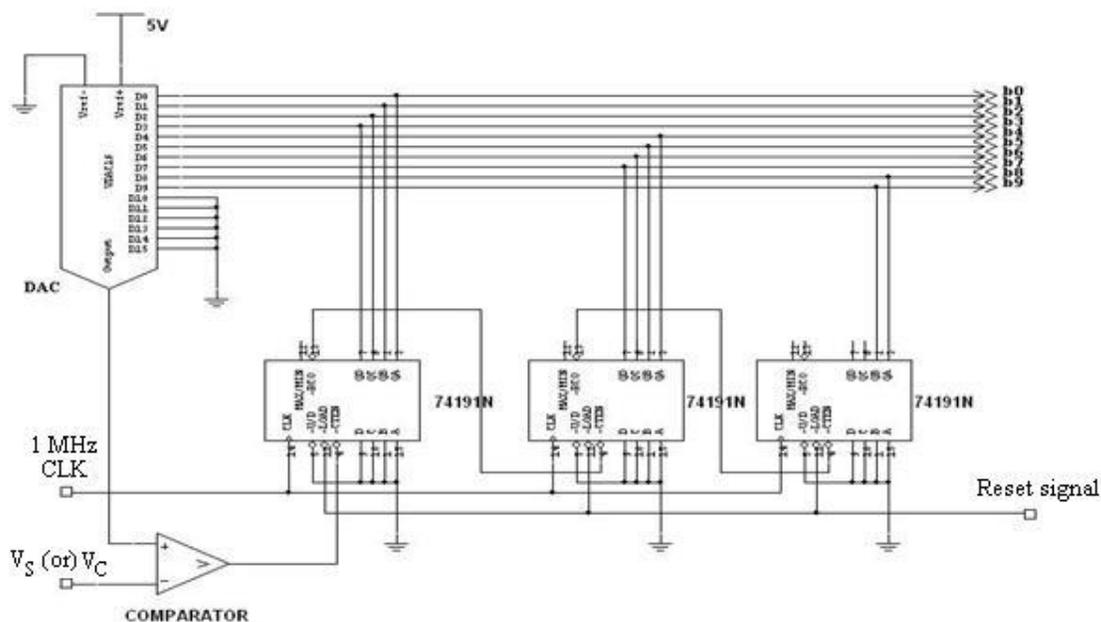


Figure 4.2: Circuit diagram for digital peak detector composed of comparator, counter and Digital-to-Analog Converter (DAC). The separate 10-bit digital data represents peak amplitude information of V_S or V_C .

4.1.2 Logic for latching, reset signal generation

The reference signal V_{Ref} for the synchro is applied to a comparator to generate zero crossing signal. Then this zero crossing signal is passed through three stages of monoshot to give

latching signal at second stage and reset signal at third stage. The three stage monoshot is shown in figure 4.3. The single monoshot is capable of generating pulses of desired width, and the basic output pulse width is determined by selection of an external resistor and a capacitor [1]. The output pulse width T_w is defined as follows,

$$T_w = K R_{ext} C_{ext} (1 + 0.7 / R_{ext}) \tag{4.4}$$

Where R_{ext} is external resistor, C_{ext} is external capacitor, $K=0.28$.

Since the reference sinusoidal signal V_{Ref} , has a time period of 20 ms, the peak occurs at 5 ms. Hence the latching signal is generated at 6 ms having duration of 3 ms to read the digital data into the microcontroller. Reset signal is generated at 9 ms having duration of 1 ms to update the digital data in each cycle of reference signals. Hence, the digital output from the counter is fed into latching circuits at 6 ms and stays for 3 ms to read into microcontroller. Then, a reset pulse of 1 ms resets the counter of digital peak detector in every cycle. The parameters which have been used for three stage monoshot to generate desired latching and reset signals are given in table 4.1.

Table 4.1: Parameters of three stage monoshot

Parameters	First monoshot	Second monoshot	Third monoshot
R_{ext}	1.7 k	4.5 k	1 k
C_{ext}	10 μ F	1 μ F	1 μ F

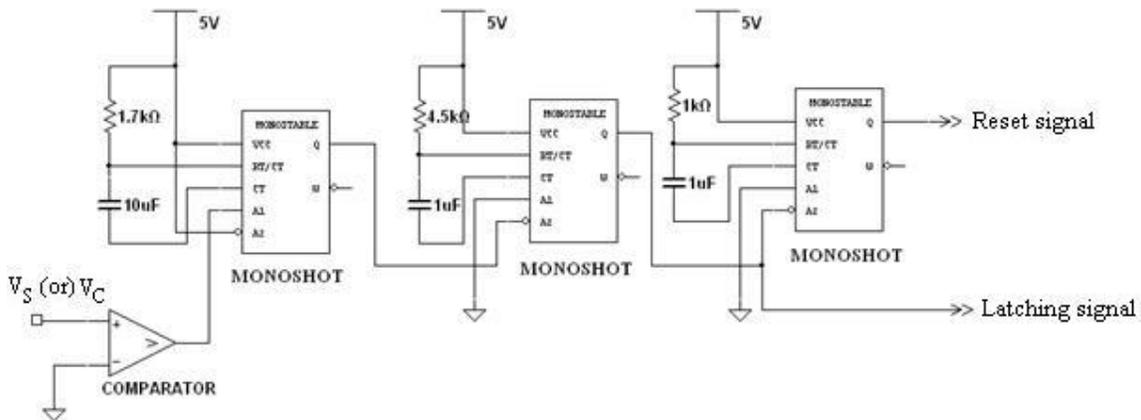


Figure 4.3: Generation of latching and reset signals using three stage monoshot. The second and third monoshot gives latching signal and reset signal respectively.

4.1.3 Quadrant determination

The evaluation of quadrant is based on graph shown in figure 4.4. It shows the variation of sine and cosine signals with respect to the reference signal. It is noticed that in I quadrant both V_S and V_C are in phase with V_{Ref} . In the II quadrant, V_S is in phase and V_C becomes out of phase with V_{Ref} . In the III quadrant both V_S and V_C are out of phase with V_{Ref} . In the IV quadrant, V_S is out of phase and V_C becomes in phase with V_{Ref} . This concept is utilized for detecting the quadrant and summarized in table 4.2.

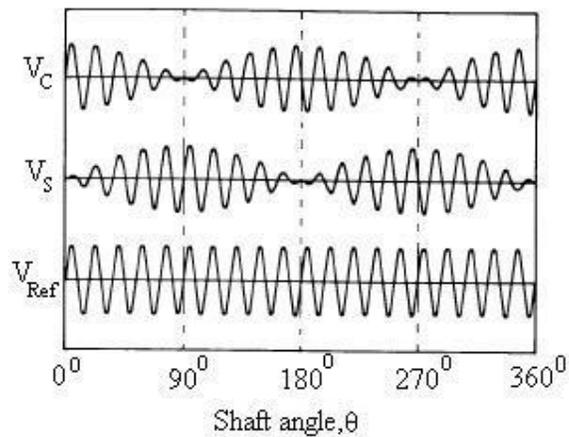


Figure 4.4: Scott-T circuit output signals, V_S and V_C along with excitation signal, V_{Ref} .

Table 4.2: Summary of quadrant determination

Quadrant			Absolute angle		
	V_{Ref} & V_S	V_{Ref} & V_C	Q_S	Q_C	(degrees)
I (0° - 90°)	in-phase	in-phase	1	1	
II (90° - 180°)	in-phase	out-phase	1	0	180° -
III (180° - 270°)	out-phase	out-phase	0	0	180° +
IV (270° - 360°)	out-phase	in-phase	0	1	360° -

Here, a new method of implementation of quadrant detector circuit, based on flip flops is introduced and shown in figure 4.5. It detects the quadrant in which the shaft is located and generates the two bits Q_S , Q_C accordingly. First the reference and scott-T signals are converted to the square waveforms with the help of comparators. The zero crossing signals of scott-T are connected to D input of the respective flip flop. A separate dual monoshot is used to generate a clock signal from reference signal, V_{Ref} .

Substituting $R_{ext} = 1.69\text{ k}\Omega$, $C_{ext} = 10\text{ }\mu\text{f}$ in equation (4.4) for the first monoshot gives a train of pulses of width 4.7 ms, obtained at every rising edge of V_{Ref} . For the second monoshot, $R_{ext} = 10\text{ k}\Omega$, $C_{ext} = 8.2\text{ nF}$ causes a train of pulses of width 0.022 ms is obtained, at every falling edge of first monoshot output. The output of second monoshot is utilized as clock signal for the flip flops. Now based on the rising edge of the clock input, flip flops determine the level of data inputs, which could be either positive or negative based on the quadrant.

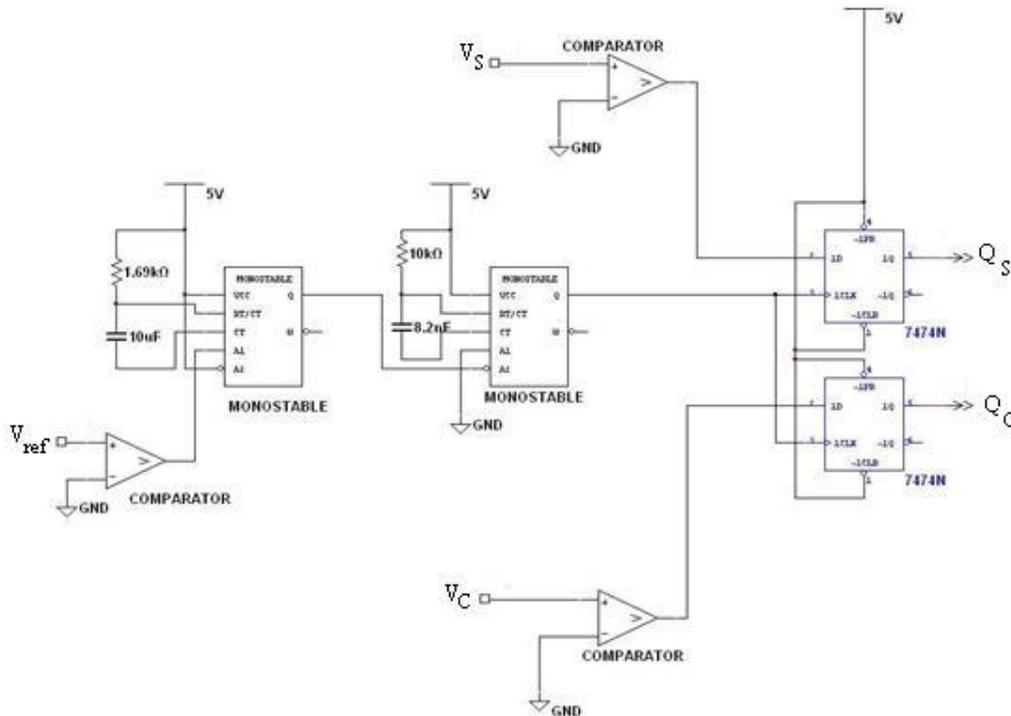


Figure 4.5: Design of quadrant detector using comparator, monoshots and flip flops. The quadrant detector outputs: Q_S and Q_C gives quadrant information of shaft.

4.1.4 Arctangent implementation

The counts of signal $\sin\theta$ and $\cos\theta$ demodulated from the carrier signal $V\sin\omega t$ along with the quadrant detector bits are fed to the AT89C51 microcontroller. The pin configuration of the AT89C51 is shown in figure 4.6 and has the following resources [2]

- 128 bytes of Random Access Memory (RAM)
- 4K bytes of on-chip Read Only Memory (ROM)
- Two timers
- One serial port
- Four 8-bit I/O ports
- Six interrupt sources

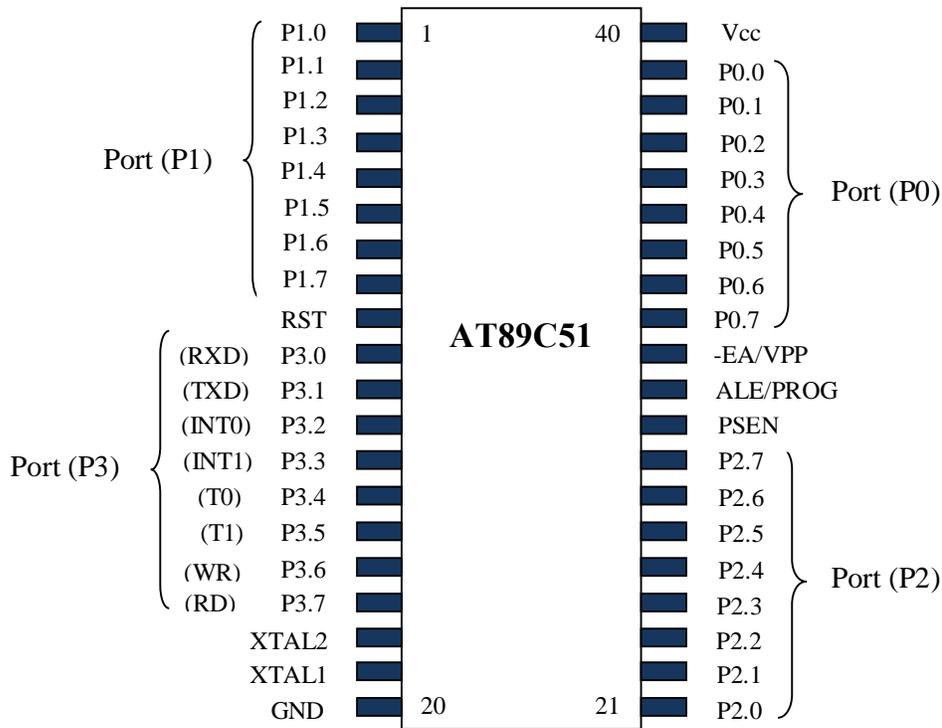


Figure 4.6: Pin configuration of the microcontroller AT89C51

A software code (shown in Appendix B) is written for the microcontroller that reads the 10-bit digital data of $\sin\theta$, $\cos\theta$ and divides the same. Then the inverse tangent function is

applied. Based on quadrant evaluated, microcontroller calculates the absolute angle as per table 4.2. The microcontroller displays the rotor angle, through an LED display.

4.2 Simulation

This scheme includes digital peak detectors, 10-bit latching circuits, microcontroller unit, latching and reset signals generation blocks and quadrant detector. To avoid electrical shock the excitation voltage V_{Ref} is stepped down from 250 V_{rms} to 24 V_{rms} . The synchro outputs V_{S1} , V_{S2} and V_{S3} supplied to the electronic scott-T to generate two equivalent signals. The generated outputs V_S , V_C along with V_{Ref} are shown in figure 4.7. The V_S , V_C outputs are connected to digital peak detectors.

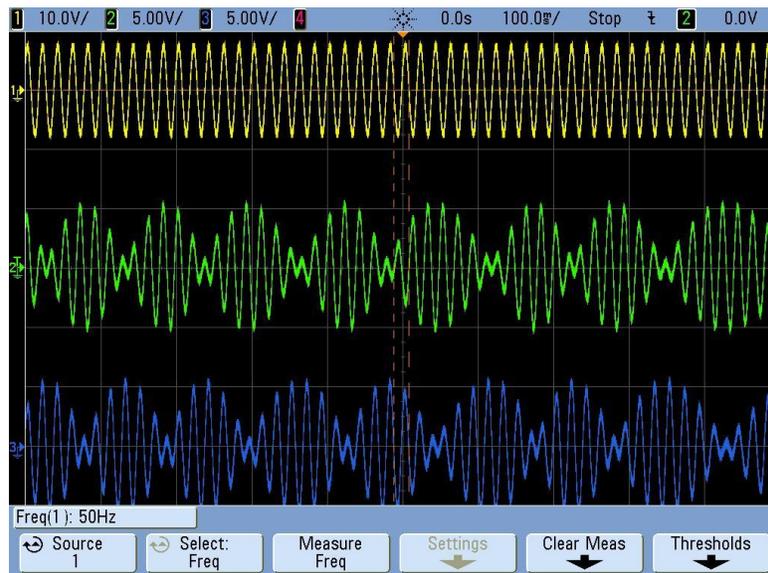


Figure 4.7: Scott δ T output signals: V_S (green) and V_C (blue) along with reference signal: V_{Ref} (yellow).

There are two sets of signals called as latching and reset signals are generated to read the digital peak information of V_S and V_C separately. The generation of latching and reset signals from zero crossing of excitation signal is shown in figure 4.8. The latching signals ls_1 and ls_2 connected to respective latching circuits L_1 and L_2 to provide microcontroller reading time of 3 ms. The reset signals rs_1 and rs_2 connected to respective digital peak detectors D_1 and D_2 to provide counter reset time of 1 ms in each cycle of scott-T outputs.

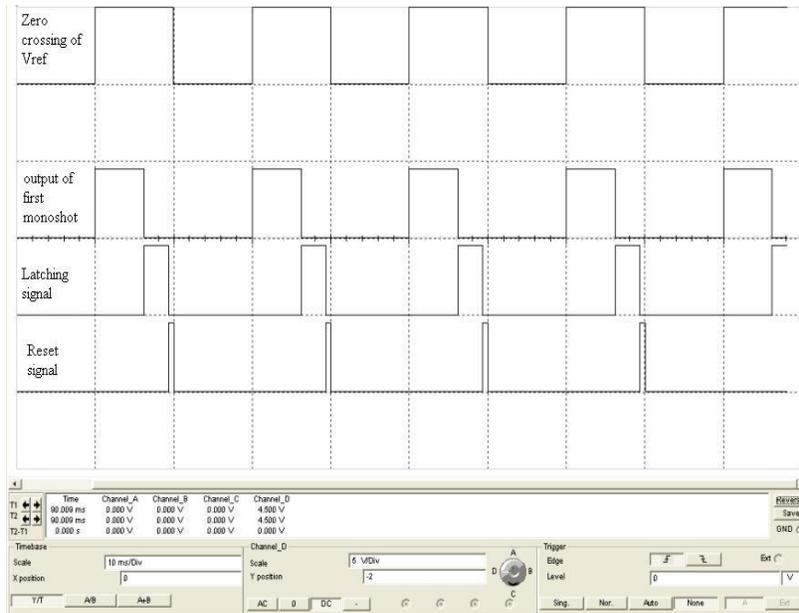
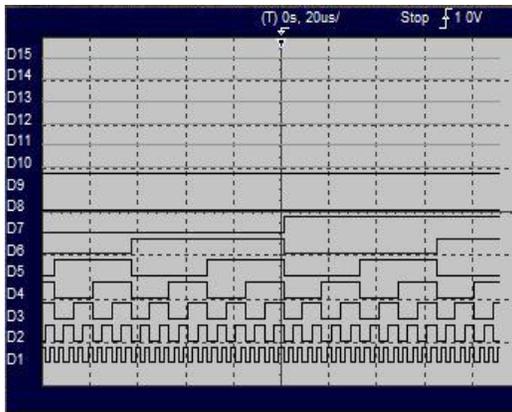
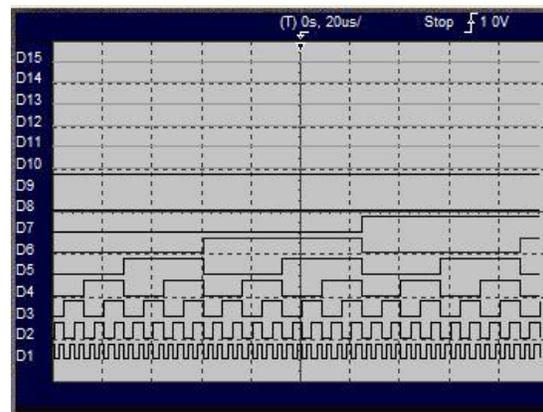


Figure 4.8: Latching signal at the falling edge of output of first monoshot and reset signal at the falling edge of latching signal.

Figure 4.9 shows the digital peak detector outputs corresponding to quadrature signals V_s , V_c . These are fed to the microcontroller for evaluation of synchro shaft angle rotation.



(a) 10-bit digital data corresponding to V_s signal



(b) 10-bit digital data corresponding to V_c signal

Figure 4.9: Digital peak detector outputs as synchro shaft is rotating.

The generation of clock signal from the excitation signal, V_{Ref} using dual monoshot is shown in figure 4.10. The zero crossing signals of V_{Ref} , V_s and V_c are represented as REFP, SINP and COSP respectively. Figure 4.11 (a)-(d) illustrates the experimental results of quadrant detector output bits Q_s , Q_c in four quadrants for a full 360° rotation of the shaft. It is observed

that Q_S , Q_C bits are high in first quadrant; Q_S bit is high and Q_C bit is low in second quadrant; Q_S , Q_C bits are low in third quadrant and Q_S bit is low and Q_C bit is high in fourth quadrant.

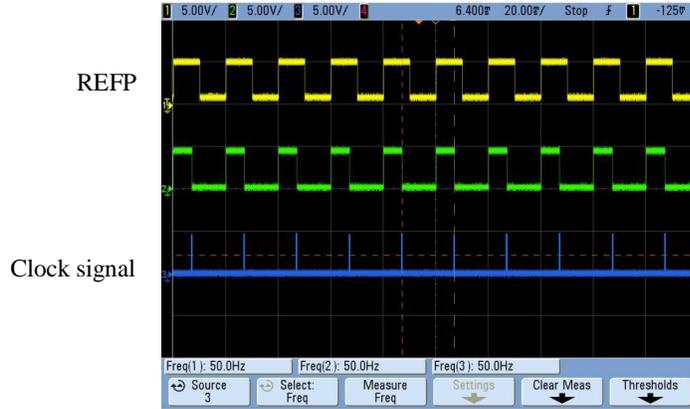


Figure 4.10: Dual stage monoshot generation of clock signal

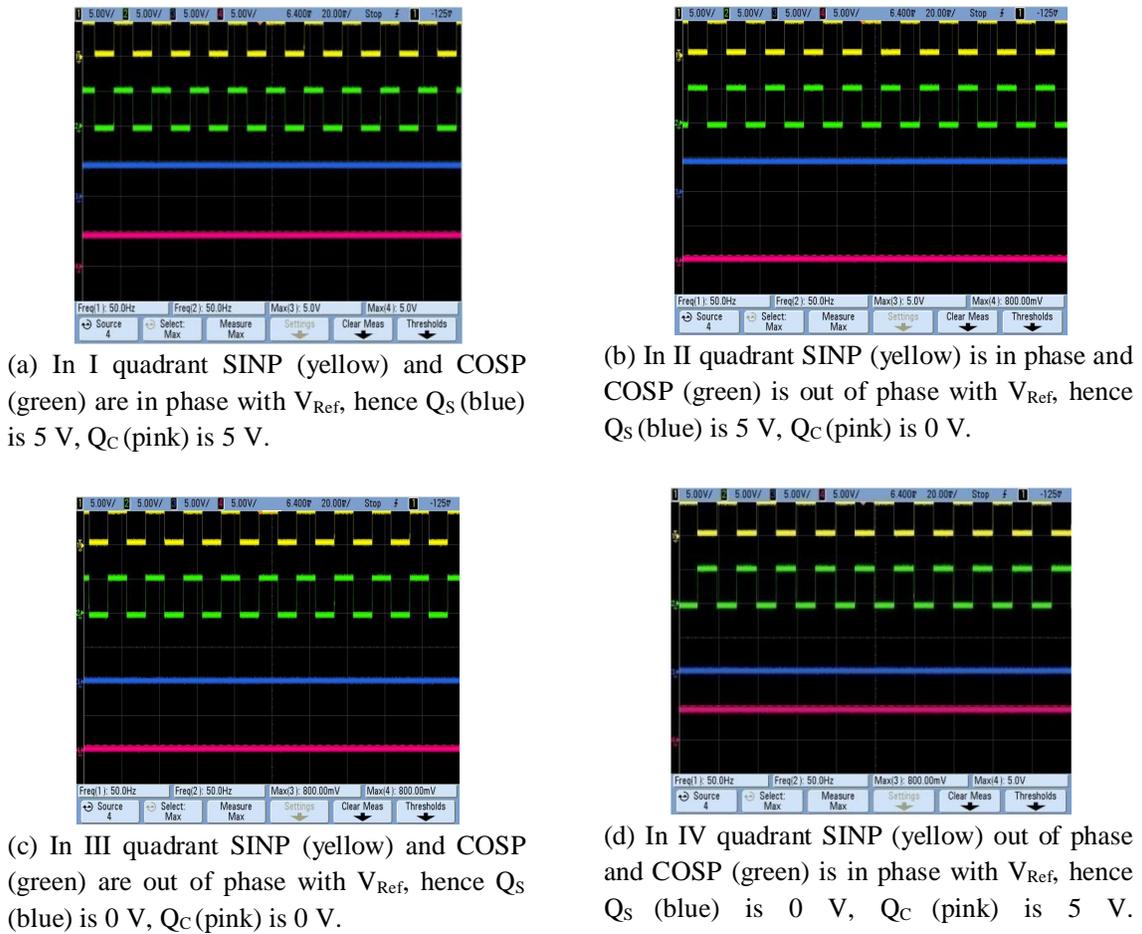


Figure 4.11: Quadrant detector outputs in four quadrants.

The arctangent computation for a full 360° rotation of the shaft in binary notations is

implemented, with 0^0 and 360^0 representing all displays of LED off and on respectively. Binary Angular Measurement (BAM) notation [3] is used to represent the shaft angle and is shown in figure 4.12.

$180^0 \cdot 2^0$ (MSB)	$180^0 \cdot 2^{-1}$	$180^0 \cdot 2^{-2}$	-	-	-	-	-	-	$180^0 \cdot 2^{-9}$ (LSB)
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Figure 4.12: A 10-bit binary angular measurement word

Figure 4.13 shows the performance of the designed SDC based on the results obtained. The display of Angle Position Indicator (API) is the reference for the actual mechanical angle of synchro. The plot indicates linearity of the converter. This new method of digitally detecting the peak amplitudes of synchro signals results in maximum angular error of 0.3^0 between the angle measured by the converter and the actual mechanical angle over the full 360^0 range.

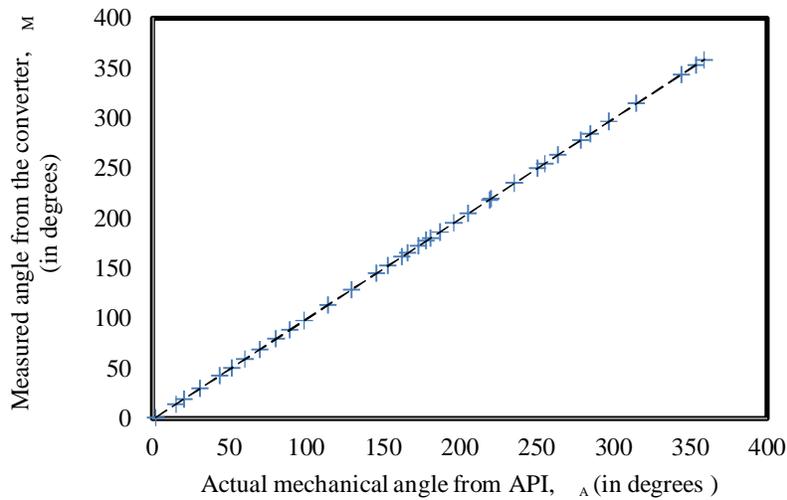


Figure 4.13: Plot of measured angle (θ_M) from the SDC versus actual mechanical angle (θ_A) in the range 0^0 to 360^0 .

Figure 4.14 shows the BAM simulation result for 113.9^0 synchro shaft angle. It is to be noted that the second, fourth and eighth bars of LED are ON and remaining bars are OFF. Based on the representation of BAM, the equivalent synchro shaft angle is calculated as

$$= 0 + 180^0 \cdot 2^{-1} + 0 + 180^0 \cdot 2^{-3} + 0 + 0 + 0 + 180^0 \cdot 2^{-7} + 0 + 0 = 113.9^0.$$

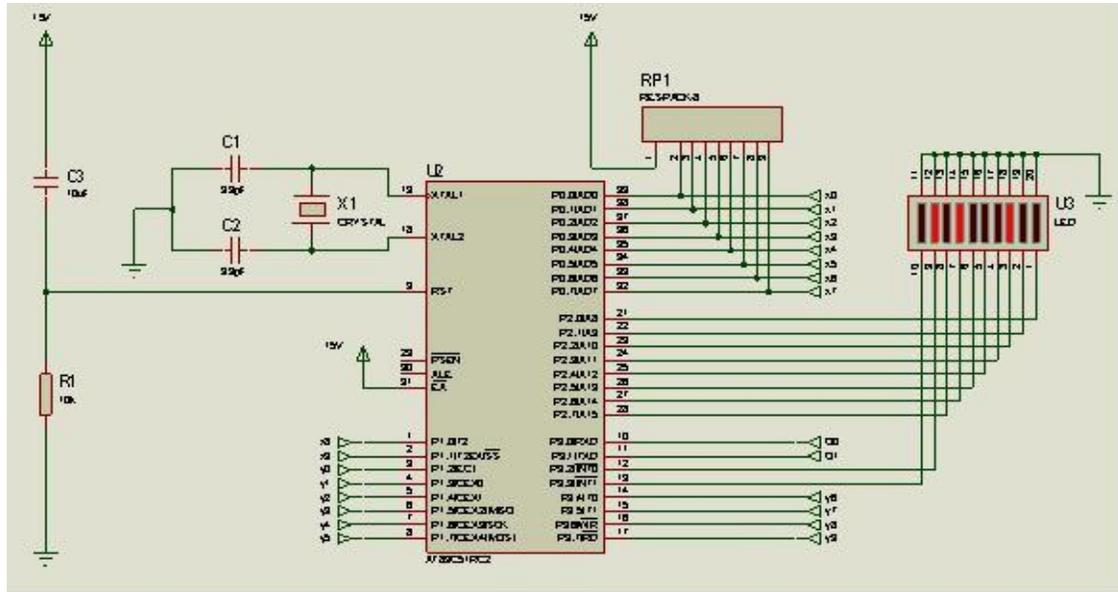


Figure 4.14: Microcontroller output for the shaft angle 113.9°

4.3 Conclusion

Digital peak detection based SDC has been presented. The digital peak detector is designed using high speed DAC, comparator and a counter. It plays a vital role in computation of shaft angle. The estimation of peak amplitude levels of continuously varying scott-T signals: V_s and V_c using DAC with a fixed reference voltage could not provide adequate resolution for output shaft angle. So a new approach is presented in chapter 5 to compute the synchro shaft angle using the concept of pulse width modulation.

References

- [1] Fairchild Semiconductor Corporation, δ DM74LS123 Dual Retriggerable One-shot with Clear and Complementary outputs, δ April 2000.
- [2] Muhhamad Ali Mazidi, Janice Gillispie Mazidi and Rolin D. Mckinlay, δ The 8051 Microcontroller and Embedded Systems, Prentice-Hall, Second edition, Taiwan.
- [3] Philip A. Laplante, δ Real Time Systems Design and Analysis, Wiley-India edition, New Delhi, 2005.

CHAPTER 5

HARDWARE IMPLEMENTATION SYNCHRO-TO- DIGITAL CONVERTER

CONTENTS:

5.1 Methodology

5.2 Implementation

5.3 Experimental results

5.4 Conclusion

References

This chapter presents the design, hardware implementation and experimental results of Synchro-to-Digital Converter (SDC). As the shaft angle information is present in the peak amplitudes of synchro outputs, a parameter called Time Duration Windows (TDW) has been introduced to estimate the synchro shaft angle. The basic idea of the scheme is the linear evaluation of peak amplitudes of scott-T signals using TDW and division of TDWs followed by the inverse tangent operation.

The scott-T output signals V_S and V_C are applied separately to the comparators along with a common triangular signal to get Pulse Width Modulated (PWM) signals. The TDW for each of scott-T signal can be obtained from triangular zero crossing signal and respective PWM signal. The digital design for generating the binary data corresponding to TDW and quadrant detector bits is implemented in a Complex Programmable Logic Device (CPLD) using Altera MAX+plus II 10.2 software. Microcontroller provides the absolute shaft angle based on the output of CPLD. The schematic and layout of prototype SDC is done using ORCAD 9.1 tool.

5.1 Methodology

The new implementation scheme comprises of an electronic scott-T unit, zero crossing detectors, comparators, CPLD and a microcontroller, as shown in figure 5.1. The rotor winding of synchro is supplied with a sinusoidal carrier signal and is given as

$$V_{\text{Ref}}(t) = V_{\text{REF1-REF2}}(t) = V \sin(\omega t) \quad (5.1)$$

where V is the peak amplitude, ω is the frequency of the excitation signal to the rotor.

Then, magnetically induced signals on three stator windings of the synchro are given as

$$\left. \begin{aligned} V_{S1}(t, \theta) &= V \sin t \cos(+120^\circ) \\ V_{S2}(t, \theta) &= V \sin t \cos() \\ V_{S3}(t, \theta) &= V \sin t \cos(+240^\circ) \end{aligned} \right\} \quad (5.2)$$

where θ is the angular position of the synchro shaft.

Equation (5.2) represents the phase voltages of the synchro. The simplification for obtaining line voltages is explained in section 3.2 of chapter 3 and given as

$$\left. \begin{aligned} V_{S3 - S1}(t, \theta) &= V \sin \omega t \sin(\theta) \\ V_{S2 - S3}(t, \theta) &= V \sin \omega t \sin(\theta + 120^\circ) \\ V_{S1 - S2}(t, \theta) &= V \sin \omega t \sin(\theta + 240^\circ) \end{aligned} \right\} \quad (5.3)$$

In this scheme, the synchro three-signal format is converted to two-signal format using electronic scott-T circuit. The electronic scott-T simplification is explained in Appendix A.

The output signals of electronic scott-T are denoted as V_S and V_C and given by

$$\left. \begin{aligned} V_S &= V \sin(\omega t) \sin \theta \\ V_C &= V \sin(\omega t) \cos \theta \end{aligned} \right\} \quad (5.4)$$

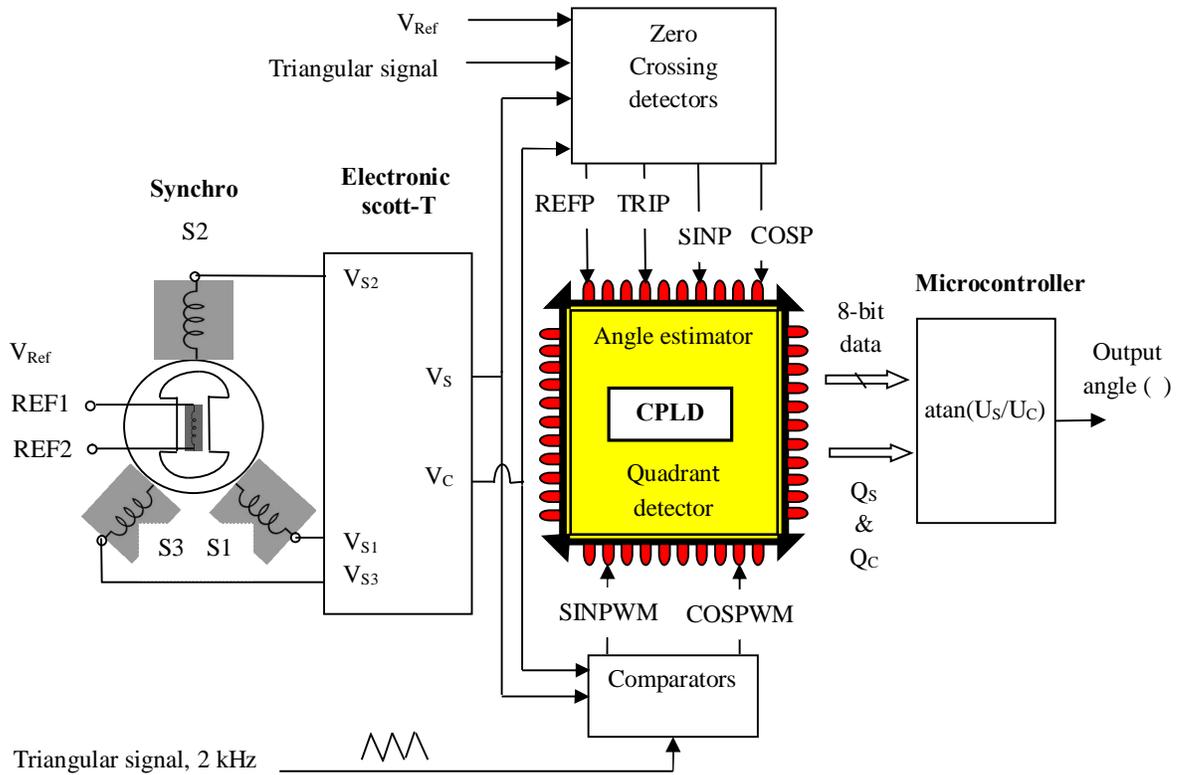


Figure 5.1: Functional block diagram of SDC. The synchro is excited by V_{Ref} and gives three stator signals. The stator voltages: V_{S1} , V_{S2} and V_{S3} are converted into two signals: V_S and V_C using scott-T circuit. These are signals are processed to compute shaft angle.

The REFP, SINP, COSP and TRIP are the zero crossing outputs of V_{Ref} , V_s , V_C and triangular signal, respectively. They are generated from operational amplifier based circuits and are useful in estimation of quadrant in which the shaft angle falls.

5.1.1 Generation of pulse width modulated signal using comparator

Pulse width modulation is a technique in which the width of the output pulse changes according to the amplitude of a modulating signal. The PWM scheme [1] involves comparison of a high frequency triangular carrier signal with a sinusoidal modulating signal. Figure 5.2 shows an operational amplifier based comparator with input and output signals. The sinusoidal and triangular signals are fed to the non-inverting and inverting input terminals of the comparator respectively and comparator outputs high and low levels. So a constant frequency PWM signal can be produced by comparing a modulating signal $m(t)$ with a carrier signal $c(t)$. The binary PWM output can be mathematically written as

$$b_{pwm}(t) = \text{sgn} [m(t) - c(t)] \quad (5.5)$$

where sgn is the signum function.

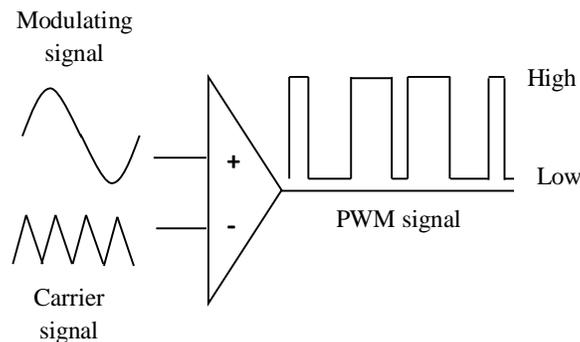


Figure 5.2: Comparator schematic circuit. The output of comparator stays high as long as modulating signal is greater than the carrier signal.

The synchro stator signals are applied to the scott-T unit to generate resolver format signals. The scott-T unit composed of sine generation circuit and cosine generation circuit. The outputs of scott-T are filtered by a low-pass filter of cut off frequency 1 kHz. The low-pass

filter guarantees that no high frequency noise is transferred to the comparator and successive stages.

There are two comparators in the converter to generate pulse width modulated signals called SINPWM and COSPWM. The first comparator is applied with V_S and second comparator is applied with V_C along with a common triangular signal. A triangular signal is applied externally to these comparators. The width of the pulses of SINPWM and COSPWM changes according to the voltage signals V_S and V_C respectively. The comparators' outputs (SINPWM, COSPWM) and zero crossing outputs (REFP, SINP, COSP and TRIP) are sent to a CPLD.

5.1.2 Complex programmable logic device

The CPLD implementation of angle estimator block and quadrant detector block is explained in the following way to achieve absolute synchro shaft angle. CPLD gives two 8-bit digital outputs (Bit₇–Bit₀) and quadrant detector bits (Q_S , Q_C).

5.1.2.1 Angle estimator block

From equation (5.4), it is evident that the angular information is present in amplitude parts of V_S and V_C , so the main objective of this block is to give equivalent digital outputs to the peak amplitudes V_S and V_C . The MATLAB simulation of the technique for synchro position measurement is shown in figure 5.3. It demonstrates the measurement of peak amplitude of V_S or V_C with the help of Time Duration Window (TDW). TDW is the time gap (t_1 - t_2) between rising edge of triangular signal and falling edge of pulse width modulated signal in every cycle of V_S (or) V_C . The TDW varies as the synchro shaft rotates and can be calculated from the equation (5.6). Hence, the number of system clocks accommodated in the TDW is a measure of peak amplitude of V_S or V_C . The linear evaluation of amplitude (A) using TDW shows the effectiveness of the technique.

$$\text{TDW} = 8\text{-bit binary count value} * \text{Time period of system clock} \quad (5.6)$$

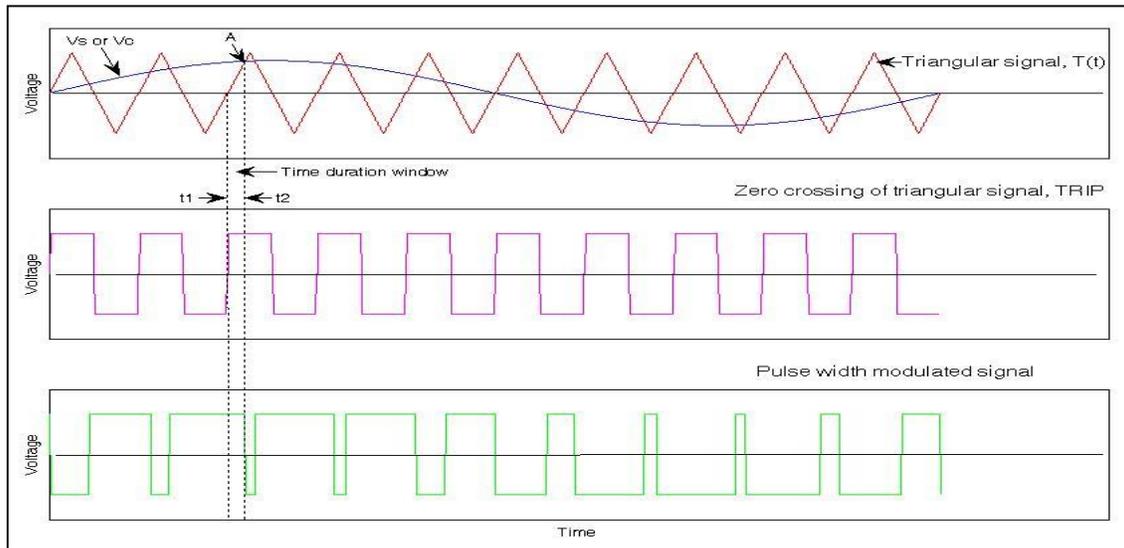


Figure 5.3: Demonstration of time duration window for shaft angle position of synchro. Time duration window is the time gap between rising edge of zero crossing of triangular signal and falling edge of pulse width modulated signal, measured at the peak amplitude of V_s or V_c .

Figure 5.4 gives the logical circuit for angle estimator block which implements the count value for the TDW ϕ of V_s and V_c . There are two sub blocks to generate 8-bit count values one for V_s another for V_c . Each sub block consists of a rising edge detectors, mod-10 counter, falling edge detector, EX-NOR gate and 8-bit counter. Since the signals V_s and V_c have a frequency of 50 Hz, the peak amplitude occurs at 5 ms. The triangular signal has a frequency 2 kHz, the tenth cycle of triangular signal approaches near to the peak amplitude of V_s and V_c . Therefore, two internal enable signals EN_1 , EN_2 are generated from mod-10 counter. EN_1 is to trigger the rising edge detector of TRIP signal and EN_2 is to trigger the falling edge detector of SINPWM (or) COSPWM signal respectively. Hence, an EN_1 signal starts the 8-bit counter at 10th rising edge of triangular signal and EN_2 signal stops the 8-bit counter at 10th falling edge of the pulse width modulated signal with respect to SINP (or) COSP. The microcontroller generates a local reset signal at the end of every cycle of V_s and V_c . In this way the counter provides 8-bit digital output for the peak amplitudes of V_s and V_c separately and these counts are used to estimate the angle of synchro shaft.

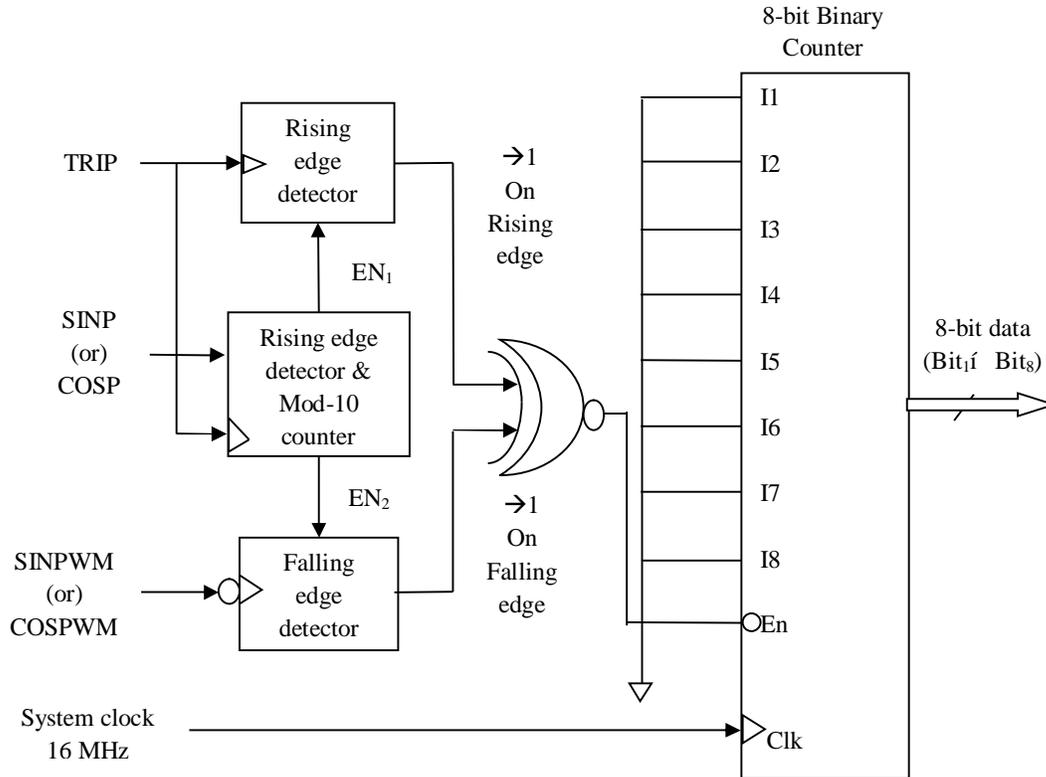


Figure 5.4: Angle estimator logic diagram. This circuit calculates the number of systems clocks falling in the time duration windows of V_S and V_C .

5.1.2.2 Quadrant detector block

Figure 4.4 of chapter 4 shows the variation of V_S and V_C signals with respect to reference signal V_{Ref} . It is noticed that in first quadrant both V_S and V_C are in phase with V_{Ref} . In the second quadrant, V_S is in phase and V_C becomes out of phase with V_{Ref} . In the third quadrant both V_S and V_C are out of phase with V_{Ref} . In the fourth quadrant, V_S is out of phase and V_C becomes in phase with V_{Ref} . So a quadrant detector block is required to determine the quadrant in which the synchro shaft angle falls. Based on above analysis, the quadrant detector designed as a two flip flops based logical circuit which takes inputs: REFP, SINP, and COSP and generates two digital output bits: Q_S , Q_C . Table 4.2 is useful to determine the quadrant of shaft angle.

The digital realization of quadrant detector block is shown in Figure 5.5, which outputs the level of D inputs based on the rising edge of sampling clock signal. The sampling clock for

the flip-flops is designed such a way that a pulse is generated in each positive half cycle of REFP signal. The quadrant detector outputs are either high or low based on the quadrant.

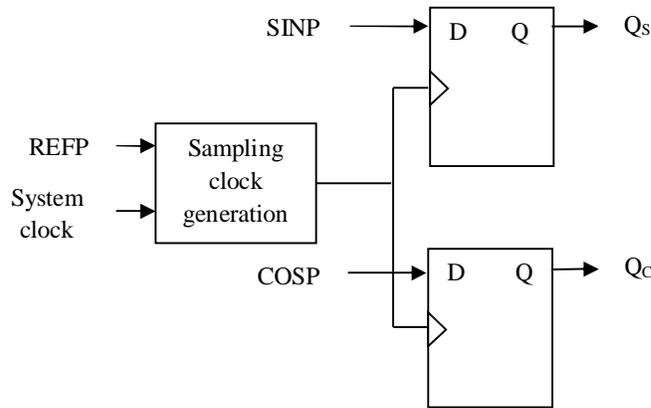


Figure 5.5: Quadrant detector logic diagram. It takes REFP, SINP, COSP and system clock as inputs and gives outputs Q_s and Q_c . These outputs determines quadrant in which shaft angle falls.

5.1.3 Microcontroller

The digital 8-bit count values of V_s and V_c represents $A \sin(\theta)$ and $A \cos(\theta)$, respectively. These are sent to the microcontroller along with quadrant bits Q_s and Q_c . A software code has been written in a microcontroller that reads U_s , U_c and divides these count values. Then the inverse function of the tangent also applied. Based on quadrant detector bits, the microcontroller calculates the absolute angle of synchro as per the table 4.2. To ensure proper reading of two 8-bit counts and quadrant bits, there are two signals sel_1 and sel_2 applied from the microcontroller.

$$\left. \begin{aligned} U_s &= A \sin(\theta) \\ U_c &= A \cos(\theta) \\ \theta &= \arctan(U_s / U_c) \end{aligned} \right\} \quad (5.7)$$

The harmonic interference [2] exists in the three-phase synchro voltage signals. The harmonic components still continue in electronic scott-T output signals V_s and V_c . They can

be cancelled ratio-metrically (from equation 5.7) such that the conversion error in the angle measurement is minimized.

5.2 Implementation

The hardware implementation of SDC involves analog and digital electronic circuits. The analog portion operates the reference excitation signal and synchro signals. These are processed into digital format and fed to digital portion of the converter for the estimation of synchro shaft angle.

5.2.1 Schematic circuits

The schematic of the analog circuitry of SDC using standard electronic components is shown in figure 5.6. The analog circuit includes differential amplifier, electronic scott-T (also called as sine and cosine generation circuit), low-pass filters (LPF), zero crossing detectors and comparators. The inputs for the analog circuit are reference signal (V_{Ref}) and stator signals of synchro. The AC supply is stepped down from 230 V_{rms} , 50 Hz to 24 V_{rms} for safe experimentation and it used as the excitation voltage. The transformation ratio between stator and rotor windings of the synchro was 0.8. As a result, the stator signals from the synchro have voltage of 19 V_{rms} (or) 27 V_{P-P} . The AC signals with 27 V_{P-P} , 50 Hz from the synchro terminals S1, S2 and S3 are connected to the converter. The triangular signal of frequency 2 kHz is also externally applied to SDC.

The peak amplitude of the signals V_S , V_C is approximately 5 V because of the voltage scaling (by one fifth) done at the first stage of the converter. Then these signals are given to LPFs. The LPFs are designed with the components $R=1.5\text{ k}$, $C=0.1\text{ }\mu\text{F}$ having a cut-off frequency 1 kHz. For better shaft angle measurement experimentation is done with the higher order LPFs however, the error between actual results and measured results is increasing. Further, the significance of LPFs here is to eliminate high frequency noise and should act as a simple buffer. The operational amplifier, AD711 [3] used to generate the zero crossing of reference

signal (REFP), zero crossing of V_s (SINP), zero crossing of V_c (COSP), zero crossing of triangular signal (TRIP). The comparator, AD790 [4] is used to generate the pulse width modulated signals (SINPWM and COSPWM). These signals provided as inputs to the CPLD. The MAX3241E RS-232 transceiver converts analog electronics operating voltage (-15 V and +15 V) levels to digital electronics operating voltage levels (0 V and +5 V) [5]. So it acts as voltage translator between the analog and digital electronics. As the implementing technique involves zero crossing detections of scott-T output signals (V_s , V_c) and triangular signal, the synchronization between them is not necessary. Further, the accuracy of the method is immune to the phase shift between the synchro outputs.

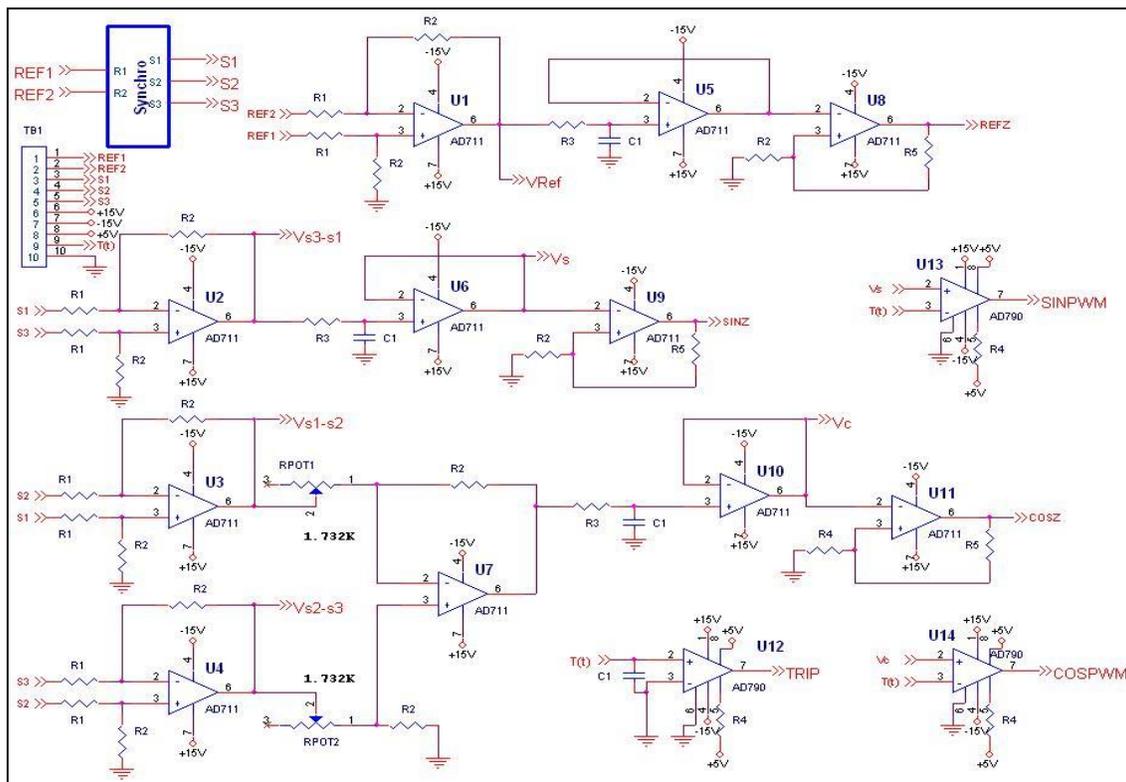


Figure 5.6: Schematic circuit of analog portion of Synchro-to-Digital Converter.

- Notes:** U1: Reference differential amplifier
 U2: Sine generation circuit
 U3, U4, U7: Cosine generation circuit } Electronic scott-T circuit
 U5, U6, U10: Low-pass filters
 U8, U9, U11, U12: Zero crossing detectors
 U13, U14: Comparators

The digital logics for angle estimator block (to generate TDWs) and quadrant detector has been implemented in CPLD. The CPLD chosen for the digital design is EPM3128ATC100. It has 128 macro cells, 100 pins and supports hot socketing. The CPLD module contains EPM3128ATC100, +5 V/+3.3 V power supply chip LT1085, 16 MHz external crystal, Joint Test Action Group (JTAG) interface circuit and power on reset chip MAX824. The JTAG programming environment has four signals: Test Mode Select (TMS), Test Clock (TCK), Test Data In (TDI) and Test Data Out (TDO) [6]. The pin assignments and the external circuits of EPM3128ATC100 are shown in figure 5.7.

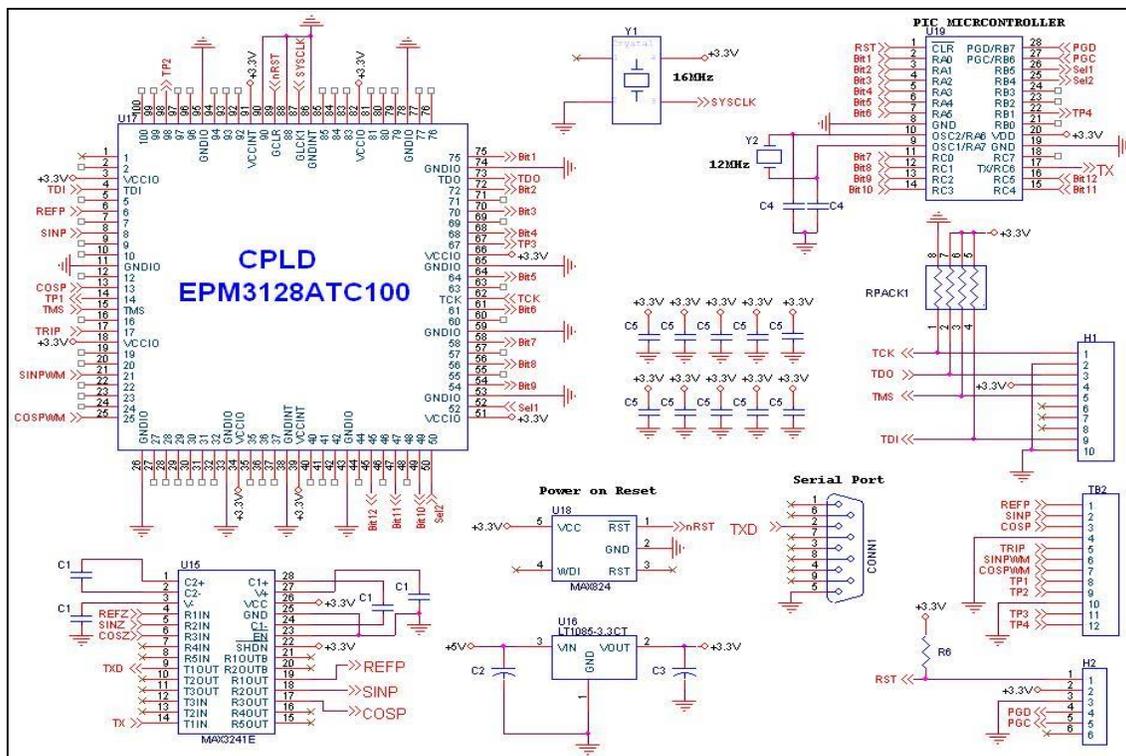
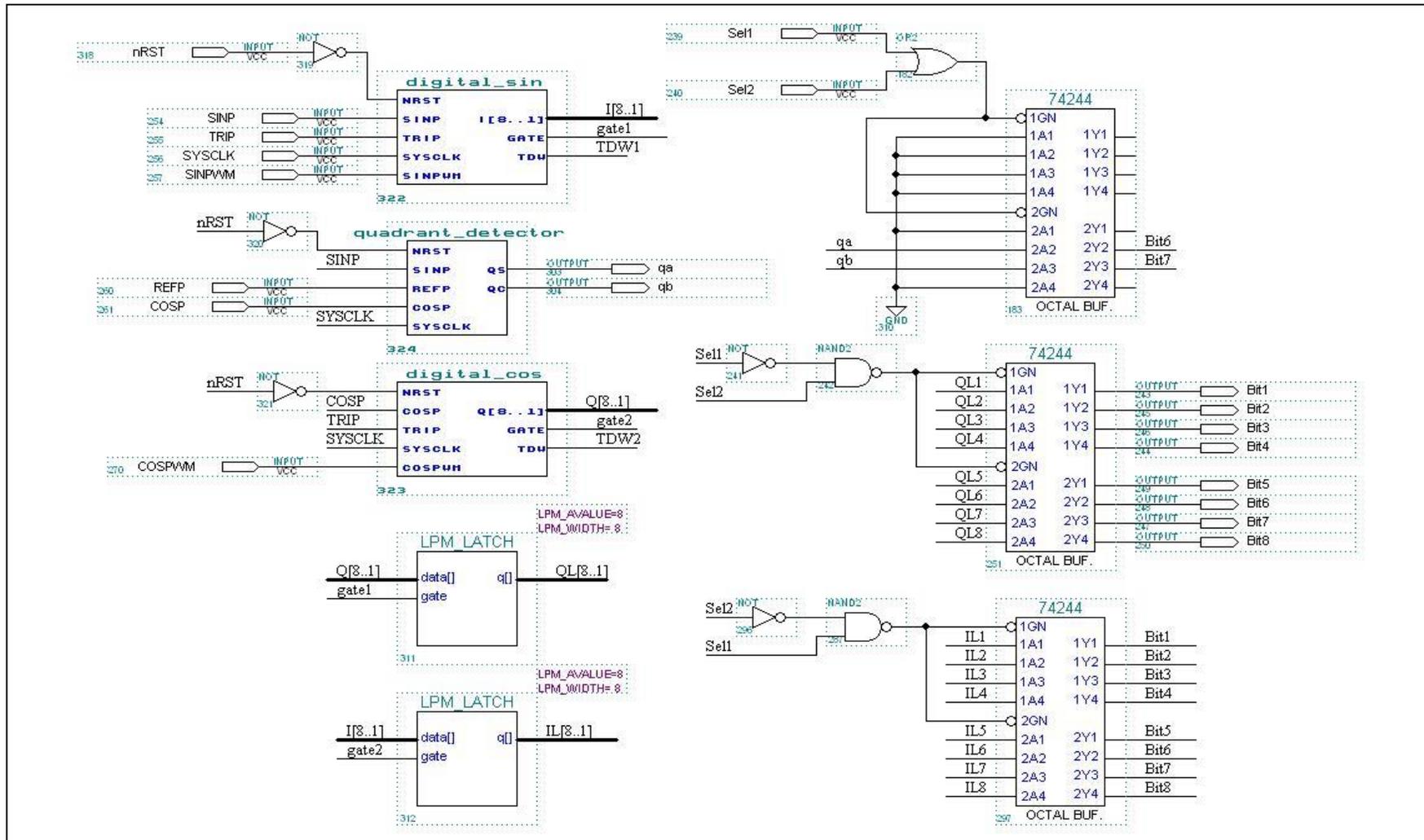


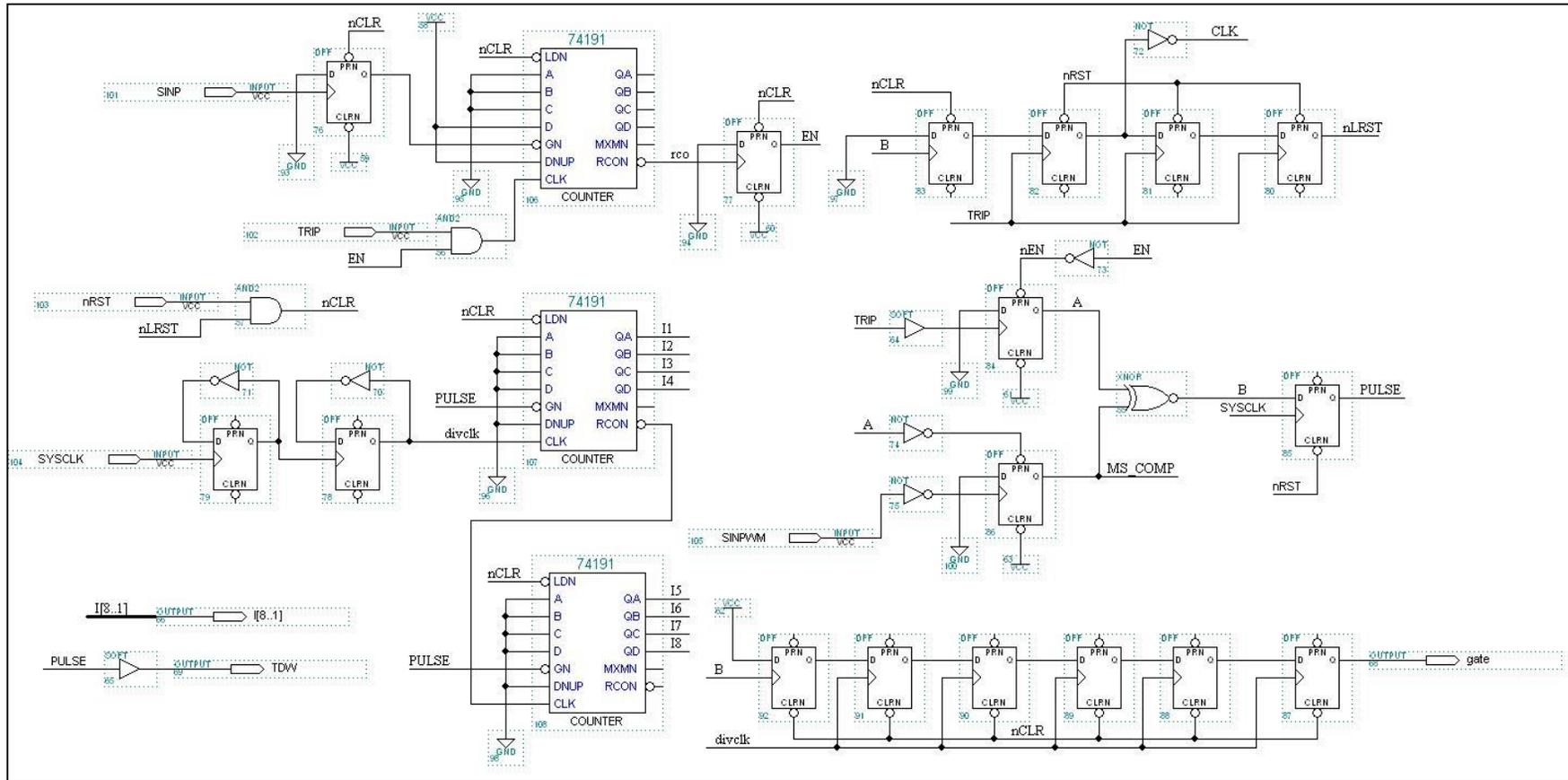
Figure 5.7: The pin assignments, external circuits of CPLD-EPM3128ATC100 and microcontroller-PIC18F25K22. The CPLD gives binary data (Bit₁ Bit₈) and quadrant bits (Q_S and Q_C) and sent to microcontroller to compute shaft angle position.

The CPLD implementation of angle estimator and quadrant detector is shown in figure 5.8. Figure 5.8 (a) shows the top level schematic circuit of CPLD. The angle estimator block consists of two separate digital circuits: digital_sine and digital_cosine, which are shown in figures 5.8 (b) and (c) respectively. This block provides two 8-bit digital outputs. The digital

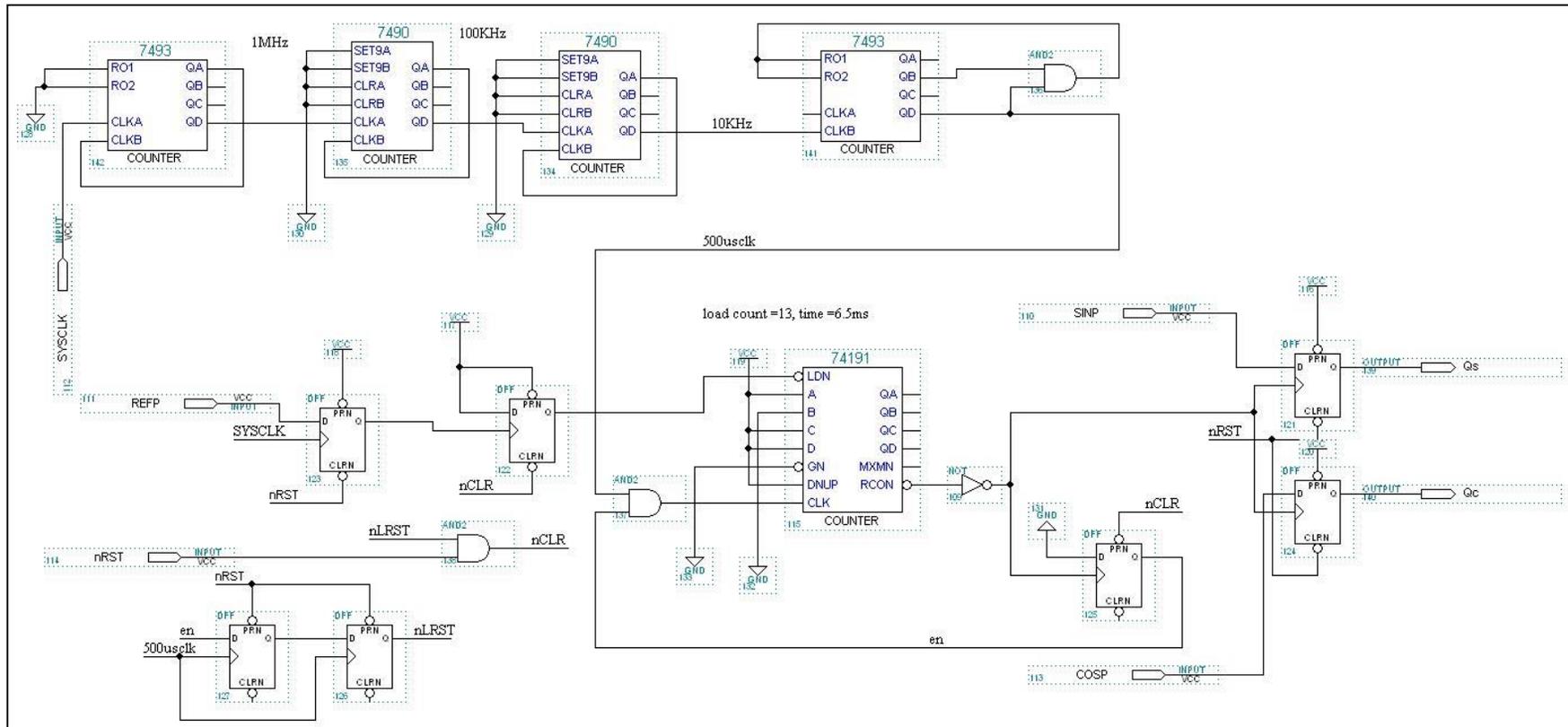
counts $[I_1 \text{ } I_8]$ and $[Q_1 \text{ } Q_8]$ represents peak amplitudes of V_S and V_C respectively. The quadrant detector block schematic circuit is shown in figure 4.8 (d), which provides two quadrant bits (Q_S and Q_C). The resource utilization of CPLD on Altera based MAX+plus II compiler is given in figure 5.9.



(a) Top level schematic circuit of CPLD



(b) Schematic circuit of digital_sine block



(d) Schematic circuit of quadrant detector block

Figure 5.8: CPLD implementation of angle estimator (digital_sine & digital_cosine) and quadrant detector

```

** RESOURCE USAGE **

Logic Array Block   Logic Cells   I/O Pins   Shareable   External
                  (used/total) (used/total) Expanders   Interconnect

A:  LC1 - LC16     7/16( 43%)  0/10(  0%)  0/16(  0%)  9/36( 25%)
B:  LC17 - LC32    16/16(100%) 2/10( 20%)  2/16( 12%) 19/36( 52%)
C:  LC33 - LC48    16/16(100%) 3/10( 30%)  1/16(  6%) 20/36( 55%)
D:  LC49 - LC64    16/16(100%) 4/ 9( 44%)  2/16( 12%) 19/36( 52%)
E:  LC65 - LC80    16/16(100%) 2/10( 20%)  2/16( 12%) 20/36( 55%)
F:  LC81 - LC96    16/16(100%) 7/ 9( 77%) 12/16( 75%) 29/36( 80%)
G:  LC97 - LC112   16/16(100%) 5/ 9( 55%) 13/16( 81%) 25/36( 69%)
H:  LC113 - LC128  15/16( 93%) 1/ 9( 11%)  3/16( 18%) 20/36( 55%)

Total dedicated input pins used:           2/4   ( 50%)
Total I/O pins used:                       24/76  ( 31%)
Total logic cells used:                    118/128 ( 92%)
Total shareable expanders used:            35/128 ( 27%)
Total Turbo logic cells used:             118/128 ( 92%)
Total shareable expanders not available (n/a): 0/128 (  0%)
Average fan-in:                            4.71
Total fan-in:                              556

Total input pins required:                  10
Total output pins required:                 12
Total bidirectional pins required:          0
Total reserved pins required:               4
Total logic cells required:                 118
Total flipflops required:                   86
Total product terms required:               371
Total logic cells lending parallel expanders: 0
Total shareable expanders in database:      30
Logic cells inserted for fitting:           2

Synthesized logic cells:                   4/ 128 (  3%)
  
```

Line 235 Col 65 INS

Figure 5.9: Resource usage of CPLD-EPM3128ATC100

The flowchart of the program is shown in figure 5.10. A software code (shown in Appendix C) written in microcontroller (PIC18F25K22) that reads the digital data of U_s and U_c and calculates actual shaft angle. The available resources in this microcontroller are 32 KB of flash memory, 1536 Bytes of Static Random Access Memory (SRAM), 256 Bytes of Electrically Erasable Programmable Read Only Memory (EEPROM), 19 channels 10-bit ADC, three 8-bit timers, four 16-bit timers, Serial Peripheral Interface (SPI) and Inter Integrated Circuit (I^2C) modules [7].

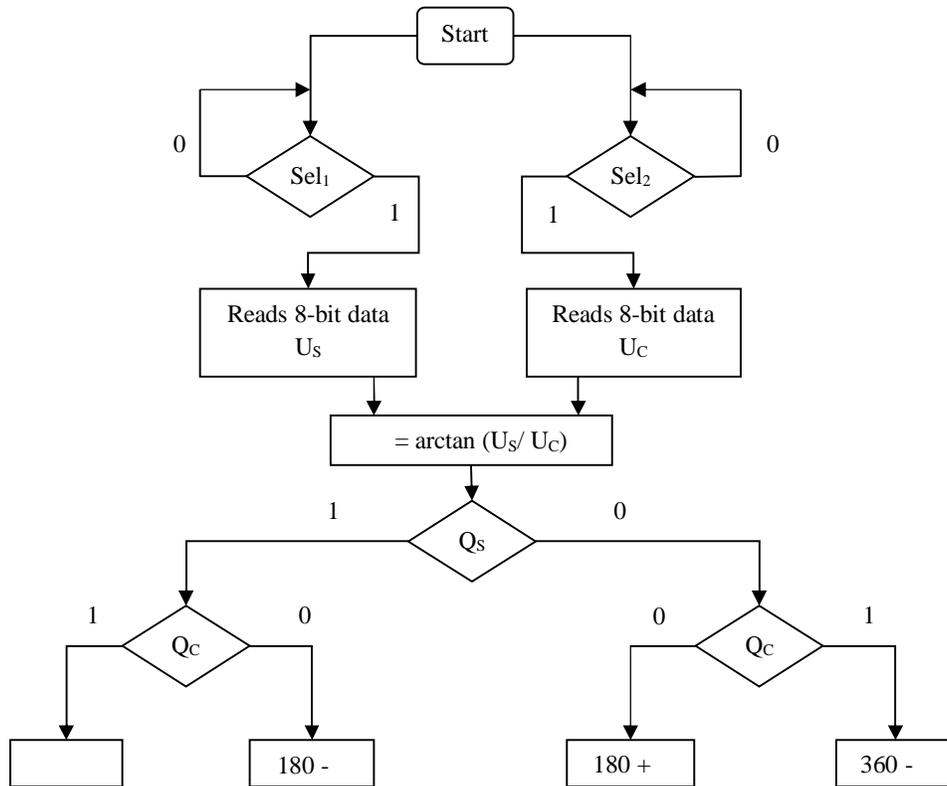


Figure 5.10: Flowchart of the software program

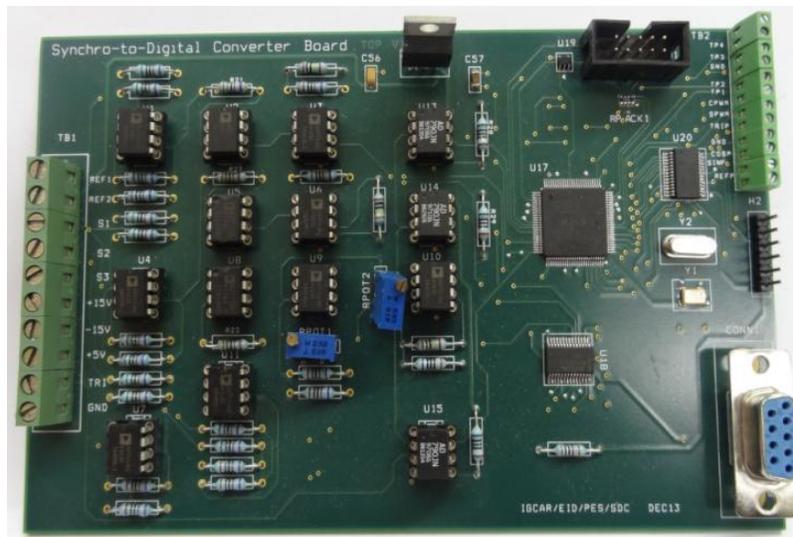


Figure 5.11: A photograph of the SDC board

5.2.2 Experimental setup

The prototype SDC is designed and fabricated, which is shown in figure 5.11. The Bill Of Materials (BOM) is given in Appendix D. In order to validate the implemented converter, an

experimental setup has been established as shown in figure 5.12. In this experiment, a standard synchro (23CX5b) is mounted on the shaft of a 3-phase induction motor (runs at 1440 rpm) with a 983:1 gear reduction. The main specifications of synchro are given in table 5.1.

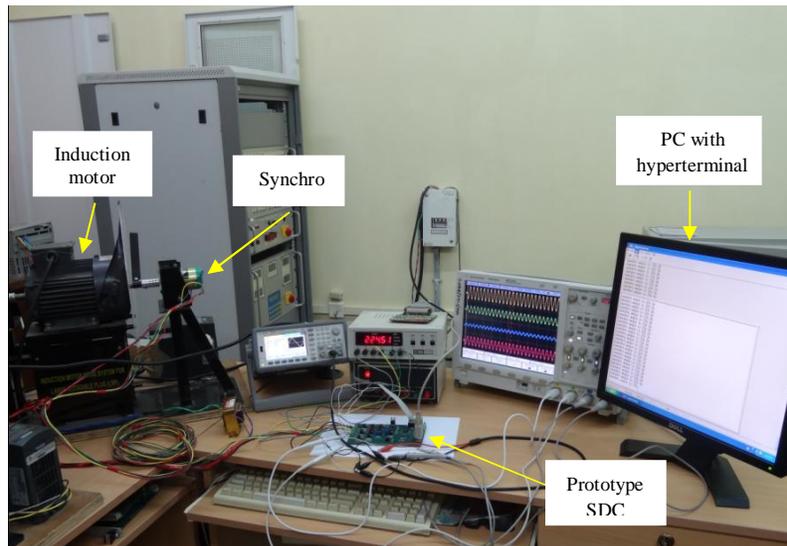


Figure 5.12: Experimental setup of the implemented SDC system. The synchro stator outputs are connected to SDC and the shaft angle is displayed on computer monitor.

Table 5.1: Specifications of synchro used for experimentation

Parameter	Value
Model	23CX5b
Angle range	$0^{\circ} - 360^{\circ}$
Diameter	2.3 inch
Accuracy	7 arc min
Input frequency	50 Hz
Primary voltage	$115 V_{rms}$
Primary current	100 mA
Primary power	3 W
Transformation Ratio	0.76 - 0.8

5.3 Experimental results

The synchro is excited by an AC voltage signal at the rotor and it generates three phase voltages at the stator based on the principle of electromagnetic induction. The signal, V_{Ref} shown in experimental results is one-fifth of the excitation signal. The induced stator line voltage signals: V_{S3-S1} , V_{S2-S3} , V_{S1-S2} of synchro along with input signal V_{Ref} are shown in figure 5.13. The synchro outputs are supplied to the electronic scott-T to generate two equivalent signals called as V_S and V_C . The generated outputs V_S , V_C along with V_{Ref} are shown in figure 5.14.

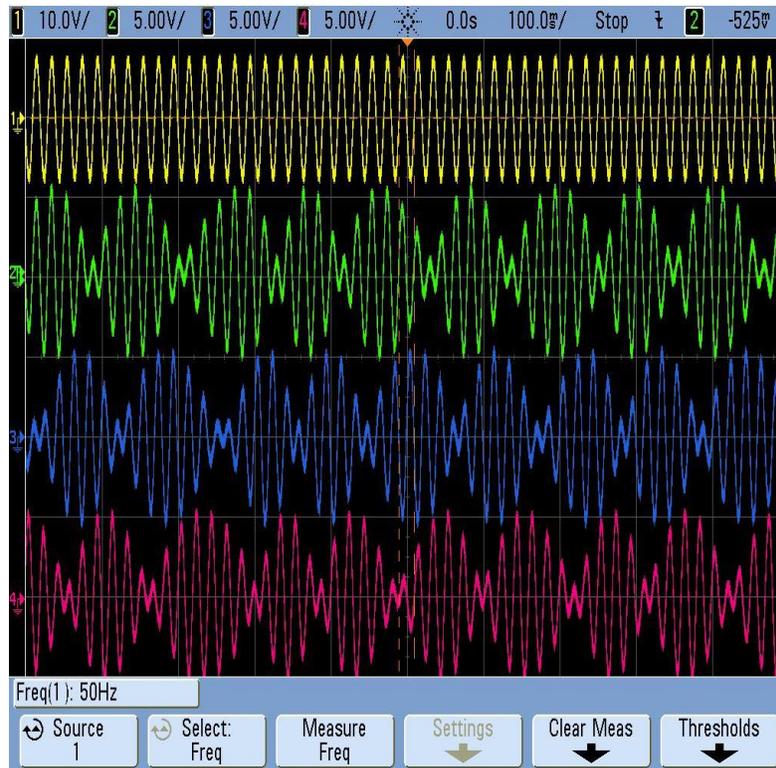


Figure 5.13: Input signal: V_{Ref} (yellow) and output signals: V_{S3-S1} (green), V_{S2-S3} (blue), V_{S1-S2} (pink) of synchro. The output signals are amplitude modulated by rotor angle.

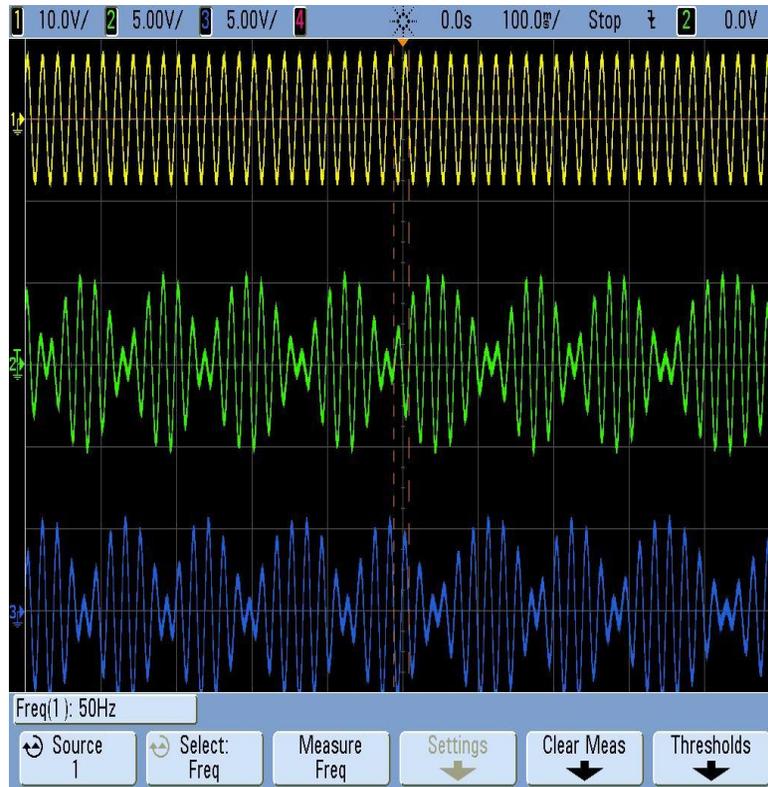
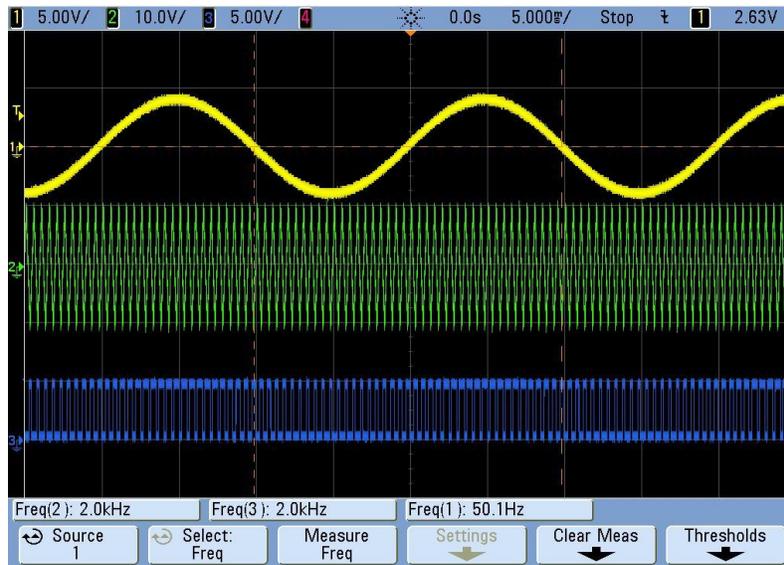
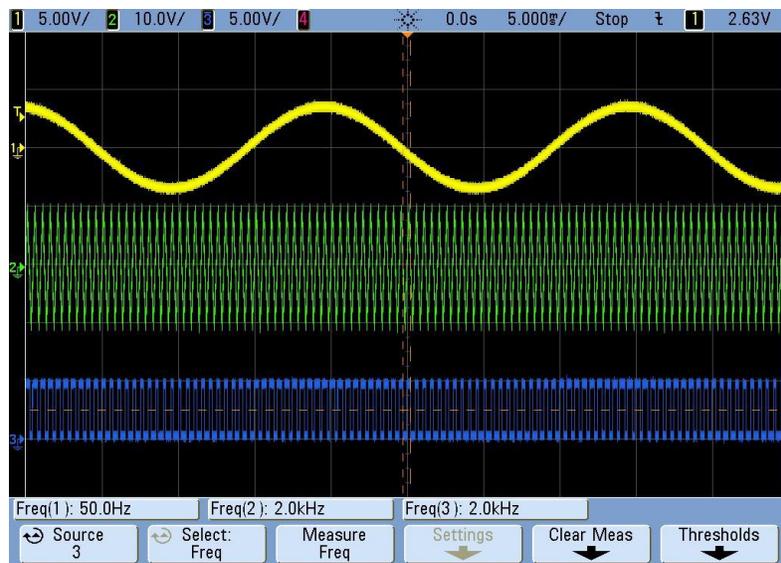


Figure 5.14: Electronic scott-T output signals: V_s (green) and V_C (blue). The amplitude variations of V_s and V_C are in quadrature.

The comparators AD790JN have been adopted for each scott-T filtered output signal. A 2 kHz triangular signal is applied to the comparators to generate the pulse width modulated signals. Figure 5.15 shows the generation pulse width modulated signals when the shaft is stationary at 131.41° . Figure 5.15 (a) shows the pulse width modulated signal, SINPWM corresponding to the signal V_s . Figure 5.15 (b) shows the pulse width modulated signal, COSPWM corresponding to the signal, V_C . The width of the pulses increases as the amplitude of scott-T signals increasing and vice versa. Since the synchro shaft is in second quadrant, V_s and V_C are out-of phase by 180° to each other.



(a) Generation of pulse width modulated signal, SINPWM (blue) by comparison of V_s (yellow) and triangular signal (green).

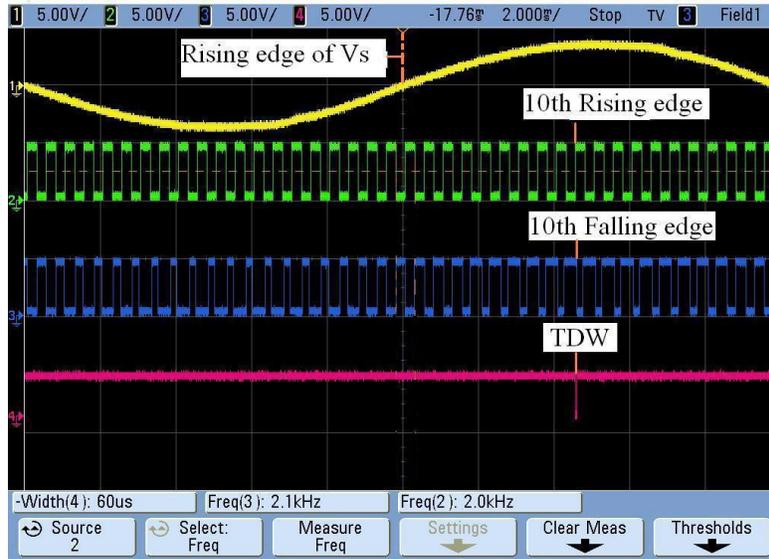


(b) Generation of pulse width modulated signal, COSPWM (blue) by comparison of V_c (yellow) and triangular signal (green).

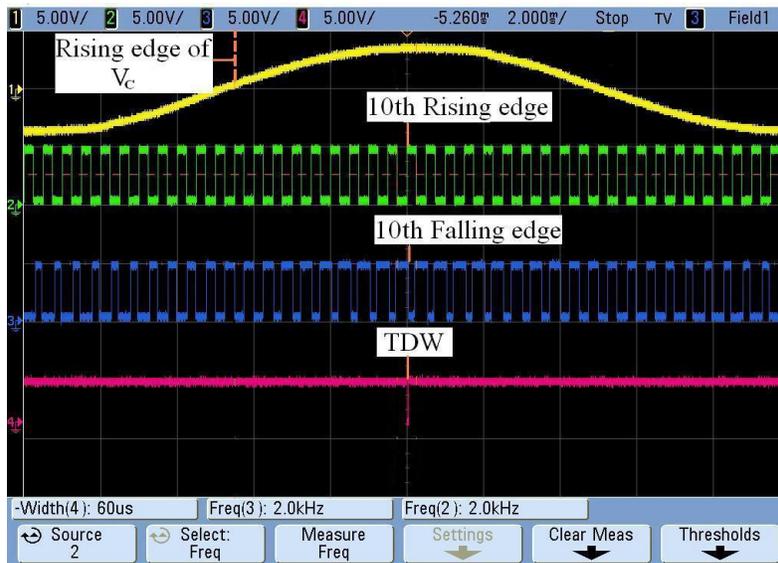
Figure 5.15: Generation of pulse width modulated signals using comparator.

Figure 5.16 shows the generation of TDWs using CPLD. Since the reference sinusoidal signal V_{Ref} is having the time period of 20 ms (50 Hz), the peak amplitudes of V_s and V_c occurs at 5 ms. The triangular signal has a time period of 0.5 ms (2 kHz), hence the 10th rising edge of TRIP and the 10th falling edge of pulse width modulation signals are

considered to measure the peak amplitudes of V_S and V_C . The number of system clocks accommodated in TDWs is measure of peak amplitude of V_S and V_C correspondingly. The 8-bit counters inside the CPLD gives the digital output corresponding to V_S and V_C .



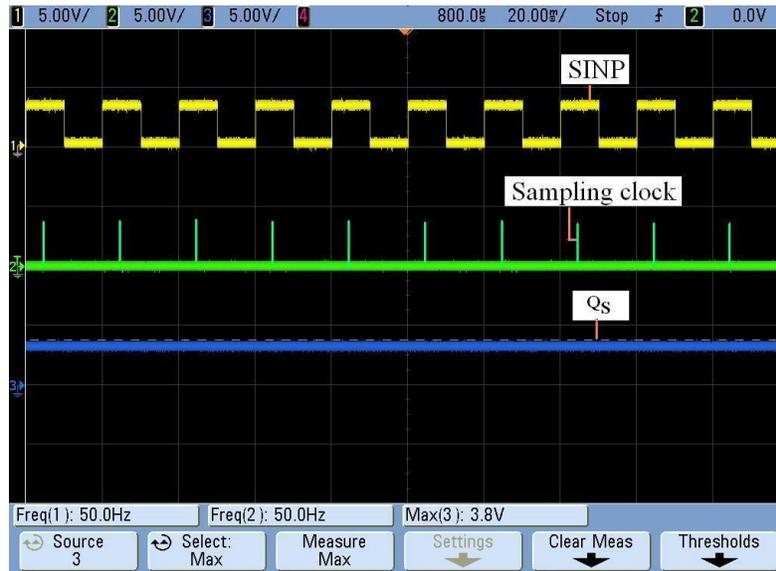
(a) Time duration window (pink) at the peak amplitude of V_S (yellow). It is a pulse of small width obtained between 10th rising edge of TRIP (green) and 10th falling edge of SIMPWM (blue).



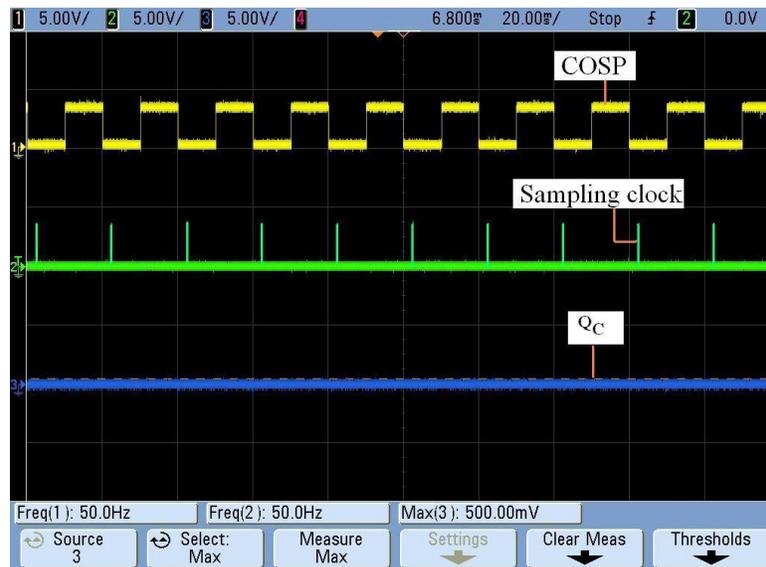
(b) Time duration window (pink) at the peak amplitude of V_C (yellow). It is a pulse of small width obtained between 10th rising edge of TRIP (green) and 10th falling edge of COSPWM (blue).

Figure 5.16: CPLD generation of Time Duration Windows (TDW).

Figure 5.17 illustrates the experimental results of quadrant detector for the synchro shaft angle 131.41° . It is noted that Q_S bit is high and Q_C bit is low in second quadrant. It was experimentally verified that Q_S , Q_C bits are high in first quadrant; Q_S , Q_C bits are low in third quadrant; Q_S bit is low and Q_C bit is high in fourth quadrant.



(a) Sine quadrant bit, Q_S is at high voltage



(b) Cosine quadrant bit, Q_C is at low voltage

Figure 5.17: Quadrant detector output polarity levels when rotor shaft stationary at 131.41° .

The two 8-bit digital outputs multiplexed on the same output pins of CPLD represent the peak amplitudes of V_S and V_C . Quadrant detector bits represent the quadrant in which synchro shaft angle falls. The digital outputs and quadrant bits sent to the microcontroller. The microcontroller calculates the absolute angle of synchro which is generated as TX. A serial interface connector has been provided on board to display the angle through hyper terminal. Figure 5.18 shows the results of measured synchro shaft angles obtained by the SDC.

```

SDCTEST - HyperTerminal
File Edit View Call Transfer Help
synchro angle is 2.86 107.29
synchro angle is 2.86e is 103.54
synchro angle is 2.86angle is 101.72
synchro angle is 2.86hro angle is 97.98
synchro angle is 2.8686is 234.78e is 359.5
synchro angle is 2.86.48.56
s
synchro angle is 2.8686.5529.5654.78e is 3
synchro angle is 2.86s 85.84 129.56

synchro angle is 2.86
synchro angle is 2.86
synchro angle is 3.56
synchro angle is 4.27
synchro angle is 6.89
synchro angle is 9.03
synchro angle is 15.07
synchro angle is 18.29
synchro angle is 21.20
synchro angle is 29.41
synchro angle is 34.54
synchro angle is 45.84
synchro angle is 51.29
synchro angle is 60.54
synchro angle is 64.50
synchro angle is 68.66
synchro angle is 75.10
synchro angle is 115.32
synchro angle is 131.41
synchro angle is 146.84
synchro angle is 158.83
synchro angle is 175.91
synchro angle is 181.18

```

Figure 5.18: Display of hyper terminal, showing the synchro angle.

High accuracy tracking-type angle position indicator (AP-501 from CSI) is used to notify the actual mechanical angle (θ_M) of synchro. Figure 5.19 compares the results obtained from the converter and mechanical angle of synchro for various shaft angle positions. From the plot, it is cleared that the converter exhibits good linearity over 0° - 360° range. The maximum error (θ_{M-}) between actual to measured angle is 0.16° , so the implemented converter nearly has 11-bit resolution. The performance specifications and comparison of the present work with earlier published reports are given in table 5.2 and table 5.3 respectively.

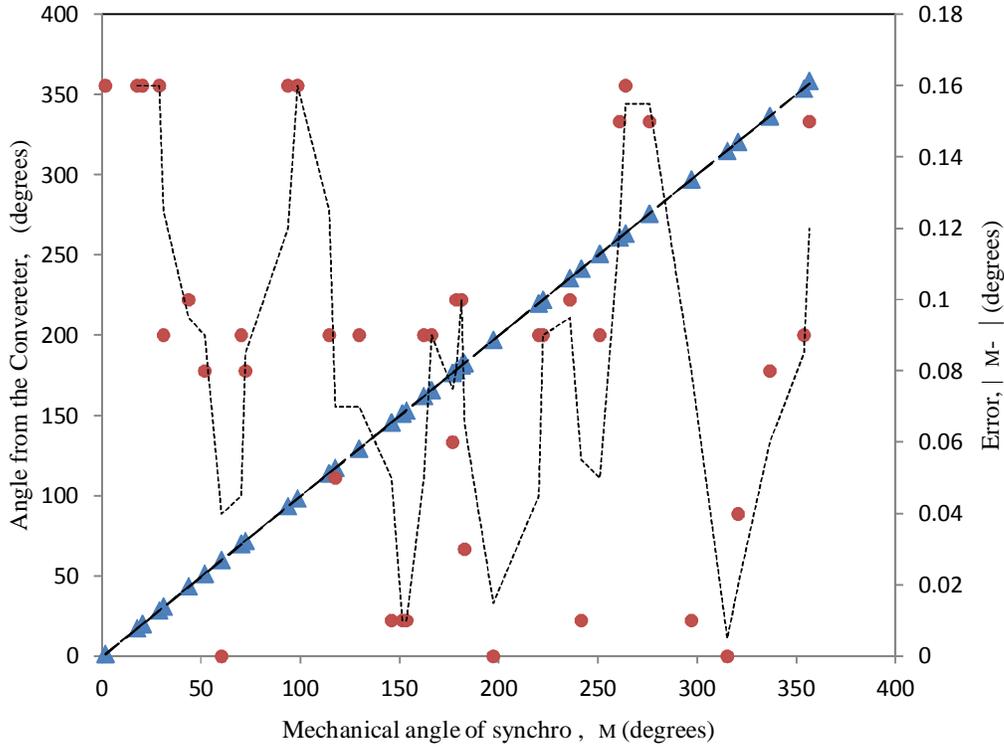


Figure 5.19: Plot of mechanical angle of synchro versus angle obtained from the implemented converter. The dashed line is a linear fit to the measured angles (▲). Also shown is the error (●) between actual mechanical angle and measured angle.

Table 5.2 The specifications of prototype SDC

Parameter	Commercial SDC	Prototype SDC
Input frequency	50 Hz	50 Hz
Resolution	12-bit	11-bit
Accuracy	8.5 arc minutes	10 arc minutes
Shaft speed measurement	Not available	Available
Diagnostic features		
i) loss of signal detection	Not available	Available
ii) stator reversal connection detection		

Table 5.3 Comparison of competitive methods

Conversion method	Main modules involved	Excitation input	Measured parameters	Output form	Simulation/Experimental	Angular accuracy (degrees)
Attaianese and Tomasso	ADC and EPROM	Square signal	Angular position and speed	analog	Experimental	1.4
Sarma et al.	DSP processor, ADC and S&H circuit	Sinusoidal signal	Angular position	analog	Both Simulation and Experimental	Not reported
Ben-Brahim et al.	Quadrant determination circuit, triggering circuit and S&H circuit	Sinusoidal signal	Angular position	analog	Both Simulation and Experimental	Not reported
Khaburi	ADC and angle tracking observer	Square signal	Angular position	analog	Experimental	0.33
Nay Lin Htun Aung et al.	Synchronous integrator and tracking observer	Sinusoidal signal	Angular position and speed	analog	Both Simulation and Experimental	0.25
Present work	Scott-T, comparators, angle estimator, quadrant detector and arctangent function	Sinusoidal signal	Angular position and speed	Both analog and digital	Both Simulation Experimental	0.16

The tracking rate of the proposed converter can be calculated in the following way.

$$\begin{aligned}
 \text{Tracking rate} &= 1/\text{conversion time} \\
 &= 1/((2^{\text{resolution}}) * \text{excitation signal time period}) \\
 &= 1.4 \text{ rpm}
 \end{aligned}$$

This converter finds an application in accurate positioning measurement, where the motor driven mechanisms rotate at low speeds (approximately at 1 rpm). However, the Small Rotatable Plug (SRP) & Large Rotatable Plug (LRP) drives of reactor run at fast speed of 0.298 rpm and 0.196 rpm respectively.

5.4 Conclusion

A novel method is proposed using the concept of PWM for the computation of synchro shaft angle. In this method, the accuracy of the present converter mainly depends on TDW. The in-

house developed low-cost SDC is a combined analog and digital circuit. The analog circuitry implemented using operational amplifiers while the digital circuitry realized using CPLD. The prototype Synchro-to-Digital Converter provides a digital readout of synchro mechanical angle through onboard serial port. The experimental results are presented using a laboratory setup. It is observed that the deviation of the angle measured by the converter from the actual mechanical angle does not exceed 0.16° over the full 360° range.

References

- [1] Francesco Vasca, Luigi Iannelli, *Dynamics and control of switched electronic Systems*, Springer, London, 2012.
- [2] Yan Liu, Zegang Ye, *Study on harmonic analysis and error correction in synchro to digital conversion*, *Advanced Materials Research*, Vols. 225- 226, pp. 334-337, 2011.
- [3] Analog Devices, *Precision, Low Cost, High Speed, BiFET Op Amp AD711*, USA, 2002.
- [4] Analog Devices, *Fast, Precision Comparator AD790*, USA, 2002.
- [5] Maxim, *$\pm 15\text{kV}$ ESD-protected, Down to 10nA, 3.0V to 5.5V, Upto 1Mbps, True RS-232 Transceiver*, USA, 2003.
- [6] Altera, *MAX 3000A Programmable Logic Device Family*, USA, 2006.
- [7] Microchip, *PIC18(L)F2X/4XK22 datasheet*, USA, 2012.

CHAPTER 6

IMPLEMENTATION OF DIAGNOSTIC FEATURES

FOR SYNCHRO-TO-DIGITAL CONVERTER

CONTENTS:

- 6.1 Design of loss of signal detector
- 6.2 Design of stator terminal reversal connection detector
- 6.3 Conclusion
- References

This chapter presents the diagnostic features for Synchro-to-Digital Converter (SDC). They are (i) Loss Of Signal (LOS) detection and (ii) Reversal connection detection. If the synchro is not connected properly to the SDC, the output digital display of SDC shows an illogical value. To diagnose the inadvertent mistakes, an investigation is taken up for the incorporation of diagnostic features in the SDC.

The design of LOS detector and reversal connection detector mainly involves a monoshot. The pulse stretching operation of monoshot is mainly used to detect the cable disconnection and reversal connection detection between synchro and SDC. The connection between synchro and SDC is shown in figure 6.1. The R1, R2, S1, S2 and S3 terminals of synchro are connected to the RH, RL, S1, S2, and S3 inputs of the converter respectively. An excitation voltage is applied between R1 and R2 terminals of synchro and given as

$$V_{\text{Ref}}(t) = V \sin \omega t \quad (6.1)$$

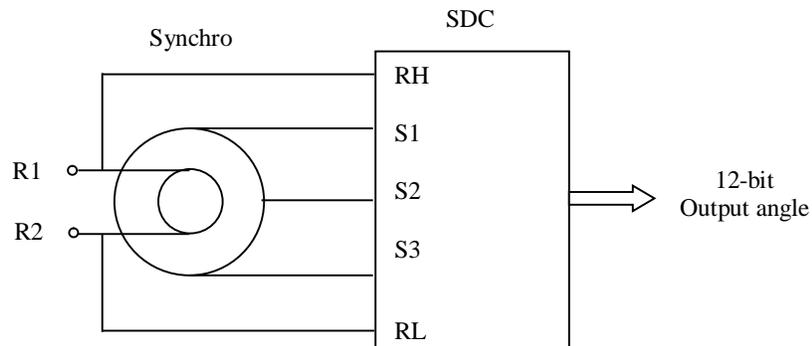


Figure 6.1: The connections between synchro and Synchro-to-Digital Converter (SDC). The terminals: R1, R2, S1, S2 and S3 of synchro are connected to RH, RL, S1, S2 and S3 terminals of SDC.

6.1 Design of loss of signal detector

6.1.1 Methodology

The block diagram of LOS detector is shown in figure 6.2. It consists of inverting amplifiers, zero crossing detectors and monoshots. The investigation of loss of signal detection is done using the phase voltage signals of synchro. The synchro is excited with a sinusoidal signal,

$V \sin\omega t$ then the induced phase voltage signals on three stator windings are given as

$$\left. \begin{aligned} V_{S1}(t) &= V \sin\omega t \cos(\theta+120^\circ) \\ V_{S2}(t) &= V \sin\omega t \cos(\theta) \\ V_{S3}(t) &= V \sin\omega t \cos(\theta+240^\circ) \end{aligned} \right\} \quad (6.2)$$

The main idea of the design is the generation of zero crossing signals for each stator terminal voltage of synchro. These signals are responsible for deciding the discontinuity of stator signals of synchro.

The output signals of synchro has a voltage swing of -25 V to +25 V and to operate these signals at analog electronic saturation levels, a voltage scaling stage is required. This is implemented by using operational amplifiers (AD711JN) [1]. There are three voltage scaling amplifiers in inverting configuration providing one fifth division for the input signals.

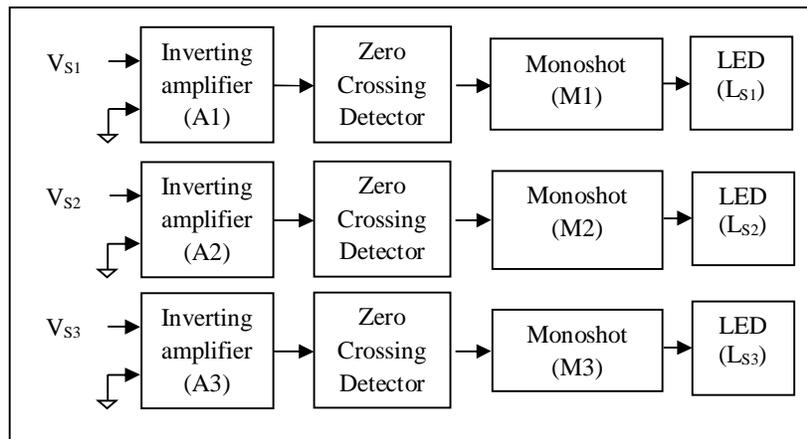


Figure 6.2: The block diagram of Loss Of Signal (LOS) detector. It takes synchro stator voltages: V_{S1} , V_{S2} and V_{S3} and gives cable disconnection information through LED indications.

The operational amplifier based comparator; AD790 acts as zero crossing detector to generate zero crossing outputs for synchro signals [2]. Since the monoshots accepts the voltage levels 0 V to +5 V, the voltage translator is needed to convert analog electronics operating voltage levels (-12 V to +12 V) to digital electronics operating voltage levels (0 V to +5 V). Hence, the comparator itself serves as a voltage translator.

In this method, it is required to generate high or low voltage level to indicate the status of input signal. As the monoshot has an application in pulse stretching, 100% duty cycle is possible by application of an input signal such that it can generate high voltage level at the output. A single monoshot is capable of generating pulses of desired width, and the basic output pulse width is determined by selection of an external resistor and a capacitor [3]. The output pulse width T_w is defined as follows,

$$T_w = K R_{ext} C_{ext} (1 + 0.7 / R_{ext}) \quad (6.3)$$

where R_{ext} is external resistor, C_{ext} is external capacitor, $K = 0.28$

Since the signals V_{S1} , V_{S2} and V_{S3} have the time period of 20 ms, the external resistance of 10 k and capacitance of 7.5 μ F were chosen for monoshot circuit such that a continuous high logic state is maintained for 20 ms. The timing diagram of the input and output signals of monoshot is shown in figure 6.3. From timing diagram, it is observed that the input signal is available for time duration of 60 ms. Hence, the output of monoshot stays at high level for 60 ms and then goes to low level. The output of monoshot again goes to high level whenever it detects rising edge of input signal. The monoshot turn the LED ON when the input signal is disconnected and OFF when connected firmly to the SDC.

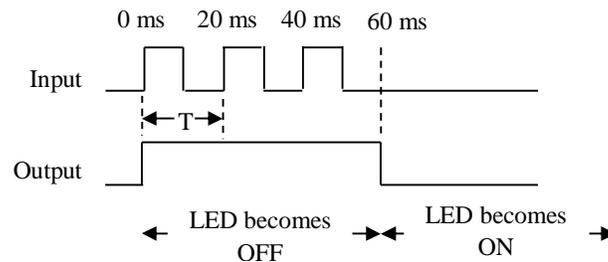


Figure 6.3: Monoshot timing diagram with input and output signals. The signal is available for the first 60 ms and absent afterwards.

6.1.2 Implementation

The schematic circuit of LOS detector is shown in figure 6.4. The availability and non-availability of signal is represented by switch (sw) in closed and opened condition

respectively. In this circuit, the synchro phase voltage signals V_{S1} , V_{S2} and V_{S3} are applied through sw1, sw2 and sw3 respectively.

The outputs of the voltage scaling stage are applied to the zero crossing stage to obtain zero crossing signals. This zero crossing detector stage itself acts as voltage translator between the voltage scaling stage and the monoshot stage. The zero crossing signals are passed through the monoshots to generate high or low voltage levels. There are three LEDs (L_{S1} , L_{S2} and L_{S3}) at the outputs of monoshots, which indicates the loss of input signals to the SDC.

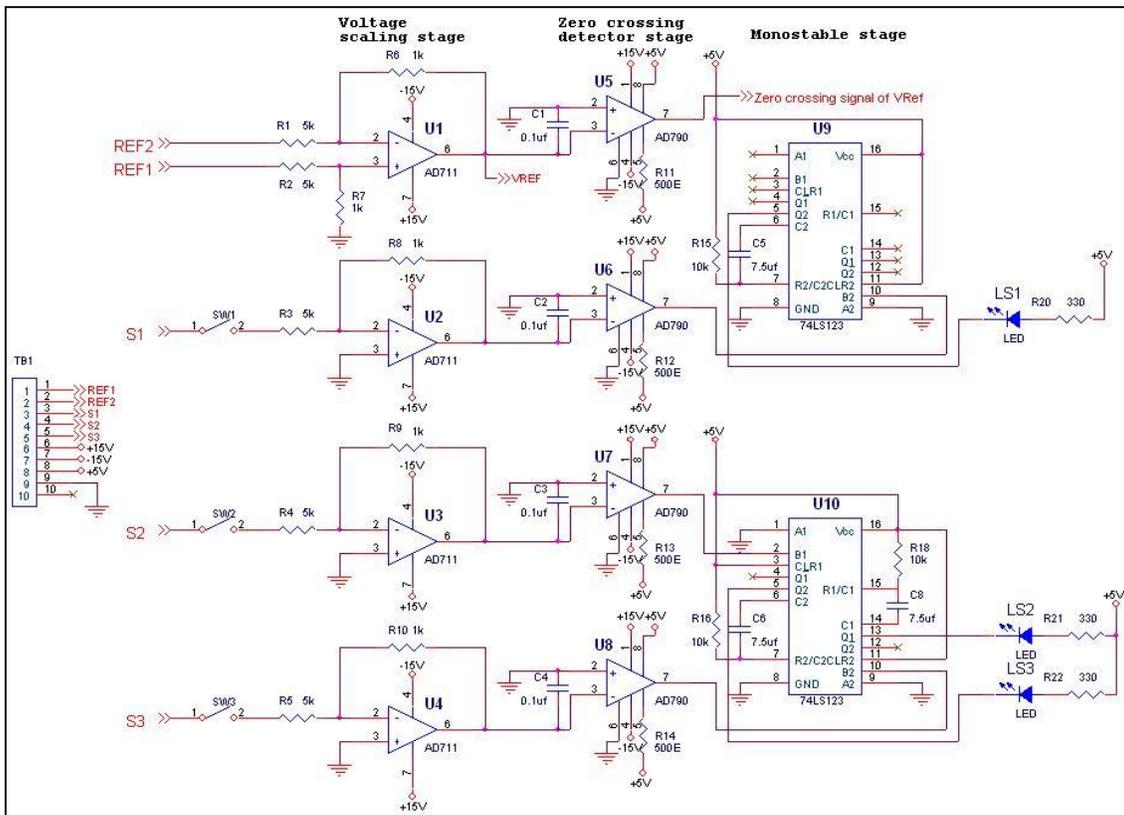
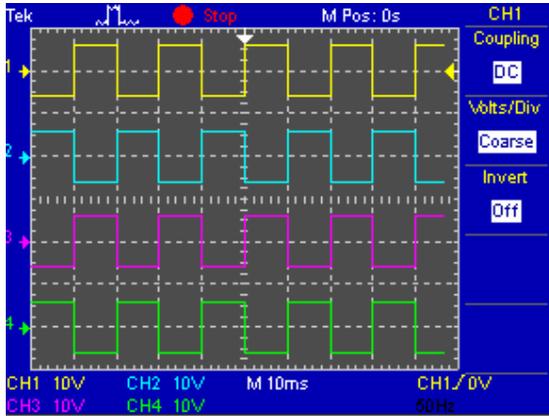


Figure 6.4: Schematic circuit of loss of signal detector. The voltage scaling stage makes the synchro signals to operate at analog electronic saturation levels. The zero crossing detector stage gives zero crossing signals of phase voltages: V_{S1} , V_{S2} , V_{S3} and acts as voltage translator. The monoshot stage gives high or low voltage levels to LEDs to indicate stator signals disconnection between synchro and SDC.

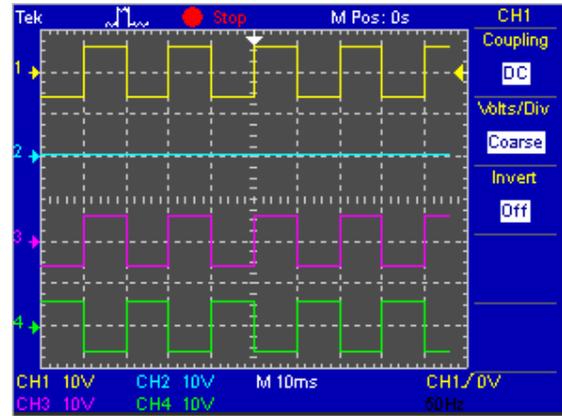
6.1.3 Experimental results

The AC supply is stepped down from 230 V_{rms} to 24 V_{rms} for safe experimentation. A sinusoidal signal of 24 V_{rms} with a frequency of 50 Hz is used to excite the synchro. The zero

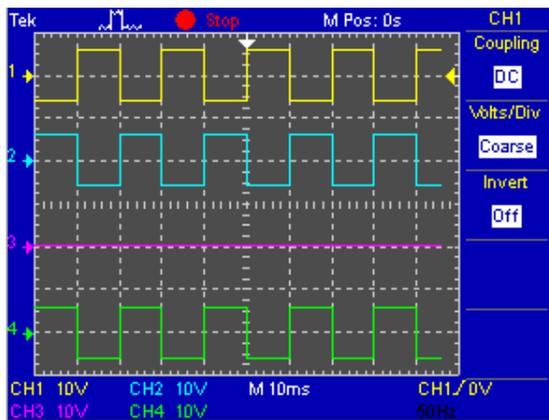
crossing outputs are captured when the shaft of the synchro is at mechanical zero position. At this position, the signals V_{S1} , V_{S3} are out of phase and the signal V_{S2} is in phase with V_{Ref} . The outputs of zero crossing detector stage are sent to the monoshot stage. Figure 6.5 shows the zero crossing signals of excitation and synchro signals for possible disconnections between synchro and SDC.



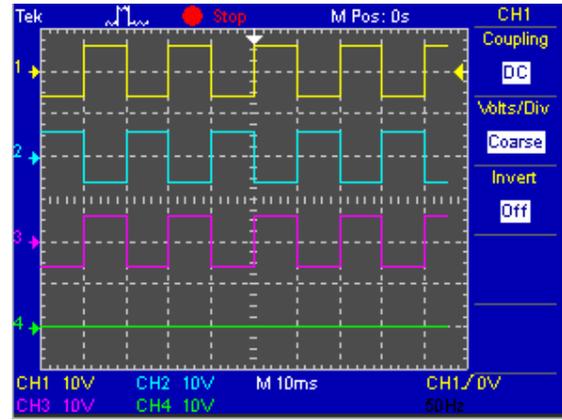
(a) Presence of zero crossing signals of V_{Ref} (yellow), V_{S1} (cyan), V_{S2} (pink), V_{S3} (green) when synchro and SDC are connected firmly.



(b) Absence of zero crossing signal of V_{S1} (pink) when S1 terminal is disconnected between synchro and SDC.



(c) Absence of zero crossing signal of V_{S2} (cyan) when S2 terminal is disconnected between synchro and SDC.



(d) Absence of zero crossing signal of V_{S3} (green) when S3 terminal is disconnected between synchro and SDC.

Figure 6.5: Output signals of zero crossing detector stage

Notes: Channel 1, 2, 3, 4 correspond to the zero crossing output of V_{Ref} , V_{S1} , V_{S2} and V_{S3} respectively.

The LEDs are in sink mode i.e. the anode terminal is connected to positive power supply and cathode terminal is connected to output of monoshot. Thus, LED becomes OFF when there is a high voltage signal from the monoshot, otherwise it is ON. It is experimentally verified for all possible ways of loss of synchro signals to the SDC. Table 6.1 shows the LED indications for different signal losses between the synchro and the SDC.

Table 6.1: Summary of LOS detector indications

Stator voltages	V_{S1} (sw1 opened)	V_{S2} (sw2 opened)	V_{S3} (sw3 opened)
LEDs			
L_{S1}	ON	OFF	OFF
L_{S2}	OFF	ON	OFF
L_{S3}	OFF	OFF	ON

6.2 Design of reversal connection detector

6.2.1 Methodology

The block diagram of the stator terminal reversal connection detector between synchro and SDC is shown figure 6.6. It consists of phase-to-line voltage converter, zero crossing detectors, clock signal generator and a flip flop register bank.

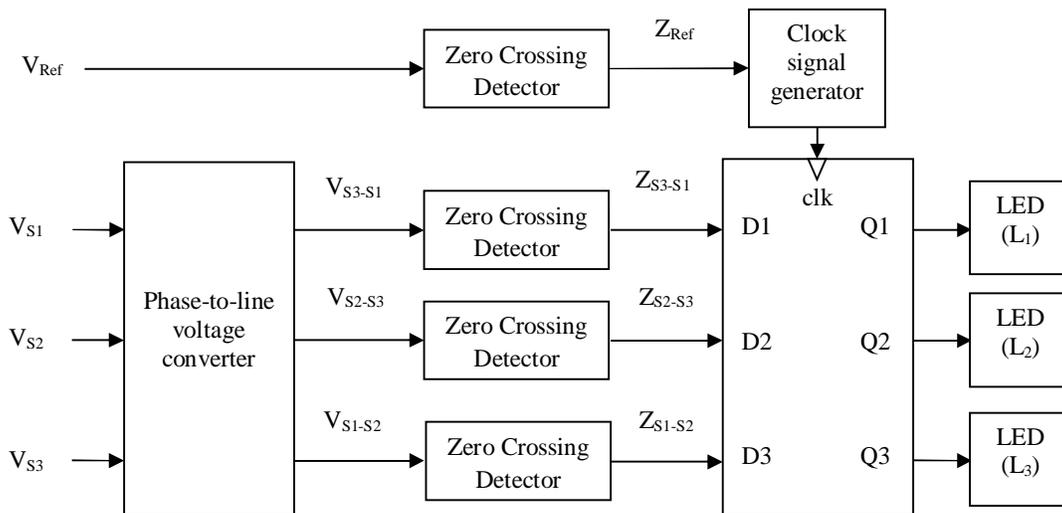


Figure 6.6: Block diagram of the stator terminal reversal connection detector.

The analysis of stator terminal reversal connection detection is done using the line voltage signals of synchro. The line voltages are obtained by considering voltage between the terminals: S3 and S1; S2 and S3; S1 and S2. The phase voltages of synchro V_{S1} , V_{S2} , V_{S3} are converted into line voltages V_{S3-S1} , V_{S2-S3} , V_{S1-S2} using phase-to-line voltage converter. The phase-to-line voltage converter is designed using differential amplifiers. The expressions of line voltages are given as

$$\left. \begin{aligned} V_{S3-S1}(t) &= V \sin t \sin \\ V_{S2-S3}(t) &= V \sin t \sin(+120^\circ) \\ V_{S1-S2}(t) &= V \sin t \sin(+240^\circ) \end{aligned} \right\} \quad (6.4)$$

The main idea of the design is to generate the zero crossing signals for each stator voltage of synchro and a clock signal from the excitation signal, V_{Ref} . The phase relationship between excitation signal and synchro signals is used to find the stator terminal reversal connections. The possible reversal connections along with correct connections are described using the cases shown in table 6.2. The details of each case are described below.

Table 6.2: List of connections between the synchro and SDC

Case	Description	Connections between synchro and SDC	
		Synchro terminals	SDC terminals
i	Correctly Connected	S1 S2 S3	→ → → S1 S2 S3
ii	S1-S2 swapped	S1 S2 S3	→ → → S2 S1 S3
iii	S1-S3 swapped	S1 S2 S3	→ → → S3 S2 S1
iv	S2-S3 swapped	S1 S2 S3	→ → → S1 S3 S2
v	S1, S2, S3 swapped	S1 S2 S3	→ → → S3 S1 S2

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Case (i): Synchro and SDC are connected correctly.

Let V_{Ref} is applied as excitation signal and the trigonometric simplification to obtain the line voltages of synchro is as follows

$$\begin{aligned}
 V_{S3-S1} &= V \sin t \cos(+240^0) \text{ ó } V \sin t \cos(+120^0) \\
 &= V \sin t \{[\cos \cos240^0 \text{ ó } \sin \sin240^0] - [\cos \cos120^0 \text{ ó } \sin \sin120^0]\} \\
 &= \zeta 3V \sin t \sin \\
 &= \zeta 3V \sin t \sin \\
 &= V^1 \sin t \qquad (6.5)
 \end{aligned}$$

When the shaft of synchro is at 0^0 , 60^0 and 120^0 position, V_{S3-S1} , V_{S2-S3} and V_{S1-S2} become zero respectively. In addition, V_{S2-S3} becomes zero when the shaft of synchro is at 240^0 position. Hence a reference shaft angle other than these values, say $= 20^0$ is considered for entire analysis. So from equations (6.1) and (6.5), it is noted that V_{Ref} and V_{S3-S1} are in phase.

$$\begin{aligned}
 V_{S2-S3} &= V \sin t \cos - V \sin t \cos(+240^0) \\
 &= V \sin t \{ \cos - [\cos \cos240^0 \text{ ó } \sin \sin240^0] \} \\
 &= \zeta 3V \sin t \sin(+120^0) \\
 &= V^1 \sin t \qquad (6.6)
 \end{aligned}$$

From equations (6.1) and (6.6), it is noted that V_{Ref} and V_{S2-S3} are in phase.

$$\begin{aligned}
 V_{S1-S2} &= V \sin t \cos(+120^0) - V \sin t \cos \\
 &= V \sin t \{ [\cos \cos120^0 \text{ ó } \sin \sin120^0] - \cos \} \\
 &= - V \sin t [1.5\cos + 0.866 \sin] \\
 &= \zeta 3V \sin t \sin(+240^0) \\
 &= - V^1 \sin t \qquad (6.7)
 \end{aligned}$$

From equations (6.1) and (6.7), it is noted that V_{Ref} and V_{S1-S2} are out of phase.

Case (ii): S1 and S2 terminals of synchro and SDC are reversed.

$$V_{S3-S1} = V_{S3-S2} = V \sin t \cos(+240^0) - V \sin t \cos$$

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$$\begin{aligned}
&= V \sin t [\cos \cos 240^\circ \acute{o} \sin \sin 240^\circ - \cos] \\
&= V \sin t [-1.5 \cos + 0.866 \sin] \\
&= -\zeta 3V \sin t \sin(+120^\circ) \\
&= -V^1 \sin t \tag{6.8}
\end{aligned}$$

From equations (6.1) and (6.8), it is noted that V_{Ref} and V_{S3-S1} are out of phase.

$$\begin{aligned}
V_{S2-S3} = V_{S1-S3} &= V \sin t \cos(+120^\circ) \acute{o} V \sin t \cos(+240^\circ) \\
&= V \sin t \{[\cos \cos 120^\circ \acute{o} \sin \sin 120^\circ] - [\cos \cos 240^\circ \acute{o} \sin \sin 240^\circ]\} \\
&= -\zeta 3V \sin t \sin \\
&= -V^1 \sin t \tag{6.9}
\end{aligned}$$

From equations (6.1) and (6.9), it is noted that V_{Ref} and V_{S2-S3} are out of phase.

$$\begin{aligned}
V_{S1-S2} = V_{S2-S1} &= V \sin t \cos - V \sin t \cos(+120^\circ) \\
&= V \sin t \{\cos - [\cos \cos 120^\circ \acute{o} \sin \sin 120^\circ]\} \\
&= V \sin t [1.5 \cos + 0.866 \sin] \\
&= \zeta 3V \sin t \sin(+240^\circ) \\
&= V^1 \sin t \tag{6.10}
\end{aligned}$$

From equations (6.1) and (6.10), it is noted that V_{Ref} and V_{S1-S2} are in phase.

Case (iii): S1 and S3 terminals of synchro and SDC are reversed.

$$\begin{aligned}
V_{S3-S1} = V_{S1-S3} &= V \sin t \cos(+120^\circ) - V \sin t \cos(+240^\circ) \\
&= V \sin t \{[\cos \cos 120^\circ \acute{o} \sin \sin 120^\circ] - [\cos \cos 240^\circ \acute{o} \sin \sin 240^\circ]\} \\
&= -\zeta 3V \sin t \sin \\
&= -V^1 \sin t \tag{6.11}
\end{aligned}$$

From equations (6.1) and (6.11), it is noted that V_{Ref} and V_{S3-S1} are out of phase.

$$\begin{aligned}
V_{S2-S3} = V_{S2-S1} &= V \sin t \cos - V \sin t \cos(+120^\circ) \\
&= V \sin t \{ \cos - [\cos \cos 120^\circ \acute{o} \sin \sin 120^\circ]\} \\
&= V \sin t [1.5 \cos + 0.866 \sin]
\end{aligned}$$

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$$\begin{aligned}
 &= \zeta 3V \sin t \sin(+240^\circ) \\
 &= V^1 \sin t \quad (6.12)
 \end{aligned}$$

From equations (6.1) and (6.12), it is noted that V_{Ref} and V_{S2-S3} are in phase.

$$\begin{aligned}
 V_{S1-S2} &= V_{S3-S2} = V \sin t \cos(+240^\circ) - V \sin t \cos \\
 &= V \sin t \{ [\cos \cos 240^\circ \text{ ó } \sin \sin 240^\circ] - \cos \} \\
 &= -\zeta 3V \sin t \sin(+120^\circ) \\
 &= -V^1 \sin t \quad (6.13)
 \end{aligned}$$

From equations (6.1) and (6.13), it is noted that V_{Ref} and V_{S1-S1} are out of phase.

Case (iv): S2 and S3 terminals of synchro and SDC are reversed.

$$\begin{aligned}
 V_{S3-S1} &= V_{S2-S1} = V \sin t \cos - V \sin t \cos(+120^\circ) \\
 &= V \sin t \{ \cos - [\cos \cos 120^\circ \text{ ó } \sin \sin 120^\circ] \} \\
 &= V \sin t [1.5\cos + 0.866 \sin] \\
 &= -\zeta 3V \sin t \sin(+240^\circ) \\
 &= V^1 \sin t \quad (6.14)
 \end{aligned}$$

From equations (6.1) and (6.14), it is noted that V_{Ref} and V_{S1-S2} are in phase.

$$\begin{aligned}
 V_{S2-S3} &= V_{S3-S2} = V \sin t \cos(+240^\circ) - V \sin t \cos \\
 &= V \sin t \{ [\cos \cos 240^\circ \text{ ó } \sin \sin 240^\circ] - \cos \} \\
 &= -\zeta 3V \sin t \sin(+120^\circ) \\
 &= -V^1 \sin t \quad (6.15)
 \end{aligned}$$

From equations (6.1) and (6.15), it is noted that V_{Ref} and V_{S2-S3} are out of phase.

$$\begin{aligned}
 V_{S1-S2} &= V_{S1-S3} = V \sin t \cos(+120^\circ) - V \sin t \cos(+240^\circ) \\
 &= V \sin t \{ [\cos \cos 120^\circ \text{ ó } \sin \sin 120^\circ] \text{ ó } [\cos \cos 240^\circ \text{ ó } \sin \sin 240^\circ] \} \\
 &= -\zeta 3V \sin t \sin \\
 &= -V^1 \sin t \quad (6.16)
 \end{aligned}$$

From equations (6.1) and (6.16), it is noted that V_{Ref} and V_{S2-S3} are out of phase.

Case (v): S1, S2 and S3 terminals of synchro and SDC are reversed.

$$\begin{aligned}
 V_{S3-S1} &= V_{S2-S3} = V \sin t \cos - V \sin t \cos(+240^0) \\
 &= V \sin t \{ \cos - [\cos \cos 240^0 \acute{o} \sin \sin 240^0] \} \\
 &= \zeta 3V \sin t \sin(+120^0) \\
 &= V^1 \sin t \quad (6.17)
 \end{aligned}$$

From equations (6.1) and (6.17), it is noted that V_{Ref} and V_{S3-S1} are in phase.

$$\begin{aligned}
 V_{S2-S3} &= V_{S1-S2} = V \sin t \cos(+120^0) - V \sin t \cos \\
 &= V \sin t \{ [\cos \cos 120^0 \acute{o} \sin \sin 120^0] - \cos \} \\
 &= - V \sin t [1.5 \cos + 0.866 \sin] \\
 &= \zeta 3V \sin t \sin(+240^0) \\
 &= - V^1 \sin t \quad (6.18)
 \end{aligned}$$

From equations (6.1) and (6.18), it is noted that V_{Ref} and V_{S2-S3} are out of phase.

$$\begin{aligned}
 V_{S1-S2} &= V_{S3-S1} = V \sin t \cos(+240^0) \acute{o} V \sin t \cos(+120^0) \\
 &= V \sin t \{ [\cos \cos 240^0 \acute{o} \sin \sin 240^0] - [\cos \cos 120^0 \acute{o} \sin \sin 120^0] \} \\
 &= \zeta 3V \sin t \sin \\
 &= V^1 \sin t \quad (6.19)
 \end{aligned}$$

From equations (6.1) and (6.19), it is noted that V_{Ref} and V_{S1-S2} are in phase.

Based on above analysis a clock signal is required to decide whether the synchro line voltages are in phase or out of phase with the excitation signal. The detail design describing the generation of clock signal from the excitation voltage is explained in quadrant determination of chapter 4. The zero crossing detectors generate the zero crossing signals of line voltages. The zero crossing signals: Z_{S3-S1} , Z_{S2-S3} , Z_{S1-S2} and clock signal applied as inputs to the flip flop register bank of three D flip flops.

6.2.2 Implementation

The schematic implementation of stator terminal reversal connection detector is shown in figure 6.7. The reversal connection between synchro and SDC is performed using switches (sw4f sw12). The switches sw9, sw4, sw11 are closed when synchro and SDC are connected correctly and the phase-to-line converter gives V_{S3-S1} , V_{S2-S3} , V_{S1-S2} . The zero crossing detector stage implemented by operational amplifier based comparators AD790. The dual monoshot, 74LS123 based clock signal generator gives clock input to the flip flops. Based on the rising edge of the clock input, the flip flops generate high voltage level when V_{ref} and synchro line voltages are in phase otherwise gives low voltage level. The LEDs are connected to the outputs of flip flops and becomes ON when flip flop output is low; OFF when flip flop output is high.

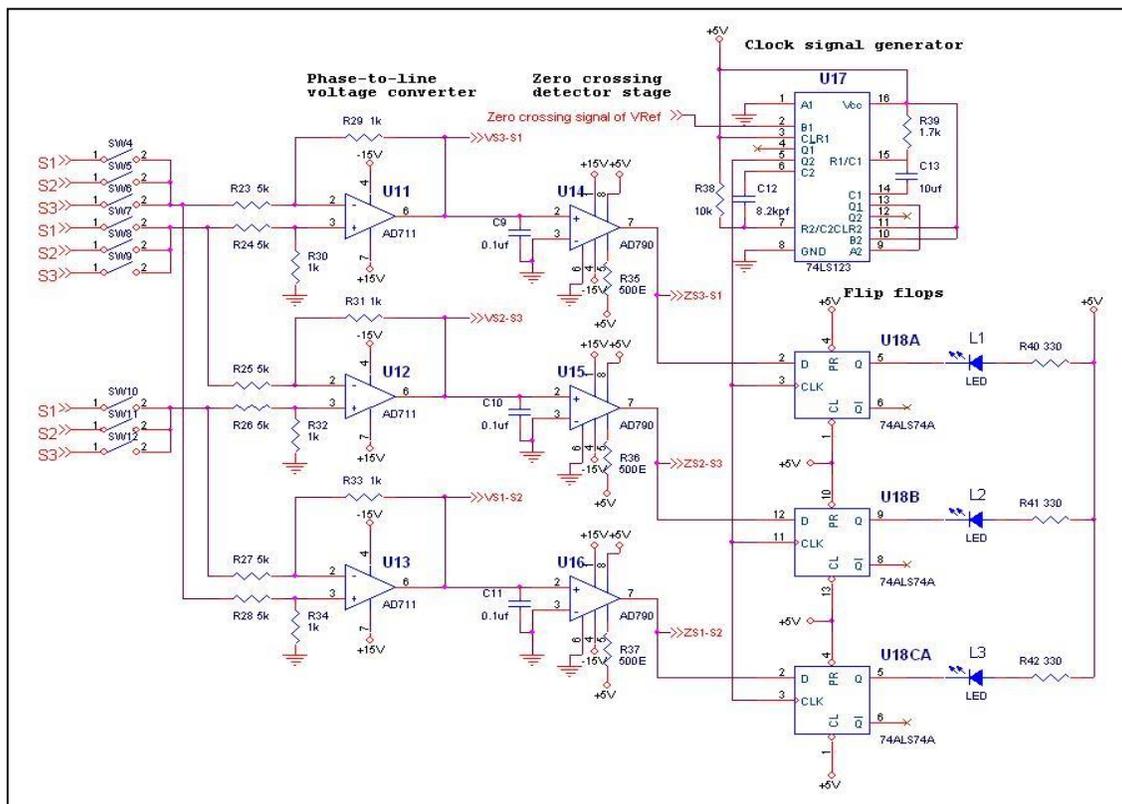


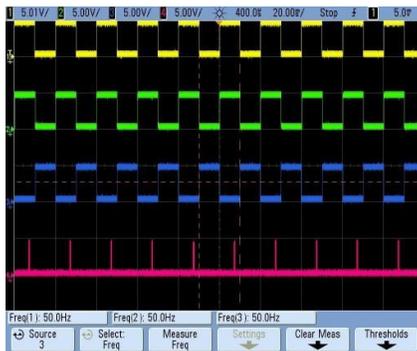
Figure 6.7: Schematic circuit of the stator terminal reversal connection detector. The phase-to-line converter gives equivalent line voltages of synchro. The zero crossing detector stage gives zero crossing signals of line voltages: V_{S3-S1} , V_{S2-S3} , V_{S1-S2} and acts as voltage translator. The flip flops give

high or low voltage levels to LEDs to indicate stator terminals reversal connection between synchro and SDC.

6.2.3 Experimental results

Case (i): Synchro and SDC terminals are connected correctly.

In this case the S1, S2, S3 terminals of synchro are connected to S1, S2, S3 terminals of SDC. The line voltages of synchro: V_{S3-S1} , V_{S2-S3} and V_{S1-S2} are converted into zero crossing signals and sent to the flip flops. The signal derived from the excitation is used as clock input to the flip flops. The zero crossing signals of synchro: Z_{S3-S1} , Z_{S2-S3} , Z_{S1-S2} are connected to first, second and third flip flop respectively. The input-outputs of first, second and third flip flops are denoted as D_1 , Q_1 ; D_2 , Q_2 ; and D_3 , Q_3 respectively. The flip flop outputs: Q_1 , Q_2 , Q_3 connected to the LEDs: L_1 , L_2 and L_3 respectively. From the analysis V_{S3-S1} , V_{S2-S3} are in phase and V_{S1-S2} is out of phase with V_{Ref} . Figure 6.8 shows zero crossing signals of synchro and flip flop output voltage levels along with the clock signal (representative of excitation signal) when the synchro and SDC terminals are connected correctly. From the analysis, V_{S3-S1} , V_{S2-S3} are in phase and V_{S1-S2} is out of phase with V_{ref} . The flip flop outputs: Q_1 , Q_2 becomes high for Z_{S3-S1} , Z_{S2-S3} and Q_3 becomes low for Z_{S1-S2} . Hence, the LEDs: L_1 , L_2 becomes OFF and L_3 becomes ON.



(a) Zero crossing signals, Z_{S3-S1} (yellow), Z_{S2-S3} (green), Z_{S1-S2} (blue) and clock signal (pink)



(b) Output voltage of flip flops: Q_1 (yellow) is at 5 V, Q_2 (green) is at 5 V, Q_3 (blue) is at 0 V and clock signal (pink)

Figure 6.8: Zero crossing signals and flip flops output when the synchro and SDC terminals are connected correctly.

Case (ii): S1 and S2 terminals of synchro and SDC are reversed.

In this case the S1, S2 terminals of synchro are connected to S2, S1 terminals of SDC respectively. Figure 6.9 shows zero crossing signals of synchro and flip flop output voltage levels along with the clock signal when S1 and S2 terminals of synchro and SDC are reversed. From the analysis, V_{S3-S1} , V_{S2-S3} are out of phase and V_{S1-S2} is in phase with V_{ref} . The flip flop outputs: Q_1 , Q_2 becomes low for Z_{S3-S1} , Z_{S2-S3} and Q_3 becomes high for Z_{S1-S2} . Hence, the LEDs: L_1 , L_2 becomes ON and L_3 becomes OFF.



(a) Zero crossing signals, Z_{S3-S1} (yellow), Z_{S2-S3} (green), Z_{S1-S2} (blue) and clock signal (pink)

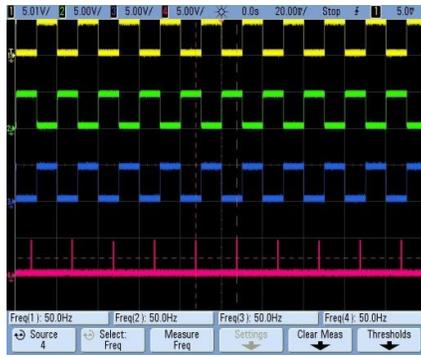


(b) Output voltage of flip flops: Q_1 (yellow) is at 0 V, Q_2 (green) is at 0 V, Q_3 (blue) is at 5 V and clock signal (pink)

Figure 6.9: Zero crossing signals and flip flops output when S1 and S2 terminals of synchro and SDC are reversed.

Case (iii): S1 and S3 terminals of synchro and SDC are reversed.

In this case the S1, S3 terminals of synchro are connected to S3, S1 terminals of SDC respectively. From the analysis V_{S3-S1} , V_{S1-S2} are out of phase and V_{S2-S3} is in phase with V_{ref} . Figure 6.10 shows zero crossing signals of synchro and flip flop output voltage levels along with the clock signal when S1 and S3 terminals of synchro and SDC are reversed. From the analysis, V_{S3-S1} , V_{S1-S2} are out of phase and V_{S2-S3} is in phase with V_{ref} . The flip flop outputs: Q_1 becomes low for Z_{S3-S1} , Q_2 becomes high for Z_{S2-S3} and Q_3 becomes low for Z_{S1-S2} . Hence, the LEDs: L_1 , L_3 becomes ON and L_2 becomes OFF.



(a) Zero crossing signals, Z_{S3-S1} (yellow), Z_{S2-S3} (green), Z_{S1-S2} (blue) and clock signal (pink)

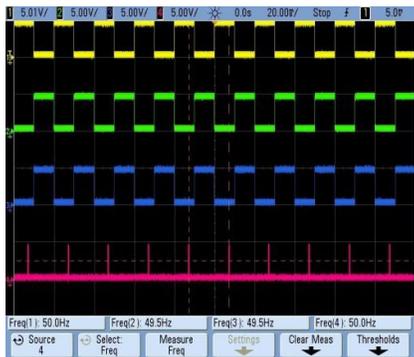


(b) Output voltages of flip flops: Q_1 (yellow) is at 0 V, Q_2 (green) is at 5 V, Q_3 (blue) is at 0 V and clock signal (pink)

Figure 6.10: Zero crossing signals and flip flops output when S1 and S3 terminals of synchro and SDC are reversed.

Case (iv): S2 and S3 terminals of synchro and SDC are reversed.

In this case the S2, S3 terminals of synchro are connected to S3, S2 terminals of SDC respectively. From the analysis V_{S3-S1} , are in phase and V_{S2-S3} , V_{S1-S2} are out of phase with V_{Ref} . Figure 6.11 shows zero crossing signals of synchro and flip flop output voltage levels along with the clock signal S2 and S3 terminals of synchro and SDC are reversed. From the analysis, V_{S3-S1} , are in phase and V_{S2-S3} , V_{S1-S2} are out of phase with V_{ref} . The flip flop outputs: Q_1 becomes high for Z_{S3-S1} , Q_2 , Q_3 becomes low for Z_{S2-S3} , Z_{S1-S2} . Hence, the LEDs: L_1 becomes OFF and L_2 , L_3 becomes ON.



(a) Zero crossing signals, Z_{S3-S1} (yellow), Z_{S2-S3} (green), Z_{S1-S2} (blue) and clock signal (pink)



(b) Output voltage of flip flops: Q_1 (yellow) is at 5 V, Q_2 (green) is at 0 V, Q_3 (blue) is at 0 V and clock signal (pink)

Figure 6.11: Zero crossing signals and flip flops output when S2 and S3 terminals of synchro and SDC are reversed.

Case (v): S1, S2 and S3 terminals of synchro and SDC are reversed.

In this case the S1, S2, S3 terminals of synchro are connected to S3, S1, S2 terminals of SDC. From the analysis V_{S3-S1} , V_{S1-S2} are in phase and V_{S2-S3} is out of phase with V_{Ref} . Figure 6.12 shows zero crossing signals of synchro and flip flop output voltage levels along with the clock signal when S1, S2 and S3 terminals of synchro and SDC are reversed. From the analysis, V_{S3-S1} , V_{S1-S2} are in phase and V_{S2-S3} is out of phase with V_{ref} . The flip flop outputs: Q_1 becomes high for Z_{S3-S1} , Q_2 becomes low for Z_{S2-S3} and Q_3 becomes high for Z_{S1-S2} . Hence, the LEDs: L_1 , L_3 becomes OFF and L_2 becomes ON.



(a) Zero crossing signals, Z_{S3-S1} (yellow), Z_{S2-S3} (green), Z_{S1-S2} (blue) and clock signal (pink)



(b) Output voltage of flip flops: Q_1 (yellow) is at 5 V, Q_2 (green) is at 0 V, Q_3 (blue) is at 5 V and clock signal (pink)

Figure 6.12: Zero crossing signals and flip flops output when S1, S2 and S3 terminals of synchro and SDC are reversed.

The synchro signal phase relationship with excitation signal and LED indications for various reversal connections between synchro and SDC is shown in table 6.3.

Table 6.3: Summary of LED indications of stator terminal reversal connection detector

Case	Description	V_{Ref} & V_{S3-S1}	V_{Ref} & V_{S2-S3}	V_{Ref} & V_{S1-S2}	LEDs		
					L_1	L_2	L_3
i	Correctly Connected (S1→ S1, S2→ S2, S3→ S3)	In phase	In phase	Out of phase	OFF	OFF	ON
ii	S1-S2 swapped	Out of phase	Out of phase	In phase	ON	ON	OFF
iii	S1-S3 swapped	Out of phase	In phase	Out of phase	ON	OFF	ON
iv	S2-S3 swapped	In phase	Out of phase	Out of phase	OFF	ON	ON
v	S1, S2, S3 swapped (S1→ S3, S2→ S1, S3→ S2)	In phase	Out of phase	In phase	OFF	ON	OFF

6.3 Conclusion

This study presents the design and functional verification of loss of signal detector and stator terminal reversal connection detector for the SDC. The realization of these detectors requires simple and optimum number of components. Hence it provides high reliability for the SDC. Since these detectors have LED indications at output side, one can easily locate the fault either because of cable disconnection or stator terminal reversal connection between synchro and SDC. The open line detection and reversal connection detection are useful at the commissioning stage of systems, where the synchro is deployed as positional sensor. Further, this design approach can be applied to other converters like resolver-to-digital converters.

References

[1] Analog Devices, "Precision, Low cost, High speed, BiFET Op Amp AD711," USA,

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2002.

[2] Analog Devices, "Fast, Precision Comparator AD790," USA, 2002.

[3] Fairchild Semiconductor Corporation, "DM74LS123 Dual Retriggerable One-Shot with Clear and Complementary Outputs," USA, 2000.

CHAPTER 7

SUMMARY AND FUTURE SCOPE

CONTENTS:

7.1 Summary

7.2 Future scope

The work presented in this thesis covers the study of synchro in terms of parameters, non ideal behavior and also aims the development of Synchro-to-Digital Converter (SDC). The summary and future scope of the research work is as follows:

7.1 Summary

The fuel handling mechanisms of nuclear reactor are discussed to understand the operation and scope of synchro. Synchro is an important component in motion and position sensing applications. The mathematical study of synchro is carried out to emulate functional behavior of the synchro. A study on non-ideal characteristics of synchro is taken up. A quantitative analysis of the same is presented to estimate the angular error occurring due to non ideal behavior of synchro.

A MATLAB/Simulink based simulation model is developed for SDC to compute the rotation angle and speed of rotor of synchro. This method mainly involves dual stage monoshot to extract the peak amplitude levels as the angular position information embedded into the envelope of output signals of synchro. However, the monoshot employs resistor and capacitor as external components to generate sampling signal for S&H circuit. Due to temperature variations and drifts in resistance, it is difficult to generate sampling pulses exactly at peak amplitude instances of synchro signals. Hence the accuracy in measurement of shaft angle comes down.

To eliminate the external factors on the analog components, a digital detection method of extracting the peak amplitude information is proposed. This design comprises of electronic scott-T circuit, digital peak detectors, latching & reset signals generation circuits, flip flops based quadrant detector and a microcontroller. The digital peak detector consists of a comparator, 10-bit counter and 10-bit DAC. This method requires stringent and high speed DACs to implement digital peak detectors. Further, the DAC is operated with a fixed

reference voltage; it may not give good resolution for output shaft angle because the output signals of synchro are continuously time varying signals from small to high voltage swing.

A new method is proposed using the concept of pulse width modulation for the estimation of synchro shaft angle. The basic idea of the scheme is the linear evaluation of peak amplitudes of scott-T signals using Time Duration Windows (TDW) and division of TDWs followed by the inverse tangent operation to get rotor shaft angle. The experimental results are demonstrated using a prototype SDC developed in-house.

The diagnostic features such as loss of signal detection and stator terminal reversal connection detection between synchro and SDC are implemented. The pulse stretching feature of monoshot is used to turn the LED ON when the input signals is disconnected and OFF when connected firmly to the SDC. The phase relationship analysis between line voltages of synchro and excitation voltage gives the idea to design a circuit which detects the reversal connection through corresponding LED indications.

7.2 Future scope

The prognosis of synchro failure is another focus area, where it provides information on the status of faults severity, its progression and time to failure.

The synchro and associated electronics like SDC are used increasingly in industrial motor drives and aircraft systems. Hence, the research in this area can be encouraged. The methods and analysis presented in this thesis gives insight on synchro and SDC. The present study can be applied to high frequency operated synchros to get appreciable resolution and tracking rate for high accuracy and high speed applications.

Further scope exists in the transmission of synchro shaft angle information to distant places. For transmission of synchro outputs to SDC which is sitting at far, it is advisable to use wireless connection instead of physical wiring. Hence a wireless communication can be established between synchro and SDC for various applications.

APPENDICES

A

Electronic scott-T simplification

Consider the stator output equations of a synchro

$$V_{S3 - S1} = V \sin(\omega t) \sin\theta \quad (A1)$$

$$V_{S2 - S3} = V \sin(\omega t) \sin(\theta + 120^\circ) \quad (A2)$$

$$V_{S1 - S2} = V \sin(\omega t) \sin(\theta + 240^\circ) \quad (A3)$$

From the equation (A1), it can be noticed that $V_{S3 - S1}$ directly gives one of the outputs of electronic scott-T.

$$V_S = V \sin(\omega t) \sin\theta \quad (A4)$$

For evaluating $V \sin(\omega t) \cos\theta$, equations (A2) and (A3) are manipulated. Consider the following manipulations,

$$(A2) - (A3) = V \sin(\omega t) ((\sin\theta \cos(120^\circ) + \cos\theta \sin(120^\circ)) - (\sin\theta \cos(240^\circ) + \cos\theta \sin(240^\circ))).$$

$$\text{Thus } V \sin(\omega t) (-1/2 \sin\theta + \sqrt{3}/2 \cos\theta + 1/2 \sin\theta + \sqrt{3}/2 \cos\theta) = V \sqrt{3} \sin(\omega t) \cos\theta.$$

Hence the scaling of $1/\sqrt{3}$ is done to get,

$$V_C = V \sin(\omega t) \cos\theta \quad (A5)$$

The equations (A4) and (A5) represent scott-T output signals.

B

8051 microcontroller software code

Microcontroller software code reads two sets of 10-bit digital data along with quadrant bits and calculates synchro shaft angle.

```

#include<reg51.h>
#include <math.h>
float atan2 (float,float); /* function prototype for inverse tangent */
void dec2bin(unsigned int);/* function prototype for decimal to binary conversion
*/

unsigned int i;
sbit qs= P3^0; /* quadrant detector bits declaration */
sbit qc= P3^1;
bit t[10];
sbit t[0]= P2^0; /* assigning output shaft angle to i/o pins */
sbit t[1]= P2^1;
sbit t[2]= P2^2;
sbit t[3]= P2^3;
sbit t[4]= P2^4;
sbit t[5]= P2^5;
sbit t[6]= P2^6;
sbit t[7]= P2^7;
sbit t[8]= P3^2;
sbit t[9]= P3^3;

void main(void)
{
unsigned char x,x1,x2,y,y1,y2;
float w,z,m;
TMOD=0x20; /* set timer1 in 8 bit auto-reload timer mode */
SCON=0x50; /* initialize serial communication */
TH1=0xFD; /* load timer 1 to generate baud rate of 9.6kbps */
TR1=1; /* start timer1 */
while(1)
{
x1=P0; /* reading of sin(theta) */
x2=P3;
x2 = x2 & 11000000;
x2 = x2<<2;
x = x2 | x1;
y1=P1; /* reading of cos(theta) */
y1 = y1 & 00111111;
y2=P3;
y2 = y2 & 11110000;
y2 = y2<<2;
y= y2 | y1;
w=atan2(x,y);
z=w*180*7/22; /* radian to degree conversion */
z= (z*512)/180;
if (qs=='1') /* absolute angle estimation of shaft angle */
{
if (qc=='1')
{

```

```
    m=z;
    dec2bin(m);
  }
  else
  {
    m=180-z;
    dec2bin(m);
  }
}
else
{
  if(qc=='0')
  {
    m=180+z;
    dec2bin(m);
  }
  else
  {
    m=360-z;
    dec2bin(m);
  }
}
}
}

void dec2bin (unsigned int x) /* subroutine to convert decimal to binary */
{
for (i=0;i<10;i++)
{
t[i]=x%2;
x=x/2;
}
}
```

C

PIC microcontroller software code

Software code computes the synchro shaft angle for the set of two 8-bit binary data and quadrant bits.

```

#include <demo.h>
#include <stdio.h>
#include <math.h>
#define TX PIN_C6
#define SEL2 PIN_B4      /* selection inputs to read digital sine, digital cosine
                        data and quadrant detector bits */

#define SEL1 PIN_B5
void Read_digital1();   /* function prototype for digital sine data*/
void Read_digital2();   /* function prototype for digital cosine data*/
int8 QS,QC;           /* quadrant detector bits declaration */
char flag1;
float angle2,angle1;
float sinedat,cosdat,err; /* digital sine and digital cosine data declaration */
float arr[4][4];      /* array declaration for quadrant detector bits */

void main()
{
setup_timer_3(T3_DISABLED | T3_DIV_BY_1);
setup_timer_4(T4_DISABLED,0,1);
setup_timer_5(T5_DISABLED | T5_DIV_BY_1);
setup_timer_6(T6_DISABLED,0,1);
setup_comparator(NC_NC_NC_NC);
flag1=0;
arr[1][1]=0.0;
arr[1][0]=-180.0;
arr[0][0]=180.0;
arr[0][1]=-360.0;
while(1)
{
while(flag1==0)
{
output_bit(SEL1,0); /* reading of quadrant detectors bits */
output_bit(SEL2,0);
QS=input(PIN_A5);
QC=input(PIN_C0);
Read_digital1(); /* subroutine call for digital sine data */
Read_digital2(); /* subroutine call for digital cosine data */
angle1 = atan2(sinedat,cosdat);
angle1 = angle1 * 57.324; /* radian to degree conversion */
flag1=1;
}
}
}

```

```

while(flag1==1)
{
Read_digital1();      /* subroutine call for digital sine data */
Read_digital2();      /* subroutine call for digital cosine data */
angle2 = atan2(sinedat,cosdat);
angle2 = angle2 * 57.324; /* radian to degree conversion */
err=abs(angle2-angle1);
if(err<=0.6)
{
printf("synchro angle is %f\n\r",abs(angle1+arr[QS][QC]));
flag1=1;
}
else if(err>0.6)
{
if(err<10.0)
{
printf("synchro angle is %f\n\r",abs(angle2+arr[QS][QC]));
flag1=0;
}
else
{
}
}
}
}

void Read_digital1()      /* subroutine to read sine data [I1..I8] */
{
long x;
output_bit(SEL1,0);
output_bit(SEL2,1);
x=input(PIN_C1)*128+input(PIN_C0)*64+input(PIN_A5)*32+input(PIN_A4)*16+
input(PIN_A3)*8+input(PIN_A2)*4+input(PIN_A1)*2+input(PIN_A0);
sinedat = (float)x;
}

void Read_digital2()      /* subroutine to read cosine data [Q1..Q8] */
{
long x1;
output_bit(SEL1,1);
output_bit(SEL2,0);
x1=input(PIN_C1)*128+input(PIN_C0)*64+input(PIN_A5)*32+input(PIN_A4)*16+
input(PIN_A3)*8+input(PIN_A2)*4+input(PIN_A1)*2+input(PIN_A0);
cosdat=(float)x1;
}
/* demo.h */
#include <18F25K22.h>
#define adc=16
#define FUSES NOWDT          /* No Watch Dog Timer */
#define FUSES WDT128        /* Watch Dog Timer uses 1:128 Postscale */

```

```
#FUSES HSM /* High speed Osc, medium power 4MHz-16MHz */
#FUSES NOPLLEN /* 4X HW PLL disabled, 4X PLL enabled in software
*/
#FUSES NOFCMEN /* Fail-safe clock monitor disabled */
#FUSES NOIESO /* Internal External Switch Over mode disabled */
#FUSES NOBROWNOUT /* No brownout reset */
#FUSES WDT_SW /* No Watch Dog Timer, enabled in Software */
#FUSES NOLVP /* No low voltage prgming, B3(PIC16) or B5(PIC18)
used for I/O */
#FUSES NOXINST /* Extended set extension and Indexed Addressing
mode disabled (Legacy mode) */

#use delay(clock=12000000)
#use FIXED_IO(B_outputs=PIN_B5,PIN_B4,PIN_B3,PIN_B2,PIN_B1,PIN_B0)
#use FIXED_IO(C_outputs=PIN_C7,PIN_C5,PIN_C4,PIN_C3,PIN_C2)
#use rs232(baud=9600,parity=N,xmit=PIN_C6,rcv=PIN_C7,bits=8)
```

D

Bill of materials of Synchro-to-Digital Converter

Bill Of Materials (BOM) of the prototype Synchro-to-Digital Converter

S. No	Component description	Component reference	Manufacturer	Ordering code	package
1	5k/100mW, 0.01% Tol Resistor	R1	NA	NA	Through hole
2	1k/100mW, 0.01% Tol Resistor	R2	NA	NA	Through hole
3	1.5k/100mW, 0.01% Tol Resistor	R3	NA	NA	Through hole
4	500E/100mW, 1% Tol Resistor	R4	NA	NA	Through hole
5	1M/100mW, 1% Tol Resistor	R5	NA	NA	Through hole
6	10k/100mW, 1% Tol Resistor	R6	NA	NA	Through hole
7	Trim Potentiometer-2k	RPOT1- RPOT2	Bourns	Mouser 652-3296W- 1-202LF	Through hole
8	0.1µF/100V	C1	TDK	CGA3E3X7S2A104K	Case 0603
9	10µF/10V	C2	AVX	TPSA106K010R0900	Case 1206
10	22µF/10V	C3	AVX	TPSA226K010R0900	Case 1206
11	33pF/100V	C4	AVX	06031A330JAT2A	Case 0603
12	0.22µF/10V	C5	AVX	0603ZC224KAT2A	Case 0603
13	1k Resistor Network	RPACK1	Bourns	CAY16-102-J4-LF	SMD
14	AD711-OPAMP	U1-U11	Analog Devices	AD711	8 DIP
15	AD790-Comparator	U12-U14	Analog Devices	AD790	8 DIP
16	RS232 Interface IC	U15	MAXIM	MAX3241ECAI+	28 SSOP
17	3.3 V Regulator	U16	Linear Technology	LT1085-3.3V	TO-220
18	Altera CPLD	U17	Altera	EPM3128ATC100	100 TQFP
19	Power On Reset IC	U18	Maxim	MAX824	SOT23-5
20	Microcontroller	U19	Microchip	PIC18F25K22	28 SSOP
21	Oscillator- 16 MHz	Y1	Fox Electronics	FOX924B-16.00	SMD
22	Crystal Oscillator- 12 MHz	Y2	Euro Quartz	Element 14 order - 1640871	Through hole
23	Phoenix Terminal Block - 10 pin	TB1	Phoenix	MKDS 3/ 2- 5, 08	Through hole
24	Mini Phoenix Terminal Block - 12 pin (2.54 mm Pitch)	TB2	Phoenix	MPT 0.5/10-2.54 A	Through hole
25	DSUB Connector 9 Pin Female, Vertical Mount	CONN1	NA	NA	Through hole
26	10 Pin Male Header	H1	TE Connectivity	1-1634688-0	Through hole
27	Vertical Bergstrip- 6 pin	H2	FCI	68000-136 HLF	Through hole
28	4 Layer PCB 160 mm X 100 mm	NA	MICROPAK	NA	NA