Investigations on High Power Solid State RF and Microwave Amplifiers for Superconducting Structures

By

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Final approval and acceptance of this dissertation is contingent upon the candidate's submission of the final copies of the dissertation to HBNI.

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DECLARATION

I, hereby declare that the investigation presented in the thesis has been carried out by me. The work is original and has not been submitted earlier as a whole or in part for a degree / diploma at this or any other Institution / University.

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List of Publications arising from the thesis

Journal

1. "Improved performance of two-way power divider using dielectric resonator", Akhilesh Jain, P. R. Hannurkar, S. K. Pathak, A. Biswas, M. Srivastva, *Microwave and optical Letters*, April **2014**, *Vol*. 56, No. 4, p. 858-861.

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3. "Design and analysis of a high-power radial multi-way combiner", Akhilesh Jain, D. K. Sharma, A. K. Gupta, P. R. Hannurkar, S. K. Pathak, *Int. J. of Microwave and Wireless Technologies*, Feb. **2014**, *Vol*. 6, No. 1, p. 83-91.

4. "Compact solid state radio frequency amplifiers in kW regime for particle accelerator subsystems", Akhilesh Jain, D. K. Sharma, A. K. Gupta, P. R. Hannurkar, S. K. Pathak, *Sadhna, Academy Proceedings in Engineering Sciences*, Aug. **2013**, *Vol*. 38, No. 4, p. 667-678.

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2. "Solid state RF amplifiers for Indus-2 Synchrotron Radiation Source", Akhilesh Jain, P. R. Hannurkar, M. Lad, R. Kumar, M. K. Badapanda, N. Tiwari, D. K. Sharma, A. K. Gupta, A. K. Tiwari, P. Bugdwal, P. D. Gupta, in *National Symposium on High Power RF and Microwave HPRFM13*, Sep. 4-6, **2013**, Bhat, Gandhinagar.
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DEDICATIONS

Dedicated to My Family

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CONTENTS

SYNOPSIS

The radio frequency (RF) and microwave power amplifier is a key technology for the different commercial and strategic systems. The commercial systems include communication system in majority and other systems, for a variety of applications like jamming, EMI/EMC and RF heating. Among different strategic systems, particle accelerator, which heavily depends upon the high power RF amplifiers, is used for high energy physics research and energy generation. It embraces huge machines like collider, synchrotron radiation source and accelerator driven reactor. For such accelerators, the requirement of the RF power is very high among all applications. Each of these applications has its own unique requirements for the frequency, bandwidth, load, power, efficiency and linearity. Though, such requirements govern the characteristics of the RF amplifier used therein, nevertheless, the desired output power is a major factor in deciding the amplifier technology. This technology, in turn dictates the overall cost and performance of the particular system.

For high power systems, vacuum tube based amplifiers have well-established history for communication as well as for particle accelerator. However, in recent years, solid state transistor based power amplifiers, have been attractive in research community. Unparalleled advantages of solid state technology and the practical advancement demonstrated for the superconducting particle accelerating structures have made such solid state power amplifier (SSPA) a promising candidate compared to its vacuum tube counterparts. The latter one depends upon a single tube, for RF signal amplification and for meeting the output power requirement. Conversely, multiple RF transistors (with moderate power handling capability) are suitably paralleled for making a SSPA system with equal power. These transistors, appropriately designed with the impedance matching networks and bias circuits, take the

form of a power amplifier (PA) module. Thus, major constituent blocks of a typical SSPA system are these modules, power combiner/dividers and directional coupler.

With suitable academic efforts, the wide zone of solid state amplifier design, mainly driven by the communication segment, needs to be narrowed down to cater typical requirements of the particle accelerator. Due to a multi-stage *divide and combine* architecture of the SSPA, the design of each constituent block is equally important. Therefore, its investigation needs to be carried out at component level, for better efficiency, design repeatability and higher output power; and at system level, for improved reliability and graceful degradation.

Summary of Research Work and Thesis Organization

The objective of this research work is to explore newer design techniques and topologies for high power solid state RF amplifiers and these constituent blocks, followed by their physical implementation and experimental verification. The solid state PA module, which is a workhorse of the kW level SSPA system, determines the system linearity, efficiency and deliverable output power. Hence to start with, the design equations for fundamental and harmonic terminations, fundamental power and efficiency were derived in terms of transistor's terminal voltage waveform coefficients. For power dividing and combining solution at high power, a novel and multi-way radial combiner was proposed. For RF power measurement, the rigid rectangular coaxial line based directional couplers were devised to give low insertion loss and good directivity. For kW level SSPA systems, the influence of amplitude and phase imbalance on useful performance figures like system gain, system efficiency and power distribution for real time operation was studied.

This thesis presents an effort towards investigating solid state amplifiers topologies, their analysis, characteristics and integration issues, rendering them suitable for high power applications, like particle accelerator. It is organised in six chapters, followed by a conclusion, three appendices and a list of references.

Chapter 1 contains introduction of solid state amplifier, particle accelerator and RF system, followed by literature survey and motive behind this work. It also describes briefly about popular technologies for RF power source.

Chapter 2 includes the analysis and the circuit level design, for the conventional harmonic shorted or tuned load operating modes and related PA circuits. To this end the designs, based on such reduced conduction angle modes, are discussed, implemented, and tested. The applicability of such *a-priori* design and experimental investigation are discussed with the successful implementations of a low power (10 W) and two high power (270 and 400 W) PA modules, using Class A and AB modes of operation.

In **chapter 3,** the investigation on the newer concept of harmonic tuned design space for PA operation is presented along with the experimental studies, at high power (> 500 W). The design techniques, using this concept, are often a subset of Class J, continuous Class J, continuous Class F and multi-mode. The formulation of these types of modes in terms of design coefficients, exemplified in this chapter, provides a mathematical framework to describe a set of the fundamental/harmonic impedance loci, voltage gain and efficiency. The continuous mode resolves the problem of the maximum drain-source voltage for the LDMOS devices. Three such modes were physically examined for the design procedure and their applicability at high power. The first two modes, incorporating continuous class J design space, are without and with third harmonic's contribution, respectively. Their experimental verification, including the X parameter (trademark of Agilent Technology) measurement, confirms the design methodology. The last one is the extended continuous class F approach, with an incorporation of the higher order harmonics.

Chapter 4 encapsulates an overview of the popular divider/combiner schemes and a design theory of N (equal to 2, 8 and 16) ports topology. The design of a novel radial combiner, using the rigid coaxial and radial slab type transmission lines, is presented. This design

depends upon the ability to model a radial transmission line for the calculation of its input impedance. This calculation can be performed by solving the wave equation and corresponding expressions, in terms of Bessel and modified Bessel (Neumann) functions, as suggested by Marcuvitz and Ramo. However, the whole process is significantly complicated due to the existence of a complex characteristic impedance of the line with spatial dependence. Therefore, a different approach using segmented transmission line theory is adopted here. Its application is experimentally demonstrated in this chapter, by designing and fabricating two types of combiners. The first type includes three different novel 8-way combiners at 4 kW, operating at the centre frequency of 352, 505.8 and 704 MHz, respectively. The second one was designed at 16 kW and 505.8 MHz. In this chapter, the design and testing of 2-way combiners, at different power levels is also detailed. Finally, in this chapter, the studies for the performance enhancement of a low power Wilkinson 2-way divider, by loading it with a dielectric resonator, is presented. The necessary vector and high power scalar measurements for all these physically fabricated dividers/combiners are presented to validate the design procedures and to demonstrate their suitability for high power SSPA system.

In **chapter 5,** the theoretical and experimental studies, for high power and wideband directional couplers based on rigid mechanical structures, is described. Such couplers, suitable for high power measurements, were designed in the 300-700 MHz band at different RF powers of 1 kW, 5 kW and 20 kW. These couplers make use of the aperture coupled coaxial transmission lines with a rectangular cross section. The developed electromagnetic models of these couplers for the full wave analysis are presented, followed by a discussion of their fabrication and measured results. These results show a good agreement with the design specifications and simulated data.

In **chapter 6**, the system related issues like architecture selection, power degradation for different degree of the amplitude/phase imbalance and worst case efficiency for a real operat-

ing condition are examined. In this chapter, for such integrated system, the graceful degradation analysis is presented for the uniform as well as random amplitude and phase imbalance. A scattering parameter based behavioural model, for supporting this analysis developed in tune with the design guidelines available from the literature, is described. This analysis and simulation study (using Visual system simulator) is helpful for predicting the power gain, system (wall-plug) efficiency, and the reflected power due to amplitude and phase imbalance in the SSPA system. The successful design and experimental study for three high power SSPA systems at 2 kW, 20 kW and 50 kW respectively, as an outcome of the above study, is exemplified in this chapter. Finally, future scope of the conducted research work is discussed with the concluding remarks.

In this research work, an investigation for the design and analysis was carried out for high power (kW level) solid state radio frequency amplifiers. These amplifiers incorporate moderate level power amplifier modules, power dividers, power combiners and directional couplers. The successful design and physical implementation of conventional and newer harmonic tuned amplifier modules paves the way towards implementation of the continuous class J and class F family, for the cutting edge technology of solid state devices based power sources in the field of particle accelerators. The theoretical design and experimental work, carried out for the radial combiner and rigid directional coupler, represent a significant improvement for high-power *divide and combine* architectures. These components, after being optimised with a simulation software, based on finite-element method, were tested to demonstrate very good agreement with simulation results, confirming the validity of the proposed design method. The developed analysis and research study is equally applicable to the higher frequency regime. This research work provides the design and experimental data concerning real time performance for research community associated with high power radio frequency and microwave solid state amplifiers.

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LIST OF ABBREVIATIONS

ADS	Accelerator-driven system
APS	Advanced Photon Source (www.aps.anl.gov)
CERN	European Organization for Nuclear Research (www.cern.ch)
CL	Coupling loss
C-MET	Centre for material for electronic technology
CTL	Coaxial transmission line
CW	Continuous wave
DC	Direct current
DR	Dielectric resonator
ECM	Electronic countermeasure
EM	Electromagnetic
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESRF	European Synchrotron Radiation Facility (www.esrf.fr)
GSM	Global System for mobile communication
HBT	Hetero-junction Bipolar Transistors
HEMT	High Electron Mobility Transistors
HFSS	High frequency structure simulator
HOM	Higher order mode
IL	Insertion loss
ILC	International linear collider (www.linearcollider.org)
IMN	Input impedance matching network
INFN	Instituto Nazionale di Fisica Nucleare (www.infn.it)
IOT	Inductive output tube
LDMOS	Lateral diffused Metal oxide semiconductor
LINAC	Linear accelerator
LLRF	Low-level radio frequency
LNLS	Laboratório Nacional de Luz Síncrotron (www.lnls.br)
MESFET	Metal Semiconductor FET
MOSFET	Metal oxide semiconductor field effect transistor

NCRF	Normal conducting radio frequency
NCRF	Normal conducting RF
OMN	Output impedance matching network
PA	Solid state power amplifier module –with few hundreds of Watts
PAE	Power added efficiency
PCB	Printed circuit board
PDC	Power divider and combiner
PSI	Paul Scherrer Institute (www.psi.ch)
RF	Radio Frequency
RFID	Radio Frequency Identification
RRCAT	Raja Ramanna Centre for Advanced Technology (www.rrcat.gov.in)
RTL	Radial transmission line
SCRF	Super conducting RF
SCRF	Superconducting radio frequency
SNS	Spallation neutron source (www.sns.org)
SOLEIL	Source Optimisée de Lumière à Énergie Intermédiaire du Lure (www.soleil.fr)
SRS	Synchrotron radiation source
SSPA	Solid State RF and microwave power amplifier at high power (kW levels)
TMM	Thermo state material, a trademark of Roger Inc.
	Canada's national laboratory for particle and nuclear physics (www.triumf.ca)
UHF	Ultra high frequency
VDMOS	Vertical diffused Metal oxide semiconductor
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
XFEL	(www.xfel.eu)

LIST OF SYMBOLS

a_1, a_2, a_3	Radii of the inner conductors of coaxial sections in the feed line of a radial power combiner
a_{dr}	Radius in mm for a cylindrical dielectric resonator
a_{in}	Fourier coefficient associated with the real terms in I_{ds} expression
a_m	Dimension of square transmission (main) line in directional coupler
a_{vn}	Fourier coefficient associated with real terms in V_{ds} expression
a_x	Inner dimension of square transmission line in directional coupler
A_{11}	Fundamental tone of the signal for large signal analysis
b	Radius of the outer conductor of feed line in radial power combiner
b_{co}	Output power wave from the power combiner
b_{in}	Fourier coefficient associated with the imaginary terms in I_{ds} expression
b_m	Dimension of square transmission (main) line in directional coupler
b_{si}	Output power wave from the RF power amplifier
b_{vn}	Fourier coefficient associated with imaginary terms in V_{ds} expression
b_x	Outer dimension of square transmission line in directional coupler
$b_{c0}^{'}$	Degraded output power wave from the combiner
B_1, B_2	Susceptance at radial to coaxial transmission line junction
c_1, c_2, c_3	Constant used in empirical relation for modeling nonlinear drain capacitor
B_m	Susceptance for the stub loaded Wilkinson power divider/combiner
C	Power Coupling (in dB) of a directional coupler
C_b	Ideal DC-blocking capacitor in impedance matching network
$C_j(r)$	Static capacitances at the coaxial line junction
C_m	Capacitance for the stub loaded Wilkinson power divider/combiner
C_r	Constant curvature of the annular strips for segmenting a radial line
C_{zero}	Output capacitor at zero value of drain-source voltage
C_A and C_B	Transversal capacitances (per-unit length) in directional coupler
C_{AB}	Mutual capacitance (per-unit length) in directional coupler
C_{IN}	Input capacitor in the model of a MOSFET
C_{OUT}	Output capacitor in the model of a MOSFET
d	Height of the radial line in multi-way radial power combiner
d_1, d_2, d_3	Length of coaxial sections in the feed line of a radial power combiner
D	Directivity (in dB) of directional coupler
$E_z(r)$	Electric field for radial transmission line in dominant mode
f_1	Fundamental frequency of the RF signal
f_{dr}	Resonant frequency of dielectric resonator in dominant $TE_{01\Delta}$ mode

$f_{max,E}$	Maximum operational frequency for a Class-E power amplifier
g_{ds}	Output conductance of the MOSFET
g_m	Trans-conductance of the MOSFET
G	Nominal voltage gain of the power amplifier
G_{0h} and G_{1h}	Magnitude part of Hankel functions
δG_i	Variation in gain of the output signal of i^{th} power amplifier
h	Height of the substrate, for microstrip calculation
h_1	Height of the inner conductor of auxiliary line in directional coupler
h_{dr}	Height in mm for a cylindrical dielectric resonator
$H_0^{(+)}$, $H_0^{(-)}$	Hankel functions for outward (forward) and inward waves respectively
$H_\varphi(r)$	Magnetic field for radial transmission line in dominant mode,
$i_{ds}(\theta)$	Normalized drain-source current with respect to I_{max}
I	Isolation (in dB) of directional coupler
I_{ds}	Drain current of the MOSFET
I_{max}	Maximum drain current (I_{ds}) at hard saturation
I_{DC}	DC current at the drain terminal
I_L	Load current in a power amplifier
J_n	Bessel functions
k	Wave number, equal to $2\pi/\lambda$
k_c	Mid band voltage coupling factor
k_s	Rollet stability factor for S parameter based small signal amplifier design
k_n	Design coefficients in v_{ds} expression for harmonic tuned power amplifier
K	Number of inputs in a single power combiner for tree combining scheme
l	Length of the directional coupler in *z* direction
L	Insertion loss of a single coupler/stage in travelling wave/tree power combiner
L_{RFC}	Ideal choke exhibiting short-circuit at DC and open circuit at RF
M_b	Ratio of maximum to minimum amplitude of input signal to the combiner
M_S	Ratio of maximum to minimum magnitude of transmission coefficient
N_n	Neumann function
p	Degradation in power for an unhealthy power amplifier
P_1	RF power output at the fundamental frequency
P_{1A}	RF power at fundamental frequency for Class A mode
$P_{cin,i}$	Input power fed to i^{th} branch of the combiner
P_{diss}	Power dissipation in solid state device of a power amplifier
P_{in}	Input RF power fed to power amplifier
P_{out}	Output RF power
P_{1E}	RF power at fundamental frequency for Class E mode of operation

P_{DC}	DC power delivered from the bias supply connected at the drain terminal
P_{DCA}	DC power supplied to power amplifier in Class A mode
$P_{DC,E}$	DC power delivered for the Class E mode of operation
q	Total number of segmented strips in radial line
r_a	Radius of the placement of branch connectors in radial line
r_b	Radius of the inner conductor of radial line
r_c	Radius of the outer conductor of radial line
R_o	Radius of the inner most strip in segmentation of the radial line
R_1	Fundamental RF load for in-phase fundamental voltage and current
R_{1A}	Output load resistance at fundamental frequency for Class A mode
R_{iso}	Isolation resistor in Wilkinson power divider/combiner
$R_{n,ave}$	Average radius of the n^{th} strip in segmentation of the radial line
R_p	Radius of the outermost strip in segmentation of the radial line
R_{IN}	Input resistor of the MOSFET
R_L	Load resistor of the power amplifier, generally equal to system impedance
s	Aperture spacing in directional coupler
s_{11}	Small signal reflection coefficient at terminal 1 for a 2-port network
s_{12}	Small signal reverse gain for a 2-port network
s_{21}	Small signal gain for a 2-port network
s_{22}	Small signal reflection coefficient at terminal 2 for a 2-port network
S	Number of stages in a tree power combiner
t_s	Thickness of the inner conductor radial line in a radial power combiner
$v_{ds}(\theta)$	Normalized drain-source voltage with respect to V_{DD}
$v_{ds,sn}(\theta)$	Drain voltage, shifted by V_{DD} and normalized with respect to V_1
V_1	Fundamental drain voltage component
V_{13}	Voltage coupling from main port to the coupled port in directional coupler
$V_{1,TL}$	Reduced fundamental drain voltage component due to knee voltage
V_{ds}	Voltage across the drain and source terminals of the MOSFET
V_{gs}	Voltage across the gate and source terminals of the MOSFET
V_i	Voltage amplitude of incident wave at input port of directional coupler
V_{in}	Sinusoidal RF signal at the input of a power amplifier
V_k	Turn-on or knee voltage of the MOSFET
V_{max}	Maximum (permitted) value of the drain-source voltage V_{ds}
V_n	Harmonic load voltage component at $f_n = nf_0$
V_{pk}	Peak value of the drain-source voltage in switching amplifier
V_r	Voltage of the reflected wave in a directional coupler
V_{cs}	Voltage across the shunt capacitor in Class E topology
V_{DD}	DC bias voltage applied at the drain terminal of the MOSFET

V_{GG}	DC bias voltage applied at the gate terminal of the MOSFET
V_L	Voltage across the load in a power amplifier
V_s	Amplitude of the input sinusoidal RF signal (V_{in})
V_T	Threshold voltage of the MOSFET
w	Width of copper trace or microstrip transmission line
w_o	Width of the inner most strip in segmented radial line
w_p	Width of the outer most strip in segmented radial line
$x_i(t)$	Time varying input signal
$\mathrm{X}_{22,11}^{(\mathrm{S})}$	Large signal output reflection coefficient
$X_{22,11}^{(T)}$	Large signal output reflection coefficient due to cross frequencies
$Y(t)$	Time varying output signal in an N-way amplifier-combiner system
$z'(r)$	Normalized impedance for the radial transmission line in dominant mode
Z_0	Characteristic impedance for transmission line
Z_{b1} and Z_{b2}	Branch impedances in a 2-way divider/combiner
$Z_{0,sq}$	Characteristic impedance of coaxial cable with the square outer conductor
$Z_{0,strip}$	Characteristic impedance of the strip-line
Z_b	Parallel resultant of branch ports impedances
Z_c	Input impedance of open circuited radial stub with annular width $(r_b - r_a)$
$Z_{oe}\ and\ Z_{oo}$	Even and odd mode impedances
Z_{CTL}	Impedance at the coaxial port, Z_{RTL} is the impedance of the radial line
$Z_L, Z_L(f_n)$	Load impedance at the transistor's output port at harmonic frequency f_n
Z_{RTL}	The impedance of the radial line
Z_{TEM}	Free space impedance
α	Design parameter in non-zero-crossing expression for drain-source voltage
α_m	Coefficient related to knee region sharpness in MOSFET model
β	Design parameter in non-zero-crossing expression for drain-source voltage
β_m	Coefficient related to the maximum drain current in MOSFET model
γ	Design parameter in non-zero-crossing expression for drain-source voltage
γ_m	Coefficient related to the FET 'square-law' characteristic
Γ	Reflection coefficient
Γ_{lm}	Optimal passive load termination for small signal amplifier design
Γ_{si}	Reflection coefficient at the i^{th} output of a power amplifier
Γ_{sm}	Optimal passive source termination for small signal amplifier design
δ	Voltage gain function in harmonic tuned power amplifier
δ_{max}	Difference between maximum and minimum phase of the product term $a_{ci}.s_{coi}$
δ_p	Phase shift among output signal of healthy and un-healthy power amplifier modules

δ_I	Peak value of the drain current to the respective DC component
δ_V	Peak value of the drain voltage to the respective DC component
$\delta\varphi_i$	Variation in phase of the output signal for i^{th} power amplifier
Δ	Variation of electric field in the axial or z direction for $TE_{01\Delta}$ mode
ϵ_r	Relative permittivity of the dielectric material
η_c	Combining efficiency when all input signals are equal and in-phase
$\eta_{c,max}$	Maximum combining efficiency of power combiner
η_{pc}	Efficiency for an N-way amplifier-combiner system
η_{pae}	Power added efficiency (PAE) of an amplifier module
$\eta_{pa,k}$	Reduced DC to RF drain conversion efficiency, due to knee voltage
$\eta_{pa,HT}$	DC to RF conversion efficiency for harmonic tuned power amplifier
$\eta_{pa,RF}$	DC to RF power conversion or drain efficiency
$\eta_{pa,SW}$	DC to RF conversion efficiency for power amplifier in switching mode
$\eta_{pa,TL}$	DC to RF conversion efficiency for tuned load or harmonic shorted mode
θ	Variable for angular phase shift
θ_q	Electrical length of impedance transformer in Wilkinson power divider/combiner
θ_1 and θ_2	Phase delay through the coupled and isolated path in directional coupler
θ_{qr}	Reduced electrical length of the impedance transformer in stub loaded Wilkinson power divider/combiner
λ	Guide wavelength of the RF signal
λ_m	Coefficient related to finite output conductance in MOSFET model
μ	Magnetic permeability
ξ_n	Phase angles of n^{th} component of the drain current (I_n)
φ_n	Phase angle of n^{th} impedance (Z_n) at the drain terminal of amplifier
Φ	Conduction current angle (CCA) in harmonic shorted operating modes
χ	Degradation factor due to knee voltage of MOSFET
ψ_n	Phase angles of the of n^{th} component of the drain voltage (V_n)
ω	Angular frequency

Chapter 1. Introduction

A radio frequency (RF) and microwave power amplifier (PA) is an indispensable and key technology for a broad set of commercial [1] and strategic [2] applications. Regardless of its physical realization, task is to increase the power level of the RF signal at its input in a given frequency band, up to a predefined level at its output at the expense of DC input power from the bias power supply. The commercial applications include communication system in majority and other systems for a variety of applications [3] like jamming, imaging, EMI/EMC and RF heating. The strategic system includes electronic counter measure (ECM) systems and particle accelerators. The latter one, being used for the high energy physics research and energy generation, embraces huge machines like particle collider, synchrotron radiation source and accelerator driven reactor. In communication systems like satellites, radios, radars, telemetry, and cellular phones, the RF power amplifiers are used in multitude for amplifying carrier signal modulated with baseband information. Among these systems, the wireless technology, for cellular or mobile communication, is a fast growing segment for RF amplifiers used in the base station and mobile handset. This technology is characterized by various communication standards like GSM, W-CDMA and WiMAX and thus requires different types of PAs operating in different frequency bands (900 MHz, 1800 MHz, 2100 MHz, 3500 MHz, etc.). In addition to these ubiquitous requirements, one recent application is wireless power transmission [4] or where electrical energy is transmitted from a power source to an electrical load without the use of wire. Its potential use include charging of mobile phones and laptops, radio-frequency identification (RFID), electrically charged vehicles, biomedical sensors, space solar power satellite and solar energy to earth. Such power transfer, using RF, has some advantages over other methods (like plastic sheet, inductive coupling and

Lasers) such as its use for longer distances with relatively higher efficiency and more mature technology. There are also other potential applications [5], such as material processing and atmospheric modification. The material processing uses Gyrotron technology, originally developed for the fusion program to provide a high average power millimetre-wave radiation for the ceramic sintering. The microwave atmospheric modification includes a possible solution to global problems such as ozone depletion and global warming.

Each of these applications has its own unique requirements for frequency, bandwidth, load, power, efficiency, linearity, thermal design and cost. Perhaps the output power of the RF amplifier, used therein, is a major factor deciding the technology, cost and performance of the particular system. As a consequence, increasing interest has been focused by academic and industrial communities on the RF power amplifiers. The Table 1.1 [6] shows that the requirement of the RF power among various applications is very high for the radar transmitter as well as for the particle accelerator.

Table 1.1: Typical RF power level required for different applications [6]

Sr.	**Application area/Technology**	**Typical power level**
1	Bluetooth- Class 1	100 mW
2	Bluetooth- Class 2	6 mW
3	Bluetooth- Class 3	1 mW
4	Broadcast – Low power	10-100 W (CW)
5	Broadcast – High power	100 kW (CW)
6	Cellular - Mobile phone	100 mW-4W
7	Cellular - Base station	50 W (average) 300 W (peak)
8	Magnetic resonance imaging (MRI)	30-40 kW (pulse)
9	Radar communication	100 kW (pulse)
10	WiMax – handset	200 mW
11	WiMax – Base station	20 W
12	WLAN (wireless)	100 mW
13	Particle accelerator	10-300 kW (CW) 600 kW (pulse)
14	Industrial processing	500 W – 50 kW (pulse)

The radar system locates and characterise the distant objects by radiating the electromagnetic (EM) energy, typically in S band and above. In the particle accelerator, EM energy is conveyed to the charged particles' bunches, for propelling them to high speed. For each of these systems, the EM energy comes from high power (kW level) RF systems. The majority of such systems are based on vacuum tubes amplifiers, with dominance of klystrons and traveling-wave tubes (TWT). In last few years, the tremendous progress reported for the solid-state device based power amplifiers is progressively enabling them to erode this dominant position. Performance wise, the design requirement and final implementation is nearly equally crucial for radar transmitter as well as particle accelerator. However, to outfit typical requisites of a majority of particle accelerators, their RF systems operate, at comparatively lower frequency band (VHF to S band) with slightly different characteristics. Before discussing about the RF power systems in detail, it is good to have an introductory discussion of the particle accelerator.

1.1 Particle Accelerator

The particle accelerator [7] research is one of the important fields of interest in the modern day science and technology. The basics of the particle accelerator revolve around the charged particles which are an elementary particle or a macro-particle containing an excess of the positive or negative charge. Its motion is determined mainly by the interaction with electromagnetic forces. The species of charged particles range from electrons to heavy ions whereas the energy of useful charged particle beams ranges from a few thousands of electron volts (keV) to almost 1 TeV (10^{12} eV). Nuclear physicists and cosmologists use beams of bare atomic nuclei, stripped of electrons; to investigate the structure, interactions, and properties of the nuclei themselves, and of condensed matter at extremely high temperatures and densities. This might have occurred in the first moments of the Big Bang. At lower energies, beams of accelerated nuclei are also used in medicine, as for the treatment of cancer. Besides

being of fundamental interest, the high energy electrons may be coaxed into emitting extremely bright and coherent beams of high energy photons ultraviolet and X-ray via the synchrotron radiation. Such radiations have numerous uses [8] in the study of atomic structure, chemistry, condensed matter physics and biology. Such synchrotron radiation sources are the most versatile tool for characterizing materials and processes and for producing micro and nano-structured devices. As a microscope for the micro-matter studies, the *resolution* of accelerators is limited by de Broglie wavelength. This wavelength is inversely proportional to particle momentum. Thus smaller the substance, the higher beam energy or particle momentum is needed.

The acceleration of the charged particles is conveniently divided into two categories; electrostatic and electromagnetic acceleration. The accelerating field in the first category is the gradient of an electrostatic potential, managed across an acceleration gap with the help of a high-voltage DC source. This source induces arcs and corona discharges, putting an upper limit on gap voltage and thus maximum energy attained by particles. Hence, it is more economical to make the charged particles pass through the acceleration gap many times. With DC source such scheme is not possible due to close loop. Hence, such accelerating gap is in the form of resonant circuit, excited by time-varying EM fields at RF. This resonant circuit is the main accelerating structure materialised as an EM cavity. The circular accelerators are well suited to the production of beams with a high kinetic energy. Apart from such circular accelerators, the linear accelerator (LINAC) is also popular. It uses the EM energy for the initial acceleration of low-energy beams or the generation of high-flux beams.

Some of the accelerator machine in operation are Large Hadron Collider (LHC) at CERN Geneva, PSI in Switzerland, Spallation Neutron Source (SNS) in Oak Ridge USA, European Synchrotron Radiation Facility (ESRF) in France and Indus accelerators at Raja Ramanna Centre for Advanced Technology (RRCAT) in India. The LHC machine [9] is one of the

powerful accelerators in the world. This has been built in a circular tunnel of 27 km circumference. It is in the news in view of its discovery of new particle Higgs Boson [10] which is under study. The Indus accelerator complex at RRCAT consists of Indus-1 (a 100 mA, 450 MeV storage ring) [11] and Indus-2 [12], sharing a common injector system, comprising of 20 MeV microtron and 700 MeV booster synchrotron. The storage ring Indus-2 is a 2.5 GeV Synchrotron Radiation Source (SRS) with critical wavelength of about 2Å. Its total circumference is 172 meter and its RF system operates at the radio frequency of 505.812 MHz.

The RF cavity in the circular as well as the linear particle accelerator is excited by a high power RF amplifier. This amplifier, along with the transmission line/waveguide, circulator, low-level signal processing units and power supply, makes a complete RF system.

1.2 RF System for Particle Accelerator

The RF system [13] is one of the main subsystems for any high energy particle accelerator. It compensates the loss of energy of charged particles along with necessary particle's acceleration. This loss is due to the emission of the electromagnetic radiation by charged particles, under the influence of the electric and magnetic field, or through parasitic losses because of the vacuum chamber impedances. It is depicted in Fig. 1.1, for a synchrotron radiation source using a bending magnet for controlling the trajectory of the particles.

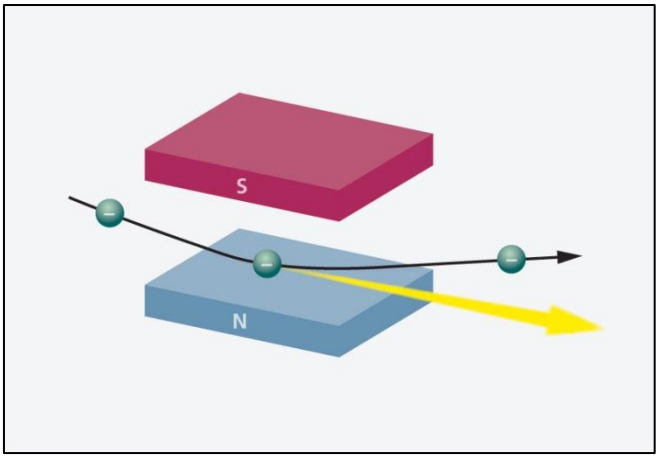


Fig. 1.1: Synchrotron light emitted by a charged particle

The RF system is an important part of the particle accelerator, affecting the quality of the beam, cavity higher order mode (HOM) impedances, beam loading, and HOM induced coupled bunch instabilities. The major components of an RF system (Fig. 1.2) are high power RF amplifier, low-level RF (LLRF) signal processing unit, circulator, different directional couplers, RF cavity and transmission lines. A master signal source, with a high signal purity and stability, distribute the signal to this system. When the total RF power requirement exceeds the capabilities of a single RF amplifier, multiple amplifiers are used. It requires a controlled distribution of the RF signal and phase synchronism among different amplifiers.

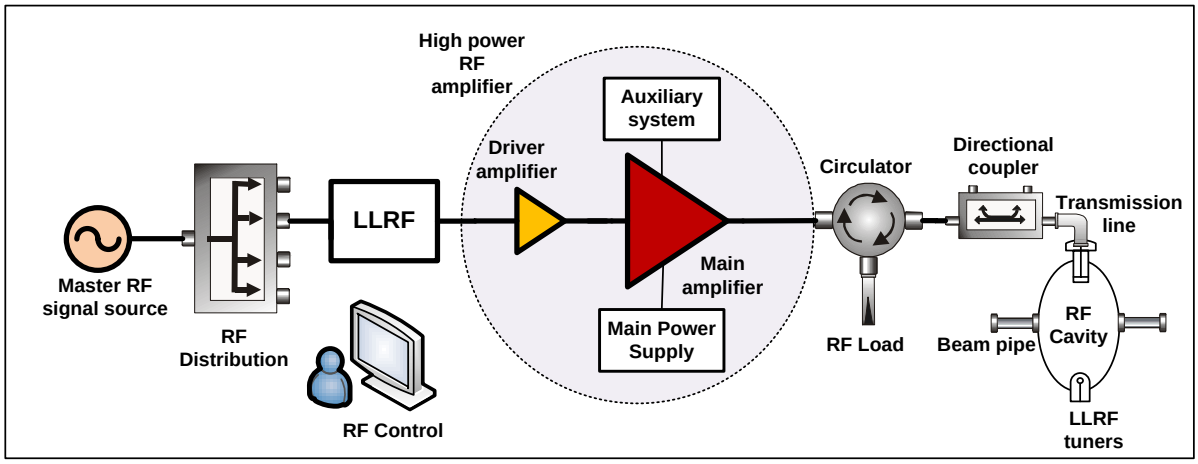


Fig. 1.2: A typical RF system used in particle accelerator

1.2.1 Low-Level RF Signal Processing Unit

In an RF cavity, the accelerating voltage is the vector sum of the RF voltage from the source and the induced voltages due to electron beam passing through beam pipe [14]. The accelerator application also requires a synchronisation of the electromagnetic wave with the particle trips and RF phase stability of the net RF voltage, both in the accelerating cavity. It ensures that the electron bunch is accelerated at the synchronous phase of the RF cavity voltage. All these tasks are accomplished with the help of control loops in the LLRF unit, which includes the main RF control and different feedback units like phase shifter, phase detector, amplitude controller. High power circulator, before the RF cavity, helps dumping of

the reflected power from the cavity without making any damage to the source. The RF power measurement and control action is taken with the help of the directional coupler and different loops, implanted inside the cavity.

1.2.2 RF Cavity

The RF cavity is an accelerating structure of the RF system where particle beam interaction with the RF signal takes place. It acts as a source of the electric field which helps to accelerate the particle beam passing through it. Essentially it is an electromagnetic resonator which resonates at a particular frequency, depending upon its physical dimension and body temperature. The commonly used resonator cavity in the storage rings are cylindrical and coaxial type. These cavities generally operate in the TM_{010} mode (fundamental mode), which has the lowest cut-off frequency. In general the sinusoidal time-varying fields are used. The basic field pattern of an RF cavity, useful for the particle acceleration, is shown in Fig. 1.3.

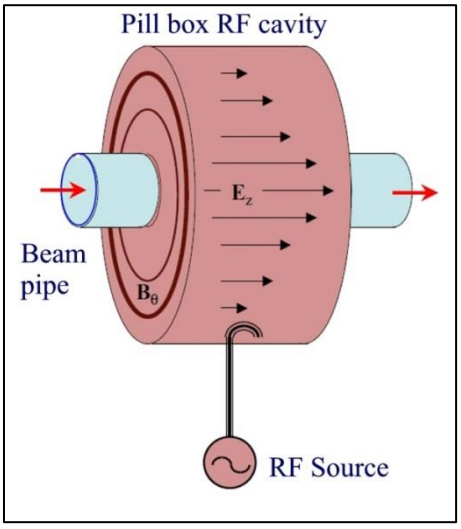


Fig. 1.3: Particle beam and dominant mode electromagnetic fields in a pill-box cavity.

The major operating parameters of a cavity include the transit time factor, shunt impedance and quality factor. The transit time factor indicates the effect of finite passage time for a particle to traverse the RF cavity, while the accelerating field varies with time. It reduces the effective voltage seen by passing particle. The unloaded quality factor is an important figure

of merit for cavity design. For copper cavity its value falls in the range of 10^6 to 10^7. It measures the energy storage efficiency of each resonant mode of the cavity. For characterising the wall losses, it is a convenient parameter for the number of oscillations it takes the stored energy in a cavity to dissipate to 1/e times the initial value. The shunt impedance is the parameter to characterize the strength of the interaction between the cavity mode and a particle of unit charge. For the accelerating mode, it represents the power efficiency of the cavity to accelerate particles. Fig. 1.4 shows RF cavities, along with major operating parameters, deployed at RRCAT in Indus-1 and Indus-2 machines, respectively.

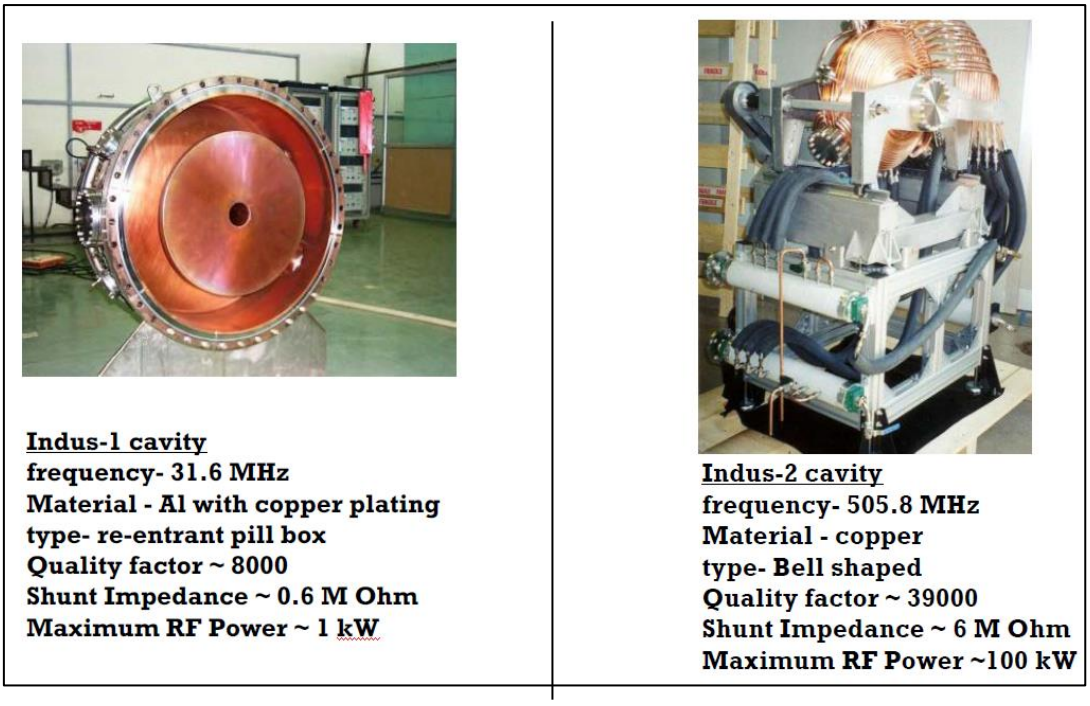


Fig. 1.4: RF cavities operational in Indus-1 and Indus-2 Synchrotron radiation sources

Both of these machines were designed for acceleration of the electrons. The RF accelerators for protons or heavier ions require low frequencies (< 1 GHz), hence, the ferrite loaded cavities are used therein. Since the ohmic power loss in the walls of a cavity increases as the square of the accelerating voltage, the normal conducting RF (NCRF) cavities made with copper material become uneconomical, when the demand for the high average power grows with the particle energy. A similar situation prevails in the pulsed accelerators that demand a

long RF pulse length. For such situation, the use of an RF cavity made with the superconducting material brings immense benefits.

The Superconducting RF (SCRF) cavity [15] has certain advantages over the normal conducting RF cavity. After accounting for the refrigerator power needed to provide the liquid helium operating temperature, a net gain factor of several hundred remains in the overall operating power for superconducting cavities over NCRF copper cavities. Only a tiny fraction of the incident RF power is dissipated in the cavity walls, the lion's share is either transferred to the beam or reflected into a load. By virtue of low wall losses, it is affordable to deploy a solid state RF power amplifier, at moderate power level, to energise a SCRF cavity.

In contrast to the DC case of superconductors, they are not free from energy dissipation in RF fields. This is because the RF magnetic field penetrates a thin surface layer and induces oscillations of the electrons which are not bound in Cooper pairs. The number of these free electrons drops exponentially with temperature. Nevertheless, the surface resistance of a superconducting cavity is of many orders of magnitude less than that of copper. Hence, the intrinsic quality factors of superconducting cavities are usually in the 10^9 to 10^{10} range. Also unlike hard superconductors used for magnets, in RF and microwave applications its limitation is not given by the upper critical field, but rather by the so-called superheating magnetic field which is well below 1 T, for all known superconductors. Moreover, the strong flux pinning appears undesirable in the RF and microwave cavities as it is coupled with hysteretic losses. Hence, a soft superconductor must be used. The pure niobium is still the best candidate although its critical temperature is only 9.2 K and the superheating field about 240 mT.

1.2.3 RF Power Amplifier

The accelerator design is extremely associated with different parameters of the RF power amplifier. The RF technologies for the power amplifier pose a challenging matrix of interdisciplinary science and engineering. Hence, its selection is not only a technical aspect but

financial and operation related aspects are also important. Different types of high power RF amplifiers [16] are available from the industry. Most of the design techniques for these amplifiers have been borrowed from the matured area of radar transmitters.

For generating a kW level of RF power, required in particle accelerator and radar, the vacuum-tube RF amplifier/transmitter is widely used due to their high power capability and established flight history. These tubes use electrons to generate a coherent electromagnetic radiation. The coherent radiation is produced when electrons that are initially uncorrelated, and produce a spontaneous emission with the random phase, are gathered into micro-bunches that radiate in phase. There are three kinds of electromagnetic radiation by the charged particles. The first one is Cherenkov or Smith–Purcell radiation of slow waves propagating with velocities less than the speed of light in vacuum. The second one is the transition radiation and the third one is bremsstrahlung. The tubes based on the first kind include traveling-wave tubes (TWT) and backward-wave oscillators (BWO). In TWT an electron beam guided by an external magnetic field, amplifies an injected electromagnetic wave in a periodic rippled-wall structure. BWOs operate in regions where the group velocity is negative and it amplifies backward waves, which propagate in the opposite direction as the electron beam, thus providing an internal feedback mechanism.

The transition radiation occurs when electrons pass through a border between two media with different refractive indices, or through some perturbation in the medium such as conducting grids or plates. In radio-frequency tubes, these perturbations are grids. Klystrons [17] are the most common type of device, based on the coherent transition radiation from electrons. A typical klystron amplifier consists of one or more cavities, separated by drift spaces followed by an output cavity. This space is used to form electron bunches from an initially uniform electron flow by modulating the electron velocity using the axial electric fields of a transverse magnetic TM_{110} mode. The output cavity produces coherent radiation by deceler-

ating the electron bunches. In recognition of the relativistic modifications to the electron equations of motion, klystron amplifier tubes operating at approximately 500 kV and above are often referred to as relativistic klystron amplifiers (RKA). The term relativistic refers principally to the use of high-energy electrons, where relativistic effects modify the usual formulas for klystron bunching. Extracting the electron kinetic energy in a single RF gap becomes increasingly difficult both as the electron energy increases and as the frequency increases. For such cases multi-section cavity structures are required. One common feature of the high-power linear-beam devices is multi-section output cavities, operating either in a standing or traveling-wave configuration. They lower the required RF fields by progressively extracting the electron kinetic energy in a sequence of gaps.

Another tube *viz.* Inductive Output Tubes (IOT) [18] has recently been adopted for several accelerators as an alternative to klystron. Conceptually, it is between tetrode and the klystron. One key advantage of the IOT at Ultra-high-frequency **(**UHF) over both the tetrode and triode is its power gain. The tetrodes and triodes offer a gain of between 13-15dB with DC to RF efficiency around 60%. The input stage of an IOT is a triode electron gun in which the current is determined by the space-charge limited flow in the region between the cathode and the grid. It uses a high voltage DC and a magnetic lens to focus a modulated high energy electron beam through a small drift tube like a klystron. This drift tube prevents the backflow of the electromagnetic radiation. The bunched electron beam passes through a resonant cavity, equivalent to the output cavity of a klystron. The electron bunches excite the cavity, and the electromagnetic energy of the beam is extracted by a coaxial transmission line. About 300 kW power can be obtained by combining IOTs. Its operation [19] has modularity and constitutes easy manipulation with the sufficient bandwidth.

Another popular accelerating scheme is two-beam acceleration. In this scheme, a low-current beam is accelerated to very high energies using microwaves generated by another

higher current electron beam at moderate voltage. It is a special kind of RKA. The micro-wave power is generated by a klystron-type interaction. The key to this concept is to use a much higher beam energy than is conventional in other klystrons, and to extract only a small fraction (10%) of the kinetic energy in a single stage, which then drives a fixed length of the high-energy accelerator. The electrons are then reaccelerated in an induction module before being sent through another extraction cavity to generate additional microwave power. If this process can be continued over and over again without severe deterioration of the beam phase space, then the overall efficiency can be quite high, since the spent electrons are continually being reused rather than collected. A two-beam accelerator concept is under investigation at CERN to generate 30-GHz microwaves for CLIC [20]. For accelerator operation, below 300 MHz, grid tubes are still used for power amplifier. Above 300 MHz, the klystron amplifiers are more popular. Dedicated super-klystron, generating power in the order of Mega-Watt (MW), for CW operation has been developed in the range of 350 MHz to 1000 MHz.

The last category of the devices uses the Bremsstrahlung radiation. It occurs when electrons oscillate in external magnetic and/or electric fields. In bremsstrahlung devices, the electrons radiate EM waves whose Doppler-shifted frequencies coincide either with the frequency of the electron oscillations or with its harmonic. The best known devices in which electrons oscillate in a constant magnetic field are the cyclotron resonance masers (CRM). The gyrotron is a CRM, in which a beam of electrons moving in a constant magnetic field, along helical trajectories, interacts with electromagnetic waves excited in a slightly irregular waveguide at frequencies close to cut-off. Gyro-devices, like linear-beam devices, have many variants. Vircators, or virtual-cathode oscillators, constitute a special Class of bremsstrahlung device in which the electrons oscillate in electrostatic fields. It can be treated as an extreme case of the intense-beam RKA. For unconditioned RF power, devices [21] like magnetron,

gyratron and vircator are preferred. The gyrotron is widely used as a power source in fusion reactors for producing an intense plasma state.

With the advent and practical progress made in the field of the SCRF cavity, the RF power required for a typical accelerator has come down to few hundreds of kWatts. For such power regime, the solid-state transistors based RF amplifier (SSPA) system is rapidly replacing the Klystron based amplifier in the modern accelerator designs. A practical high-power microwave tube must incorporate a variety of technologies, including a high-voltage power supply, a high-power electron gun, a high-power RF circuit, a suitable RF vacuum window, and an electron-beam collector. Due to high voltage supply and possible X-ray emission, the associated safety and careful operating features are essential. The RF power transistors, on the other hand, operate at a nominal DC voltage. Thus the solid state RF amplifier enjoys a simple maintenance, redundant design, the absence of a high voltage power supply, no warm up time, lower cost and simple start-up procedures. However, the RF power which can be generated by a single transistor is of the order of hundreds of watts (continuous) and up to few kW for the pulsed operation. Hence, large numbers of transistors are operated in parallel to reach the kW level of RF power, required for energizing SCRF cavity. This adds the modularity and scalability to the amplifier architecture. Earlier, this technology has been used for low power driver amplifiers in UHF [22] system, S band LINAC [23] and for radar transmitter [24], for feeding the input power to electron tubes and klystrons. With competing progress made in the solid state technology, such amplifiers now have their output power extending from a few kW to several hundred of kW, in the frequency range of 30 MHz to above 3 GHz.

Most of the research on advanced RF source for accelerators has been motivated by the requirements for the proposed new accelerators. Dramatic advances have been made in both high peak and high-average power microwave sources over the past decade. However, this

field has by no means reached its limits. New high-power sources will be needed for future fusion devices, future accelerators, and future military systems, including radar and electronic warfare devices. Though there are different RF power sources, the advent of solid state amplifier [25] outshine, due to its various advantages mentioned above.

1.2.3.1 Comparison of Klystron, IOT and Solid-State Amplifiers

Nowadays, the popular RF devices for particle accelerators are Klystron, IOT and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). It is worthwhile to make a comparative discussion for the RF power amplifier systems, based on these three devices. Klystron amplifiers essentially operate in Class A, where the DC input is independent of the RF drive. For the zero RF drive there is no RF output, although at the full DC bias. To prevent a possible destruction due to the heat dissipation at the collector, it is necessary to interlock the DC bias with the RF drive. Whereas, for the IOT amplifier, operating in Class AB/C, there is no current at the collector, unless the RF input is non-zero. This occurs because in the IOT the control grid is DC-biased to cut-off the cathode-current. Similar situation is seen for the MOSFET based SSPA. The Klystrons do offer the advantage of high-gain, typically between 40 and 50 dB. Although such high gain can make them susceptible to the RF feedback from a DC-isolated collector to the RF input, resulting in a phase instability and self-oscillation. The IOT and SSPA are less sensitive to these issues, as they have a moderate power gain. In the IOT, a bunched beam is produced directly from the cathode region, without the need for the gain cavities. Hence, it has typical gain of 23-24 dB. In the SSPA, the power gain depends upon distributed combining architecture of the corporate and binary combiners. Hence, it can be well managed as per the requirement, due to its inherent modular and scalable architecture. The variations in the output signal phase from a klystron are dominated by the small variations in the supplied beam voltage, where the phase deviation is related to the electrical length, and is typically 10° per 1% change in the beam voltage.

The IOT is electrically short, resulting in a phase pushing factor approximately 10% of a klystron, making it 20 dB less sensitive to the variations in the power supply voltage. MOSFETs, used in the SSPA, are superior to these two devices in this respect. The amplitude sensitivity to the beam supply variation is also different between the klystron and IOT [26]. The small voltage variations around the optimum value have minor effect on the output signal in an IOT than the comparable variations in a klystron. The fundamental frequency of the cathode current is directly determined by the RF input, and is relatively independent of the beam voltage. In both of these tubes, for a given value of the RF output, there will be an optimum beam voltage. Any value less than this voltage, saturates the output, leading to the excessive body current. On the other side, an excessive beam voltage produces higher collector dissipation.

Coming to the DC to RF conversion efficiency, the Klystron has a high value of typically 60%. However, it is highly dependent upon the drive power and the maximum efficiency available only at the saturation. The high amount of the DC power is needed for the klystron operation, even in no beam condition. This brings down the average running system efficiency to a value, as low as 20-33% [27] [28]. For effective control over the phase/frequency, the Klystron must be operated below its saturation point. This is not required for the IOT as well as SSPA, where there is a monotonic dependence of the output power on the input signal.

One more issue, which is favourable to SSPA, is the scheme for the RF feed/coupling port of the accelerating structure like RF quadrupole (RFQ). It requires a huge RF power of the order of hundreds of kW. However, the total power is not required to be coupled to this structure at a single port. Instead such structure has multiple RF coupling/feed ports due to electromagnetic field stability and practical limitation of high power couplers. Thus, even if such power is extracted in a single shot from an RF source, it needs to be divided for coupling all ports of such structure. In fact this makes the RF control difficult and costlier due to

the use of high power RF control components like divider, phase shifter and amplitude limiter. If a similar power is planned from the SSPA, multiple modular and scalable sources can be deployed. This alleviates the use of the costly and high power control components, and makes the overall system cheaper and efficient.

1.3 High Power Solid-State Amplifier

Motivated by the benefits of the SSPA [29], such as the low supply voltage, graceful degradation, low research cost, and a wide commercial technology base, it can serve as a promising candidate and better alternative to the vacuum tube based amplifiers. The potential advantages claimed for the SSPA in radar systems are its long failure-free life, low transmitter voltage, no risk of X-rays and electric shock, wide bandwidth and low projected volume-production costs. As a consequence, an increasing interest of both academic and industrial research communities is focused on its design methodologies. Partly, this was also possible in recent years with the practical advancement achieved for the superconducting cavity technology. Their price, performance and reliability are quite likely to improve [30] with the evolution of the wide band-gap semiconductors based devices [31] and the growing demand. Due to an overlap of the frequency regime for the wireless as well particle accelerator systems, the research effort, made for the SSPA is equally useful for these two arenas. Many institutes, including Soleil [32], ESRF [33], RRCAT [34], and APS [35], have developed such amplifiers, either as a fresh design or for replacing their vacuum tube counterparts. Along with obtaining the clean RF power (lowest phase noise and spurious), the SSPA failure rate, as reported from Soleil synchrotron, is 3% per year, including the infant mortality.

Since the first PA transistors in the 1960s, there have been steady advances in both the transistor operation as well as the semiconductor technology. Presently, a single laterally diffused metal oxide semiconductor (LDMOS) transistors can supply more than 1200 W peak power at UHF using 50 V power supply. Still, the output power from a single transistor at

RF, is not sufficient to cater the requirement of RF power in kW regime. RF transistors have very low input and output impedances which don't let their direct paralleling. Hence, in a kW level SSPA, this much power is produced by summing output power of multiple transistors, developed in the form of power amplifier (PA) modules, with the help of a power combiner. The RF input to each PA module is provided by a compatible power divider. Fig. 1.5 shows a typical amplifier architecture, realized using N-way (N=8) divider and combiner.

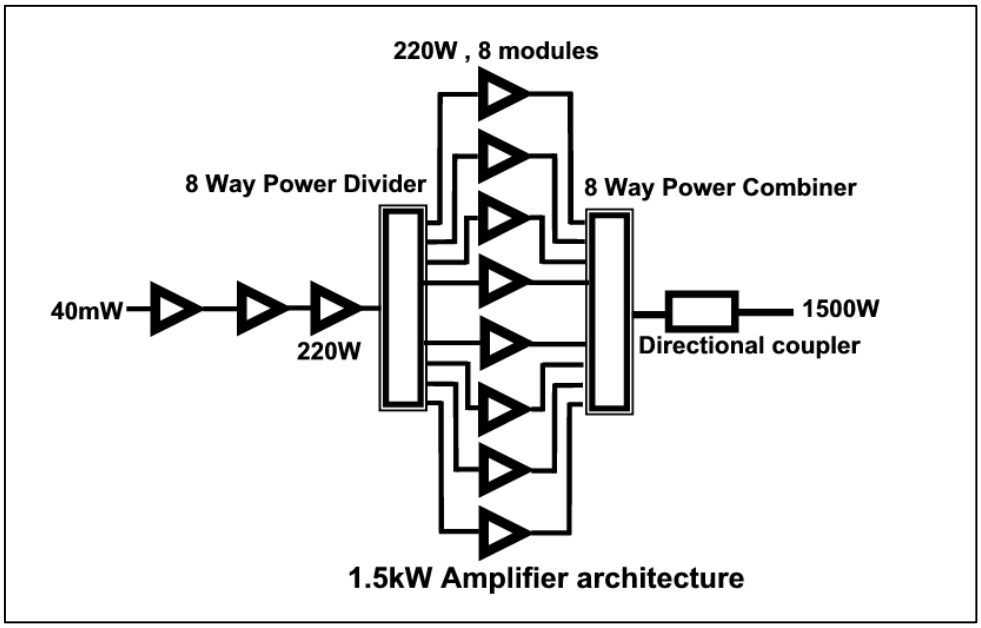


Fig. 1.5: Typical architecture of a high power solid state RF amplifier

Such schemes directly put an equal importance on the design of power divider and combiner structures, apart from the design of PA modules. Other than this, several directional couplers are needed in an SSPA system, unlike tube based amplifiers where only few of them are sufficient. These power couplers are useful for accurate measurement of the forward and reflected RF powers, at different stages. Hence, the investigation of high power solid state amplifier includes developing better design methodology for its building blocks and estimation/performance evaluation for the complete amplifier system.

Equipped with the DC biasing electrical system, cooling mechanism and control/supervisory elements, it makes a complete SSPA system. An RF PA module is an

elementary block designed with the RF transistor and mounted on a conducting metallic ground plane. It is equipped with the DC biasing network and input and output matching passive networks (IMN and OMN), as shown in Fig. 1.6.

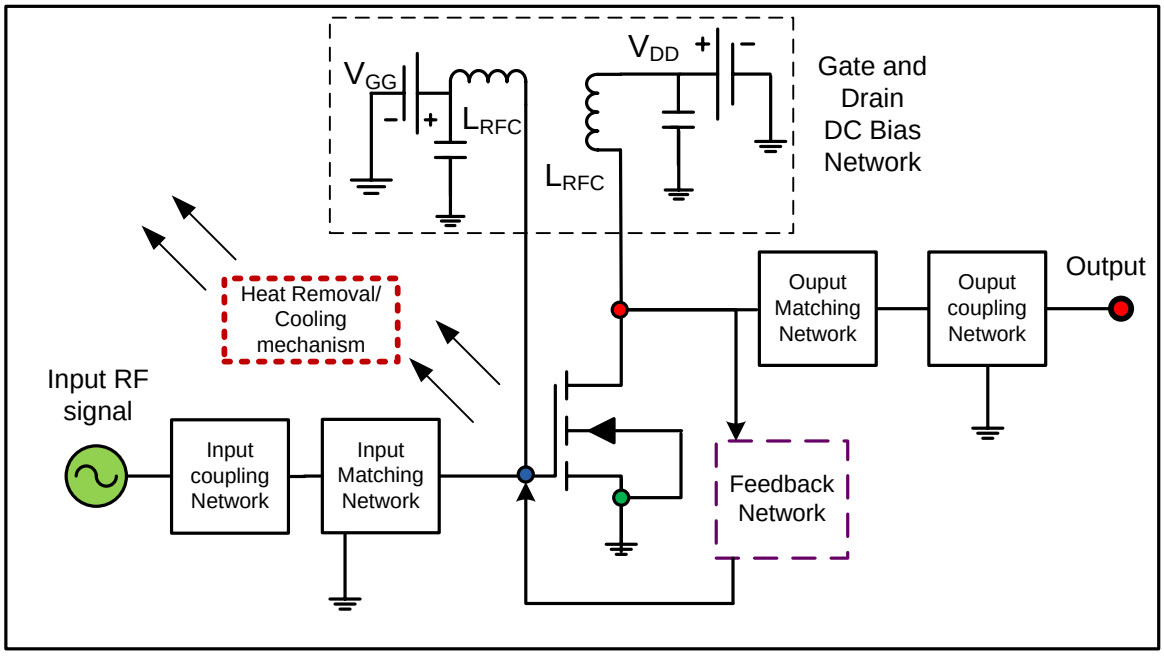


Fig. 1.6: Block diagram of a moderate level solid state RF PA module.

These networks transform the impedance at the transistor plane to the system or load plane. There are a variety of methods [36] for designing such network, depending upon the frequency range and required bandwidth. The high frequency (HF, 1–30 MHz) and very high frequency (VHF 30–300 MHz) power transistors are best matched with the discrete LC networks for the narrowband applications and transmission line transformers for the broad-band applications. The UHF transistors are matched with the planar micro-strip and transmission line transformers, or combinations of these two. For the HF to UHF frequency range, transmission line transformers are by far the most versatile matching technique as they are architecturally identical, regardless of where in the frequency spectrum they are applied. In addition to their wide bandwidth capability, they have the ability to convert an unbalanced signal to a balanced drive, required for the push-pull LDMOS transistors. They can be tailored for specific transfer function and impedance matching.

The input and output coupling capacitors are chosen to block the DC signal and to provide a minimum capacitive reactance at the lower end of the amplifier's frequency range. These capacitors must maintain resonance free operation across the amplifier's operating band. Capacitor manufacturers' data sheets usually show its typical series resonance performance curves over a particular frequency range. RF chokes are employed to deliver the DC operating bias and to decouple the RF signal from this bias supply. As in the case of coupling/decoupling capacitors, the RF chokes should also exhibit a resonance-free operation, in the desired frequency regime. Although the SSPA system does not require high voltage, it does require large current, perhaps several thousands of amperes systems. Apart from these circuit elements, an RF circulator (not shown in figure) is also used to protect the transistor and to decouple the module from other components during any failure.

While generally not considered a part of the RF PAs circuitry, the method by which heat is removed from an RF PA is equally vital. The improper heat removal can lead to the degradation of an array of RF performance parameters including linearity, efficiency, gain and stability. The heat accumulated in the transistor, during energy transformation from DC to RF, is removed by the forced air cooling or liquid cooling.

For various applications, desired features for an RF and microwave PA may vary. For particle accelerator, some of the important features are as follows.

- **Rated output power**: The RF PA must have enough output power capability to cater the requirement of the system under consideration.
- **Bandwidth**: The RF PA must have adequate operating frequency range to cover the intended application's spectrum. It should perform satisfactorily within this range.
- **Power gain**: The PA must have enough gain so that an optimum architecture of the SSPA can be realised by obtaining higher RF power for per unit volume of the space in the RF gallery. At RF and microwave, this gain is important rather than the voltage/current gain.

- **Amplitude and phase imbalance at output**: The PA must have minimum deviation in the amplitude and phase of its output signal, compared from a mean value of all PA modules, used therein. This helps obtaining a minimum power loss and good system efficiency, when these PAs are used as amplification/gain blocks in a multi-stage *divide and combine* scheme, for obtaining very high power.
- **Load VSWR tolerance**: Since multiple PAs are used in a typical SSPA using *divide and combine* scheme, their VSWR is important in order to drive other components/loads without any damage due to the reflected power. Generally a circulator is incorporated with the PA to accomplish this task.
- **Stability and spectral load pull**: The PA must be unconditionally stable in operation. It should not oscillate by driving an adverse load VSWR. It also should not get damaged at high power levels, for expected spectral range of the load impedances as well.
- **Linearity**: A linear response of the PA helps achieving the power/gain control easily by the LLRF unit. Its 1-dB compression point should be well above the required output power. Apart from the device technology, selection of the bias point and output terminations of transistor decides its linear range of operation.
- **Radiated emissions and susceptibility**: The RF PA must not interfere with or have its own operation impaired by other RF equipment. It must be adequately shielded for the EMI. The emitted radiation must be well below the safe limit, prescribed at the selected frequency. For this purpose its mechanical enclosure should be designed appropriately.
- **Mean time to failure**: The amplifier, above all, must be reliable, as particle accelerator's operation will depend on it. To ensure this, the transistor's die temperature must be kept as low as possible. The cooling system used for the PA must keep it cool all the time, specifically when operated below its optimum point. In such operating regime, the power dissipation in the transistor increase due to de-rating of the transistor's thermal resistance.

1.4 Literature Survey

The RF and microwave electronics may be dated back to the pioneering work of H. Hertz [37] and J. C. Bose [38]. In the early days of communication (1920), the RF and Microwave power was generated by thermionic tubes. During World War II, the urgent need for high power microwave generators for radar transmitters led to the development of the magnetron to its present state. In 1939 Varian brothers [39] gave the exact description of the multi-cavity klystron [40]. They derived the name klystron from the Greek verb *koyzo*, which describes the breaking of waves on a beach. The analogy is to the peaking of the electron density at the point of maximum bunching.The Vacuum tube power amplifiers [41], based on tetrode and pentode were also popular till 1970s. At the end of 1970, solid state RF devices began to appear. Their dominance in 1980 started a new era in communication applications [42]. These devices were used initially at much lower power (less than few hundreds of watts) and at much higher frequency bands [43] [44].

Using multiple pulsed microwave devices and planar radial 14-way power divide/combiner, an SSPA operating at 12 kW (pulse) in S band, was reported in late 90s, for the radar surveillance [45]. For particle accelerator applications, in 1999, 1 kW MOSFET amplifier at 500 MHz was developed by T. Ruan [46] at LURE, Orsay France. In the same year, a 4 kW driver amplifier (39-80 MHz) was reported at FNAL [47]. Advent of the superconducting RF cavities [48] in the particle accelerator and the operating advantages of solid state technology, triggered a chain reaction for achieving higher power amplifier, for directly energizing the superconducting structures. In collaboration with the LURE laboratory, Scarpa [49] reported the development of a 2.5 kW amplifier operating at 352 MHz. Following the same approach, in synergy with this project, two other amplifiers were reported, one at 352 MHz for Soleil [50] and another one at 176 MHz [51] [52], for Brazilian light source. In Soleil, an SSPA at 35 kW [53] [54] was used to power its booster machine, where a 5 cell

copper cavity of the LEP (in CERN) type was used. Growing virtue of the SSPA was seen in the third workshop on high power RF systems for accelerator [55]. The operation status of the SSPA system in Soleil was reported in 2006 [56] [53]. Major breakthrough was achieved by operating the superconducting cavities of storage ring in Soleil, using a 180 kW SSPA. For INFN and LNL, an effort was made to reach to the higher power of 10 kW SSPA [57]. In ESRF [33], an installation of solid state amplifiers is on the wheels for replacing their 1 MW Klystron. In recent years the solid state RF power source research [58] has been reported for various particle accelerators like APS [59], XFEL [60] and TRIUMPH [61].

The SSPA architecture depends upon the multiple solid state power modules, suitably power combined using a power combiner. For its investigation, the research activities for these two constituents need also to be probed. For solid state power modules, the traditional mode of operation like Class B, [62] Class F [63] etc. have been very popular. The Class B mode with a half sinusoidal current waveform has the same fundamental RF component but with reduced DC power consumption. The ideal Class F amplifier has the non-overlapping voltage and current waveforms in conjunction with a short circuit at the even harmonics and an open circuit at the odd harmonics. Due to the zero dissipation in the device and no harmonic power consumption, a maximum theoretical efficiency is obtained. However, in practice, due to the finite harmonics and an accurate tuning required for the nonlinear output capacitor of the transistor, the efficiency degrades. The Class F^{-1} PA, with a nonlinear capacitor, delivers better performance due to its large fundamental voltage, resulting in a higher fundamental termination, which is easier to match for the power devices. However, with the same drain bias voltage, the Class F^{-1} has a larger peak voltage than that of the Class F, leading to the reliability problem due to breakdown of the power devices [64]. These modes require the output impedance matching circuit to present a short/open termination to the relevant harmonics. This termination may not be practically feasible for high power amplifi-

ers. Another efficient mode of operation *viz.* switching mode PA [65], exploit the nonlinear region (switching behaviour) of the device to impose an efficient set of non-overlapping voltage and current waveforms at the drain of the transistor. For high power PAs (> 100 W) switch mode operation become difficult for LDMOS transistors, due to the high value of the output capacitor. Further, unlike the transistors used in the mobile handset/base stations, high power devices do not have luxury of affording a peak operating voltage, as required for the switching mode PA, in excess of 3-3.5 times of the drain supply voltage.

The development of emerging 4G (fourth generation) wireless systems and increasing use of the solid state power source in modern particle accelerators have necessitates the better design approaches, for high efficiency and high power amplifiers, going beyond the traditional modes of operation. One of these approaches includes the possibility of taming the harmonics [66] in the output matching circuit with classical modes of excitation. Some of these multi harmonic [67] controlled modes [68], termed as continuous modes [69] [70] [71], extend the fundamental/harmonic impedance space over which power and efficiency performance of traditional modes can be maintained. For example, the continuous formulation [72] identifies that the Class B and Class J [73] [74] are alternative solution of the same mode of operation; thus having the same efficiency and output power. Similarly, the continuous operation of the Class F mode alleviates the problem of presenting a short circuit at the even harmonics and an open circuit at the odd harmonics, whereas maintaining the RF power and efficiency similar to the Class F mode.

A multi-way *divide and combine* architecture [53] is adopted in a high power SSPA system. The N-way power combiner, in such architecture, needs to handle a high power as it sums the output signals from multiple amplifier modules. Its insertion loss and any imbalance [75] in the forward transmission coefficient, directly affect the transmitter efficiency [76]. It governs [77] the graceful degradation [78] performance and thus the available output power

of the transmitter [79]. The N-way power combiner [80], where power combining action is achieved in a single step, proves to be very efficient compared to the tree [81] and travelling wave [82] [83] type schemes. The popular N-way power combining families include the resonant [84], non-resonant [85] and the spatial [86] type combiners. The last one, using the free space as a power combining medium, is preferred near millimetre-wave frequencies. It is to be noted that a majority of the particle accelerator RF source operates somewhere in the VHF to S band. In the resonant combiners, the use of a peculiar shape for the structure with size comparable to wavelength, leads to a frequency-dependent field patterns in the structure, resulting in a resonant mode spatial distribution [87]. By properly spilling-out the resonating energy, through the branch ports, located at suitable positions, it is possible to perform the power combining functions. Such combiners [88] are narrow band and their performance is very sensitive to its structure's dimensions. Among non-resonant type, N-way Wilkinson combiner [89] is one of the widely adopted power combining structures. Its many modified versions [90] [91] [92] were reported in the literature. Apart from the Wilkinson type, several other approaches, including sector shaped [93] and exponential [94] combiners, were proposed for the N-way topology. The operation of the Wilkinson type combiners is limited in power due to the embedded nature of the floating isolation resistors (and their connection) due to the increased energy dissipation requirement. Gysel [95] provided a solution for such problem by modifying the circuit topology so that a grounded resistor can be used instead of the floating one. Being grounded, its power rating can be made very high and it can be placed and cooled outside the main circuit.

Another popular N-way topology for high power is the radial combiner [96] [97] [98]. All of the radial combiners have one circuit element which distributes the electromagnetic energy in the radial direction, and this element characterizes the type of combiner. One of the first radially divider/combiner was developed by Schellenberg [99] for an X-band applica-

tion. It was composed of a coaxial transformer and a microstrip line. A different approach, using a radial waveguide and a coaxial transformer, was followed by Belohoubek [100]. Fathy [101] outlined a simplified approach for the radial combiner, incorporating a isolation resistor and quarter wave resonators in the microstrip configuration, followed by its physical verification at 12.5 GHz and 30 W of power. Villiers [102] presented a Transverse Electro Magnetic (TEM) conical transmission line based power combiner for X band. Regarding the electrical design of such a device, the design parameters of the coaxial probes are not accurately defined in the closed-form solutions and must be determined by the analysis, using an electromagnetic field solver. However, since the characteristic impedance of the conical line is known and it is constant, the rest of the design, including the design of the coaxial transformer, can be carried out using standard transmission-line models provided the impedance of the coaxial probes are known. These coaxial ports are spaced far apart and are easily accessible. Recently, a radial coaxial waveguide based power combiner [103] at 4 GHz was reported with a door-knob and L shaped branch port design. However, difficulty, encountered during its fabrication and assembly, degrades its combining efficiency. Also high power test results were not reported therein. Majority of the reported techniques are suited for low power [104]. At high power, the conventional microstrip line based power combiner cannot be used due to their poor power handling capacity. Further in UHF band, the waveguide based combiners [105] [106] [107] are rather bulky. Majority of these techniques are suited for the low power and mid microwave range of the frequency.

Similarly, the design of high power directional couples [108] is not available readily in the literature. The reported designs are based on planar transmission line with limited operating power handling capacity. In order to control amplitude and phase imbalance in different RF components of an SSPA system, design should be also repeatable in performance.

1.5 Motivation for Present Research Work

The RF and microwave power amplifiers are at the core of nearly all high-power applications. For many years, the vacuum tube based RF power amplifiers were ideal choice for the particle accelerator. However, in recent years with the practical advancement in the superconducting cavity, the solid state technology based amplifiers have become promising candidates for particle accelerators due to their numerous advantages. SSPA's modularity, inherited from its architecture, may make fitment of different power levels inside the same system, with mass production of its elementary blocks. For a typical electron SRS with beam energy of 2 GeV and beam current of 200 mA, more than 200 kW (average) of RF power is required for its operation. For SNS [109] and ADS [110] applications, the total RF power requirement may be of the order of many MWatts. In order to fulfil such huge power requirement, the evolving landscape of SSPA dictates the strategy for its design, fabrication and optimization. With suitable academic efforts, the wide zone of SSPA design, mainly driven by the communication segment, needs to be narrowed down to cater the requirements of the particle accelerator.

Major constituent blocks of a typical high power solid-state amplifier are power amplifier modules, power combiner, dividers and directional coupler. Thus, its investigations involve at the component level, for better efficiency, design repeatability and higher output power; and at the system level, for the improved reliability and graceful degradation.

Most of the PA modules' design using the harmonic shorted [62] and harmonic tuned modes [66], reported in the literature, are aimed for the cellular phones and base stations. Such designs require an average RF power of less than 100 W. Hence, the wave shaping [111] of the voltage waveform at the terminals of the transistor is possible by selecting such device, much higher in voltage/current rating than the actual requirement. When higher power designs are planned, the optimum calculated values of voltage/current often exceed the

maximum rating of the transistor. Hence, sub optimum solutions lies in exploring newer continuous modes [112] or multi- mode [113] operation of the transistor. They are derived from the popular modes like Class B, Class, J [74] and Class F [69]. For high power design, the inclusion of the nonlinear output capacitor [114] in the design is necessary. Its value is significant for LDMOS transistors [115], which is a workhorse for the PA design. Therefore it is necessary to formulate a design procedure for high power PA, in terms of the waveform shaping coefficients for such newer modes.

Coming to the power combining domain, the design of a multi-way radial RF combiner [116], capable of handling kW level of power, is not available readily in the literature. The reported combiners [103] are for the low power and higher frequency range, mostly beyond S band. For particle accelerators, the combiner operation in kW regime and at comparatively lower frequency is required. Also it should be compact, reliable, and efficient. Similarly, a variety of designs for the directional coupler are available in the literature, including planar (strip-line and microstrip), waveguide and coaxial types. The planar couplers have attractive characteristics, useful for a variety of applications, but they are affected by the significant insertion losses and operate at the low power. Most of the coaxial couplers are loop coupled, posing a problem to achieve/tune for the required coupling and directivity. Hence, an improved version of the directional coupler needs to be explored.

A kW level SSPA system is an impedance-matched integration of these RF components. To date, its system level design and real time performance analysis is not available readily. Due to minute deviations from the ideal performance, exhibited by these components, the real time SSPA system architecture has many post-integration performance issues. In particular, issues pertaining to the amplitude and phase imbalance, among different building blocks, are important and needs to be investigated.

Thus, the purpose of this research work is to investigate the newer design techniques and topologies for power amplifier module, power combiner/divider and directional coupler, followed by their suitable experimental verification. This research work will contribute to an indigenous design of the future RF systems with an improved performance in terms of the efficiency, power, ease of fabrication and hence, the cost.

This chapter discussed briefly about application of high power RF and microwave amplifiers, particle accelerator and its typical RF system. Major prevalent technologies available for high power amplifier were discussed. In particular solid state technology was highlighted with its advantages and comparison with the popular technologies of Klystron and Inductive output tube. It was followed by a literature survey for important constituent blocks of high power solid state amplifier. Finally, motive behind this work was discussed in detail with suitable comparison along with the available literature.

Chapter 2. Harmonic Shorted Solid State Power Amplifier

The SSPA system for an accelerator, as discussed in the last chapter, is an ensemble of the solid state PA modules, power combiners/dividers, power couplers and other ancillary units. The PA module, being the main gain block, determines the system linearity, efficiency and power consumption. In order to design it at a high power, the pertaining issues like RF transistor selection, device model, load line, its operating mode and device parasitic effects are necessary to study. In this chapter, after reviewing these issues, the design and experimental verification are presented for the UHF low power and high power PA modules, operating in classical A, B and AB modes with the shorted harmonics at the output.

2.1 Selection of RF Transistor for Power Amplifier

In general, the selection of the high-power RF transistor [120] depends upon its intended application. Its application space is broad and growing, ranging from the ubiquitous cellular base station to avionics, broadcast, industrial, scientific and medical. Its selection is enumerated and qualified in terms of its technical features [121], like the power gain, output power, linearity, efficiency, reliability, thermal management, bandwidth, ruggedness and, last but certainly not the least, its cost. Till today, these features, for the commercially available transistors, are highly influenced by the requirements of communication systems. Hence, for particle accelerator applications, its selection demands proper trade-off among these features.

At the outset, solid state devices [122] for RF PA fall into two distinct physical kingdoms , the Bipolar Junction Transistors (BJT) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Thought the BJT devices served the purpose for a long time, but with the requirement for linear, powerful and high gain transistors, it was relegated in the early 1990s. Perhaps for the RF power devices, a weak spot with the BJTs is a possibility for

thermal runaway. This problem is absent in the MOSFET devices. This is because the combined effect of the inversion layer mobility, trans-conductance and the threshold voltage in a MOSFET, do not favour for the increase of the drain current with increasing temperature [123]. Their cost and performance trade-off of provide a clear advantage at frequencies below 4 GHz. In present work, RF transistor referred during discussion, means a MOSFET device unless otherwise mentioned.

In recent years, wide bandgap semiconductors [124] such as silicon carbide (SiC), Gallium Nitride (GaN) [125] have received a great deal of attention [126] for the fabrication of UHF power transistors. These semiconductors have bandgap energies about two to three times those of conventional ones such as Si, GaAs, and InPGaN. These days, the GaN is a preferred choice for the RF power MOSFETs due to its unique high electron mobility and the high critical field strength of this material. The SiC wafers still have a too high cost to be fully cost efficient. Coming to the structure [127] of the power MOSFETs, the vertical double-diffused MOSFET (VDMOS) and the Laterally Diffused MOSFET (LDMOS) structures are popular ones (Appendix A). Since early 1990s, the LDMOS [115] has gained wide acceptance for PA applications in VHF to S-Band. Its topology has the advantage of placing the source terminal at the ground potential, with a geometry layout that improves its thermal performance and minimise its feedback capacitances, and source inductance. Many such advantages translate it into a device with higher gain, higher power density, and higher DC to RF conversion efficiency.

Many transistor manufacturers, like Freescale, NXP, Semelab and ST Microelectronics, are continuously striving for better and better device technology. Fig. 2.1 shows some of the frequently used LDMOS transistors, available from these manufacturers, for accelerator applications. Perhaps the wireless market has been the main driving force behind rapid and newer device technology emerging every quarter. While this market has standardized on a

drain bias of 28–32 V, high power LDMOS were developed using 50 V processes for other applications.

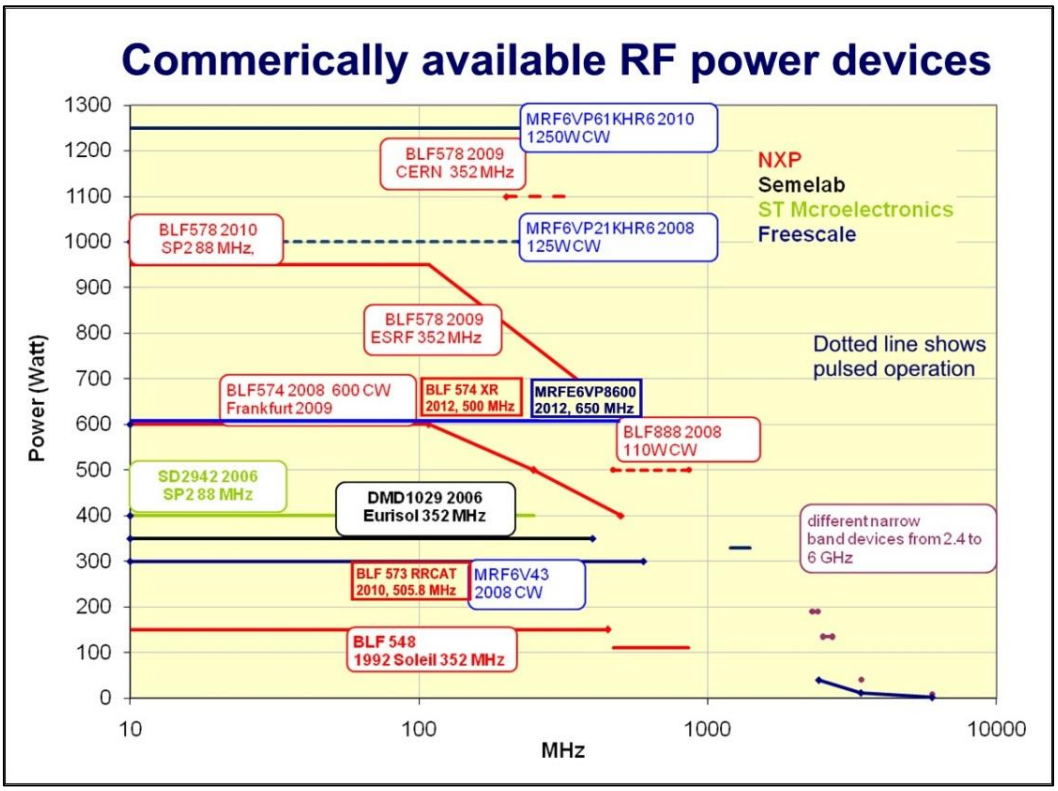


Fig. 2.1: Popular high power UHF RF transistors

2.2 Large Signal MOSFET Model

The power amplifier designer needs to weigh different options that trade off multiple device metrics. For this purpose circuit models of the transistors, that can help decide on the best approach, is essential. An important feature that a model must possess, for it to be a useful PA design tool, is the ability to predict the source and load impedance values that will produce a certain level of large-signal performance. This capability allows the designer to make the necessary trade-off of the performance in the impedance space. For *a-priori* circuit analysis, an RF MOSFET can be thought as a voltage controlled current source (equal to product of trans-conductance g_m and gate to source voltage V_{gs}) with zero output conductance and zero turn-on or knee voltage V_k, as shown in Fig. 2.2. The corresponding IV characteristics are shown in the right part of this figure. The drain current (I_{ds}) exhibits cut-

off (for input voltages below threshold voltage V_T) and reaches a maximum, or open-channel, condition where further increase of gate-source voltage results in little or no further increase in I_{ds} (hard saturation). The maximum drain-source voltage V_{ds} is indicated by V_{max}. The maximum I_{ds} allowed, corresponding to the maximum value of V_{gs}, is indicated by I_{max}.

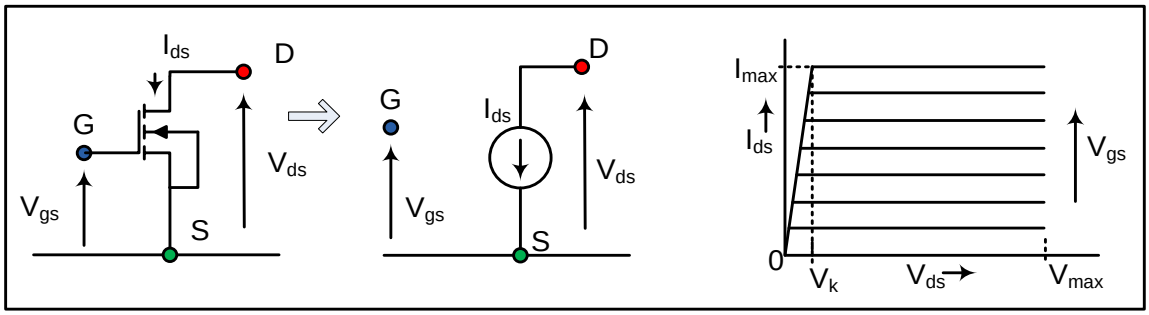


Fig. 2.2: MOSFET with its ideal circuit model and IV characteristics

These characteristics are highly ideal. They are based on following assumptions:

- Abrupt cut-off of the I_{ds} when the gate voltage drops below V_T and saturation of the current above a defined value of (I_{max}).
- Linear relationship between output current and input voltage between these limits.
- Quasi-static behaviour (same IV characteristics regardless of sweep speed).
- Negligible impact of the knee region (V_k ~ 0).
- Resistive output impedance at current source plane (across drain-source terminal).

The PA design and analysis is generally started with the ideal model, shown in Fig. 2.2, with validity of analysis results up to current source plane. Once key results are obtained, the PA design needs to be fine-tuned using more sophisticated large signal model usable in the circuit simulator. One such model, shown in Fig. 2.3, consists of input capacitor (C_{IN}), input resistance (R_{IN}), nonlinear voltage-controlled current source, nonlinear output conductance (g_{ds}), and output capacitor (C_{OUT}). More sophisticated models can also be implemented in the simulator using equivalent circuit components, but now the component parameter values are dependent on the large-signal voltages.

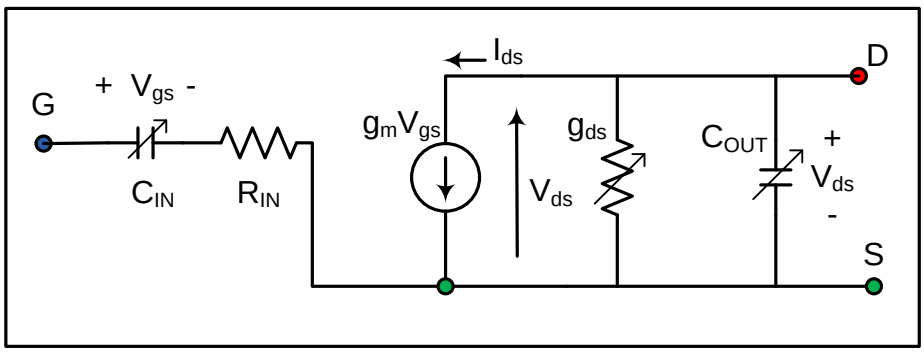


Fig. 2.3: MOSFET circuit model with nonlinear components

The first electrical equivalent models useful for simulation, for MOSFET, were the SPICE Junction models [128]. With the advent of VDMOS and LDMOS transistors, there was a renewed interest in the development of compact models like the popular Curtice [129] model and Statz or Raytheon [130] model, and more general-purpose models such as the Materka [131]. Majority of such models were extensions of the small signal equivalent circuit model, based on the intuitive association of the circuit elements with the physical structure of the transistor. Generally, in these models the DC drain current characteristic is a hyperbolic tangent function of the drain-to-source voltage, with some polynomial or other function of the gate-to-source voltage to describe the gate control. Other parameters are added [132] to account for the finite output conductance, near and sub-threshold behaviour, gate-leakage currents, and so forth. A generic drain current equation [133] is:

$$I_{ds} = \beta_m (V_{gs} - V_T)^{\gamma_m} \tanh(\alpha_m V_{ds}) (1 + \lambda_m V_{ds}) \tag{2.1}$$

Here α_m controls the knee region sharpness; β_m is related to the maximum I_{ds}, γ_m is traditionally equal to 2 (the MOSFET square-law characteristic) and λ_m term describes the finite output conductance. Any or all of the model parameters have been given further functional dependences on V_{ds}, temperature, and so forth, in attempts to obtain more accurate fitting of the DC curves. For LDMOS devices, the Motorola electro-thermal (MET) model [134] is virtually the industry-standard model. It is an empirical large-signal nonlinear model, which contains a drain current description that is single-piece and continuously differentiable,

and includes static and dynamic thermal dependencies. Thus, it is capable of accurately representing the drain-source current-voltage characteristics and their derivatives at any bias point and operating temperature. Though, it can predict the DC, S-parameters [135] and the large-signal behaviour, modifications to the gate control function, proposed by Fager [136], are claimed to improve the model's ability to predict distortion products for power amplifier applications.

2.3 Classical Design Approach for RF Amplifier

The schematic of an RF power amplifier is shown in Fig. 2.4. Here, L_{RFC} is an ideal DC short-circuit and C_b is an ideal DC-blocking capacitor; both used as part of the biasing network. The drain bias supply voltage is V_{DD}. Let V_q be the quiescent DC bias voltage applied to the gate with the help of DC voltage supply V_{GG}. Different classes of operation are possible depending upon this bias voltage. Each such Class projects a specific set of efficiency, linearity, input drive power requirement and circuit complexity. Let V_s be the amplitude of the input sinusoidal RF signal (V_{in}), applied to the MOSFET through the input matching network. The PA, performs amplification of this signal, while converting some part of the DC power (P_{DC}) from the bias supply into the RF power (P_1) at the fundamental frequency, delivered through an output matching network. The rest of DC power is dissipated as heat in the transistor and other circuit elements having small but finite resistive and dielectric losses. Such a power conversion mechanism is described by the DC to RF conversion or drain efficiency (η_{pa}). The harmonics are present only at the output of the MOSFET and they are assumed to be generated by its non-linearity.

The classical design theory [137], suited for small signal linear amplifier, is based on the scattering (S) parameters of the transistor. Mason [138] and Rollet [139] originally came up with the analysis of S parameter, targeted for complex conjugate match [140] in small signal RF amplifiers. The key results can be examined with reference to Fig. 2.5.

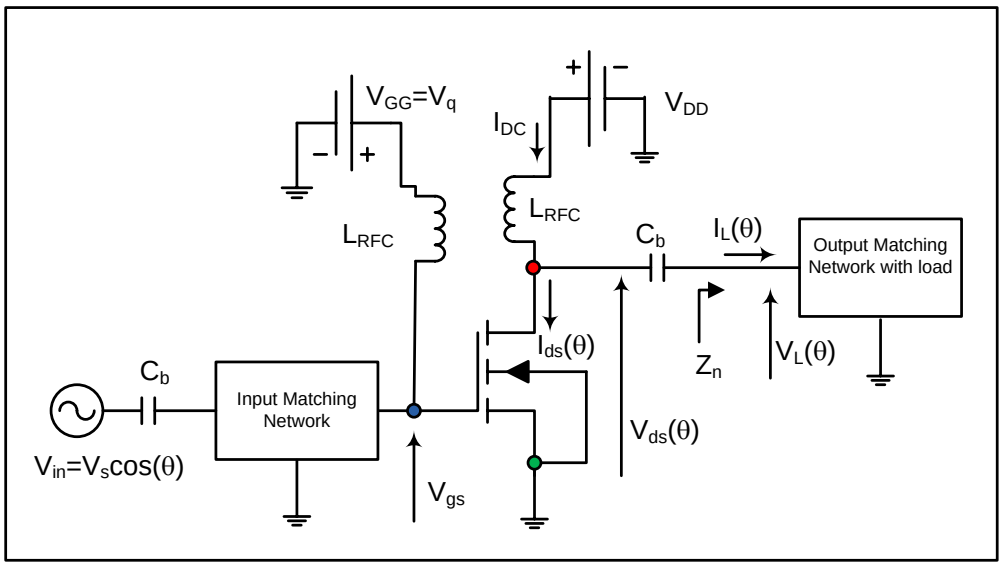


Fig. 2.4: Simplified PA scheme with bias and impedance matching networks

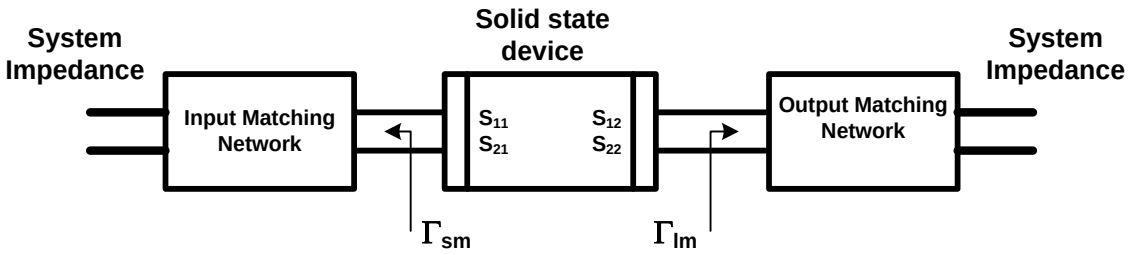


Fig. 2.5: Scattering parameter model for a solid state RF amplifier

Here, the input and output matching networks [36] are assumed to be realized using passive components. In order to focus on complex conjugate matching, the bias network is omitted here. In terms of S parameters, expressions for the stability factor k_s and optimal passive source and load termination, based on complex conjugate match theory [141], are

$$\Gamma_{sm} = \frac{C_1^{*}\left[B_1 - \sqrt{\left(B_1^{2} - 4|C_1|^2\right)}\right]}{2|C_1|^2} \tag{2.2}$$

$$\Gamma_{lm} = \frac{C_2^{*}\left[B_2 - \sqrt{\left(B_2^{2} - 4|C_2|^2\right)}\right]}{2|C_2|^2} \tag{2.3}$$

$$k_s = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta_s|^2}{2|s_{12}s_{21}|} \tag{2.4}$$

Where

$$B_1 = 1 + |s_{11}|^2 - |s_{22}|^2 - |\Delta_s|^2$$
$$B_2 = 1 - |s_{11}|^2 + |s_{22}|^2 - |\Delta_s|^2$$
$$C_1 = s_{11} - \Delta s_{22}^*$$
$$C_2 = s_{22} - \Delta s_{11}^*$$
$$\Delta_s = s_{11}s_{22} - s_{12}s_{21}$$

If k_s>1 and $|\Delta_s| < 1$, the amplifier will never oscillate for any passive input and output termination. The complex conjugate match is good enough and promises *a best possible* design for the small signal devices biased for the full cycle conduction of I_{ds}. For high power PA design this theory may not suffice due to several reasons. In actual circuit realization, the circuit losses in impedance matching network can tune k_s and in practice transistor can be used below unity k_s point safely. The transistors with higher k_s tend to have lower gain. If the gain drops a certain limit, extra input drive power required to get designated output can mitigate the advantage of complex conjugate matching. The circuit environment in which device is placed can play with k_s factor. It must be noted that the efficiency predicted for classical theory is valid if the input drive is sufficient to make full excursion of voltage and current as per transistor's IV characteristics and sufficient harmonic trap is provided in the circuit. Even if it is sufficient, it is possible that the corresponding value of voltage/current may exceed transistor's breakdown values. Hence, for a large signal amplifier a better point to start the design will be the estimation of an optimum load based on the maximum voltage and current excursion possible at the output port of the transistor.

2.4 Load Line Approach

If the conjugate match condition is adopted for the PA to operate into the large-signal regime, two possibilities, shown by dynamic load lines A and B drawn upon IV characteristics of a MOSFET (Fig. 2.6), are quite likely. Load line A, with larger value of the load, results in reduced current swing and sudden compression of the transistor output power (voltage-limited operation). On the other hand, if the external load is selected in order to fully exploit the maximum current swing, (line B), a reduced voltage swing is produced (current-limited

operation), again driving the transistor output into compression. Similarly, for the voltage swing, the limitation is related to the ohmic behaviour and breakdown, both channel and gate-drain junction related.

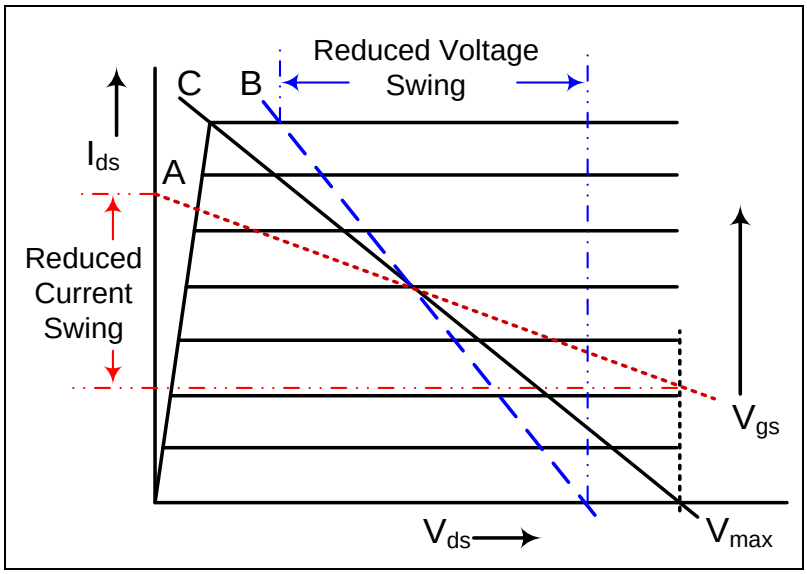


Fig. 2.6: Drain current and voltage plot with load line

Collectively, such constraints pose an upper limit to the maximum swings that output current and voltage may experience, reflecting in a corresponding limit to the device output power generation capabilities. The optimum situation is clearly in the simultaneous maximization of current and voltage swings, resulting in line C in above figure. This is often referred to as a load-line matching condition or power match condition [73].

Its mathematical formulation can be carried out with reference to the PA schematic, shown in the Fig. 2.4. Let MOSFET used in this PA is represented by the ideal model of Fig. 2.2. Here, the drain-source voltage $V_{ds}(\theta)$ is allowed to breach between V_k (lower limit) and V_{max} (upper limit). In order to fully utilize costly devices, V_{max} is up to breakdown voltage of the transistor. With the present device technology, V_{max} is up to 2.5 times of V_{DD}. The knee voltage V_k is usually some fraction (~ 0.1 to 0.2) of V_{DD}. Assuming steady-state conditions, the time-domain current and voltage waveforms at the device output (drain) are expressed through their Fourier series expansions [111] as

$$V_{ds}(\theta) = V_{DD} + \sum_{n=1}^{\infty} [a_{vn} \cos(n\theta) - b_{vn} \sin(n\theta)] \quad (2.5)$$

$$I_{ds}(\theta) = I_{DC} + \sum_{n=1}^{\infty} [a_{in} \cos(n\theta) - b_{in} \sin(n\theta)] \quad (2.6)$$

Where $\theta = 2\pi f_1 t$, and f_1 is the frequency (fundamental) of the RF signal. At load terminal, the voltage and current are

$$V_L(\theta) = \sum_{n=1}^{\infty} [a_{vn} \cos(n\theta) - b_{vn} \sin(n\theta)] \quad (2.7)$$

$$I_L(\theta) = -\sum_{n=1}^{\infty} [a_{in} \cos(n\theta) - b_{in} \sin(n\theta)] \quad (2.8)$$

Thus fundamental and harmonic load voltage and current components (at $f_n = nf_0$) are expressed as

$$V_L(f_n) = a_{vn} + j\, b_{vn} \quad (2.9)$$

$$I_L(f_n) = -a_{in} - j\, b_{in} \quad (2.10)$$

Moreover, any voltage (current) harmonic component is obviously related to the respective current (voltage) harmonic through the load impedance at the transistor's output port at harmonic frequency

$$Z_L(f_n) = \frac{V_L(f_n)}{I_L(f_n)} \quad (2.11)$$

Time averaged power delivered to load at f_n is

$$P_{out}(f_n) = \frac{Re\{V_L(f_n)\, I_L^*(f_n)\}}{2} = -\frac{(a_{vn}\, a_{in} + b_{vn}\, b_{in})}{2} \quad (2.12)$$

For simplicity $Z_L(f_n)$ and $P_{out}(f_n)$ may be denoted by Z_n and P_n respectively. For some calculation, the polar form seems useful. Hence, (2.5) and (2.6) can be rewritten as

$$V_{ds}(\theta) = V_{DD} - \sum_{n=1}^{\infty} [V_n \cos(n\theta + \psi_n) \quad (2.13)$$

$$I_{ds}(\theta) = I_{DC} + \sum_{n=1}^{\infty} I_n \cdot \cos(n\theta + \xi_n) \quad (2.14)$$

ψ_n and ξ_n are the phases of the voltage V_n and current I_n ; n^{th} harmonic component amplitudes respectively. Also V_n and I_n are related with *a* and *b* coefficients as

$$a_{vn} = -V_n \cos(\psi_n)$$
$$b_{vn} = -V_n \sin(\psi_n)$$
$$a_{in} = I_n \cos(\xi_n)$$
$$b_{in} = I_n \sin(\xi_n)$$

While plotting graph, normalised waveforms of voltage and current are convenient to deal with. These normalised waveforms are defined as

$$\frac{V_{ds}(\theta)}{V_{DD}} = v_{ds}(\theta) = 1 + \sum_{n=1}^{\infty} [a_{vn} \cos(n\theta) - b_{vn} \sin(n\theta)] \tag{2.15}$$

$$\frac{I_{ds}(\theta)}{I_{DC}} = i_{ds}(\theta) = 1 + \sum_{n=1}^{\infty} [a_{in} \cos(n\theta) - b_{in} \sin(n\theta)] \tag{2.16}$$

The corresponding polar form representation becomes

$$v_{ds}(\theta) = 1 - \sum_{n=1}^{\infty} [v_n \cos(n\theta + \psi_n) \tag{2.17}$$

$$i_{ds}(\theta) = 1 + \sum_{n=1}^{\infty} i_n . \cos(n\theta + \xi_n) \tag{2.18}$$

The active power delivered from the device to the output matching network at the fundamental frequency (P_1) and harmonics (P_n) is defined as

$$P_n = \frac{1}{2} V_n . I_n . \cos(\varphi_n) = \frac{1}{2} Z_n {I_n}^2 . \cos(\varphi_n) \tag{2.19}$$

where $\varphi_n = \psi_n - \xi_n$. An alternate expression for this power calculation is

$$P_n = \frac{1}{2\pi} \int_0^{2\pi} Re(V_1 I_1)\, d\theta \tag{2.20}$$

For the scheme depicted in Fig. 2.4, the supplied DC power (P_{DC}) is given by:

$$P_{DC} = V_{DD} \cdot I_{DC} \tag{2.21}$$

Simultaneous voltage across (V_{ds}) and current through (I_{ds}) the drain is the primary source of power dissipation (P_{diss}) in a PA. It can be obtained by integrating and averaging over a period the product of current and voltage across the transistor, resulting in the following expression

$$P_{diss} = \frac{1}{2\pi} \int_0^{2\pi} V_{ds}(\theta) \cdot I_{ds}(\theta)\, d\theta \tag{2.22}$$

Alternately

$$P_{diss} = P_{DC} - P_{out} + P_{in} \tag{2.23}$$

Here P_{in} is the input power. The DC to RF power conversion or drain efficiency is

$$\eta_{pa} = \frac{P_1}{P_{DC}} \tag{2.24}$$

For low power PAs, the power added efficiency (PAE) is defined by deducting contribution of input power (P_{in}), specifically for low power amplifiers. It is given as

$$\eta_{pae} = \frac{P_1 - P_{in}}{P_{DC}} \tag{2.25}$$

The higher PAE implies the lower power dissipation in the transistor, with major effects in reducing thermal issues and increasing device lifetime. The additional parameters of interest include the drain waveform peaking factors as discussed in [142]. These factors relate the peak value of the drain waveforms to their respective DC components, and are defined as

$$\delta_V = \frac{\max[V_{ds}(\theta)]}{V_{DD}} \tag{2.26}$$

$$\delta_I = \frac{\max[I_{ds}(\theta)]}{I_{DC}} \tag{2.27}$$

These parameters give insight into the waveform peaking characteristics of different amplifier classes, allowing the designer to scale the DC bias voltage in order to operate within the physical voltage and current limits of the transistor. The output impedance (with reference to Fig. 2.4) at n^{th} harmonic frequency (f_n), using (2.14) and (2.13) can be rewritten as

$$Z_n = \frac{V_n}{I_n} \cdot e^{j(\varphi_n)} \tag{2.28}$$

Thus the fundamental RF load for in-phase fundamental voltage and current ($\varphi_1 = 0$) has a value of

$$R_1 = \frac{V_1}{I_1} \tag{2.29}$$

This optimum value is good enough at the current source plane. In actual device this value is transformed at its actual output plane due to its output capacitance, bond-wire inductance, and the package parasitic. Thus these effects need to be taken into account in designing the final output matching network design. This is a simple task for a linear circuit simulator. Selection of optimum voltage and current is a function of the device itself and the bias point. If the bias voltage is doubled, the output resistance is doubled for the same current swing. Equation (2.29) also states that for higher-power devices, those with larger maximum currents and same bias supply, the optimum load resistance becomes increasingly smaller. Similarly, an optimum source-impedance is also necessary.

2.4.1 Source/Load Pull Measurement

In general, under large signal operation, the load line concept can be used to match boundary conditions at the interface of the transistor input/output and system impedance. There is functional dependency of output power, efficiency, and intermodulation [143] on transistor input/output impedance. This dependency can be measured or simulated and results can be plotted on impedance plane as a function of PA characteristics like output power, efficiency etc. It is termed as source/load pull [144] measurement (Fig. 2.7). It is very useful for achieving power match of the transistor. Thus load/source pull study is devoted to the identification of the optimum as well as sub optimum performances of a PA in nonlinear regime at corresponding operating conditions. Load pull contours exhibit as flattened circles

on Smith chart for different power less than optimum one. The optimum power match usually comes at the centre position of these contours.

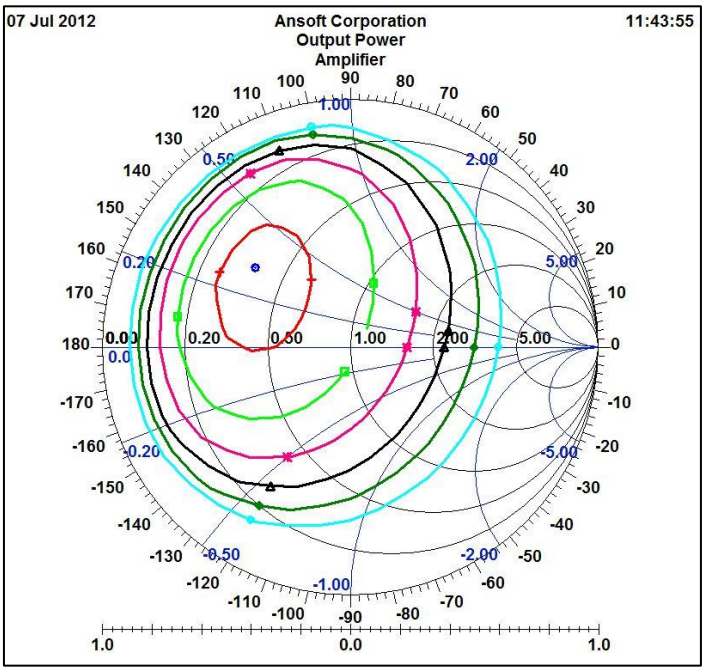


Fig. 2.7: Typical load pull measurement data on Smith chart

These contours are generated by connecting various sources/loads to the amplifier and by measuring or calculating the gain and output power at each value of source/load impedance (Γ_{source} and Γ_{load}), as shown in load pull scheme in Fig. 2.8.

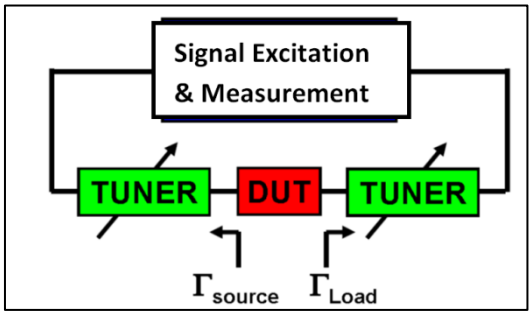
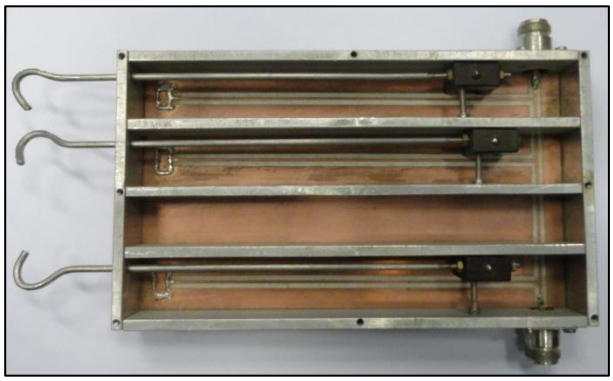


Fig. 2.8: Classical load pull set up to generate power contours on Smith chart

These are changed by passive tuners, like multiple stubs or slug tuners, having variable passive components. Passive tuners can be mechanical or electronic. Mechanical tuners are made of a piece of transmission line with a longitudinal slot in which one or two slugs are

inserted. One such triple stub tuner, designed for the present investigation using three microstrip transmission lines is shown in Fig. 2.9.



Brief Details

Length, Width: 20 cm, 11 cm

Outer Height: 3 cm, Inner depth: 2.5 cm

Stub: Microstrip type on TMM4™ Substrate

Plunger: manually moving shorting plungers

Input and Output Connectors: N type

Fig. 2.9: A passive microstrip line based slug tuner

The position of the slugs along the line, in each stub, controls the phase and the amplitude of the reflection coefficient, respectively. In automatic tuners, the same is done by means of stepper motors and vector network analyser (VNA), all controlled by a computer. In some cases like harmonically tuned amplifier design, in order to account for the nonlinear behaviour of the active transistor and thus the resulting harmonic generation phenomena, the source/load pull can be carried out at harmonic frequencies also (harmonic source/load pull).

The source/load pull measurement has the practical difficulty of measuring the load impedances at the transistor terminals because of changing reflection and possible damage to high power DUT. In such cases calculation/simulation of source/load pull contours is a useful design-aid. For a given choice of available power, the load impedance can be selected from load pull contours. In 1983, Cripps [145] showed that simple load line principles for a solid state device can be extended to predict load pull contours with proper de-embedding. The latter one is necessary in order to account package parasitic and nonlinear capacitors of the transistor. Once optimum source and load impedance are determined, the design of input as well as output impedance matching networks of the PA can be carried out. Along with this design, operating conditions including DC bias and input excitation are also important for the

PA design. These operating conditions are decided by the Class of operation or operating mode of PA as discussed next.

2.5 Operating Modes of RF Power Amplifier

PAs are normally classified on the basis of their *operating modes*. The term operating mode refers to different features which can be attributed to the PA design and characterization [62]. Such attributes include the bias point selection (Class A, AB, B or C), selection of matching network topologies (tuned Load, Class F, etc.) or the operating conditions of the transistor (Class E, Class S, etc.). Each set projects a specific efficiency, linearity, input drive power requirement and circuit complexity. Hence, the high efficiency PA modes can be divided mainly in three categories. The first one is harmonic shorted version with tuned load (TL), more popular known as Class A, AB and B modes [146]. In these modes, the identification of the quiescent bias point is performed in terms of transistor output current conduction angle (CCA), i.e. the fraction of the RF signal period where a non-zero current is flowing. In the second category transistor is driven into heavy saturation and it is considered as a switch (as ideal as possible). The Class D and E come under this switching-mode of operation [65]. It is related to the active transistor dynamic operating conditions and consequently to the matching network terminating conditions. The resulting PA could be more properly considered as a DC-to-RF power converter rather than an amplifier, since the input-output transfer characteristics are marginally considered. Such PAs have the potential for high efficiency, with drain efficiency theoretically approaching 100%. However, available power transistors are not ideal switches because of parasitic reactance, finite on-resistance, and limited gain.

Last category *viz.* Harmonic Tuning (HT) or multimode version, is influenced by continuous and multidimensional design or termination space. It is based on the harmonic terminations synthesized across the active transistor, by wave-shaping of output or drain voltage waveform to maximize output power, or efficiency or both. Examples of these classes

are the Class F [147], and newly suggested harmonically tuned modes like Class J [74] and extended continuous F [148]. These modes will be discussed in next chapter. In one variation of HT modes [149], a rectangular or half-sinusoidal gate voltage waveform is used to overcome the gain-loss mechanism, inherent in the Class-B or Class-F operation, due to full swing of the input drive signal. The harmonic shorted modes are popular ones and these are discussed next.

2.5.1 Harmonic Shorted Operating Modes

The concept of making an RF amplifier by biasing the transistor to a quiescent voltage/current and allowing the RF drive signal to swing it into conduction is familiar one. The conduction angle Φ of the transistor is the angle, measured in degrees or radians over one period, for which it remains conducting. Such classical modes are classified below in Table 2.1. It is also depicted graphically in Fig. 2.10, with the help of the transfer and output characteristics of the MOSFET in a PA.

Table 2.1: Classification of PAs in term of output current conduction angle Φ.

Operating Class	**Conduction current angle (CCA) Φ**	**Dependence on drive level**	**Bias position on V-I plot of MOSFET**
A	$\Phi = 2\pi$	No	Midway between cut-off and saturation regions
AB	$\pi < \Phi < 2\pi$	Yes	Above cut-off
B	$\Phi = \pi$	No	At cut-off
C	$\Phi < \pi$	Yes	Below cut-off

The conduction angle of a Class-A amplifier is 360° or 2π radians. The Class-B amplifier is another case where conduction angle remains equal to 180°, independent of the drive level. The output load is tuned by filtering/shorting all harmonics, generated due to reduced conduction angle, with the help of harmonic trap in output matching network. Such operation is efficient but the PA gain is lower. It is intolerable to lose this amount of gain, so, in practice, a Class-AB bias is employed, somewhere between A and B operation. This compensates the

gain loss associated with the pure Class-B operation while still reducing the device dissipation compared to the Class-A operation.

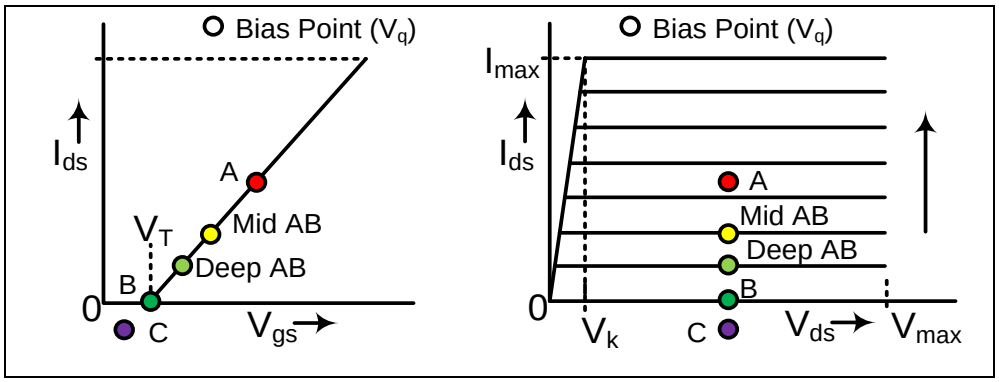


Fig. 2.10: Different classes of PA operation with transfer and output characteristics

A Class-AB amplifier is defined by a conduction angle that lies between 180° and 360°, so the transistor is switched off for a portion of a cycle when the input voltage swings sufficiently into cut-off.

The last one in these classical modes is Class C operation. It is a logical extension of the Class-B amplifier, in which the conduction angle is reduced below 180° so that the drain current is the peak of a sinusoid for a fraction of a cycle. As the conduction angle is decreased, the efficiency increases because the transistor is turned on for less time; however, the output power also decreases. Because the conduction angle is now a function of input drive, the fundamental component of the output current is no longer a linear function of input drive. One of the major problems in utilizing this mode is the large negative swing of the input voltage, resulting in reverse breakdown. For this reason, along with the rapidly decreasing output power and gain, true Class C operation is not preferred for solid state amplifiers at RF and microwave frequencies. Some renewed interest is currently apparent with enhanced negative gate drive of some newly introduced transistor (Freescale MRFE 6VP8600). Forthcoming sections present a brief analysis of the Class A and reduced conduction angle (AB and B) modes. This analysis will be useful for comparing other efficient modes of the PA.

2.5.1.1 Class A Mode Analysis

For the Class A mode analysis the ideal MOSFET characteristics are assumed. With reference to Fig. 2.4, for fully cycle conduction of I_{ds} in response to sinusoidal input voltage source, there is no harmonic at drain terminal. Hence, the input and output signals are

$$V_{gs}(\theta) = V_q + V_s\cos\theta \tag{2.30}$$

$$I_{ds}(\theta) = g_m(V_q + V_s\cos\theta) \tag{2.31}$$

Here, a linear trans-conductance g_m is assumed. With its value of unity, the resulting voltage (normalised with respect to $2V_{DD}$) and current (normalised with respect to I_{max}) waveforms with the dissipated power, are shown in Fig. 2.11. The last one is represented by the area of the curve. This is a linear operation and the drain current flows for the full cycle without any clipping. The maximum amplitude of the input signal at the gate corresponds to peak value of V_{DD} and I_{max}. For Class A mode, the voltage and current peaking factors are 2 and 1, respectively. Here, the threshold voltage V_T is assumed to be zero. For power MOSFETs, operating at 50 V, the typical value of V_T is between 2 to 5 V.

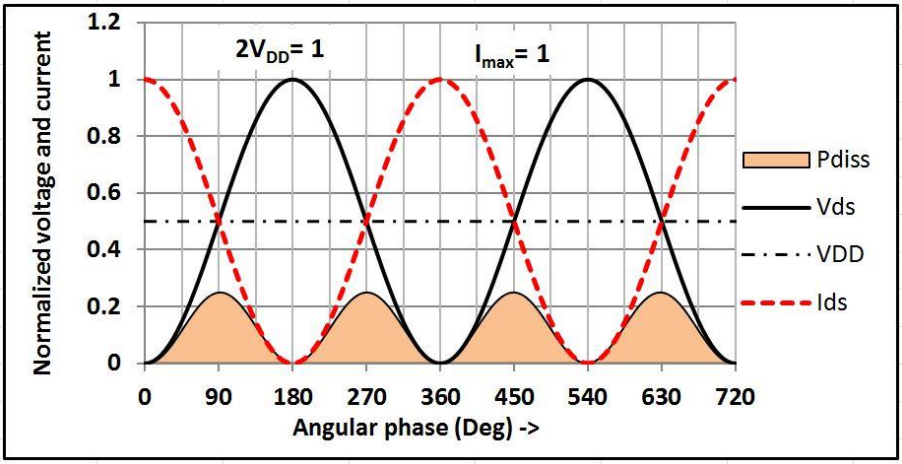


Fig. 2.11: Dissipated power, voltage and current waveforms for an ideal Class A PA

Using (2.20) the fundamental RF power in the Class A mode is given as

$$P_{1A} = \frac{V_{DC}}{\sqrt{2}} \cdot \frac{\left(\frac{I_{max}}{2}\right)}{\sqrt{2}} = \frac{V_{DD}I_{max}}{4} \tag{2.32}$$

It is denoted by additional subscript for Class A. For symmetrical excursion of I_{ds}, the DC current and the DC power, supplied to the PA circuit, is given by

$$I_{DC} = I_{max}/2 \tag{2.33}$$

$$P_{DCA} = V_{DD} I_{DC} = (V_{DD} I_{max}/2) \tag{2.34}$$

The optimum load for maximum rail to rail excursion is given as

$$R_{1A} = V_{DD}/(I_{max}/2) \tag{2.35}$$

Clearly for this ideal analysis, the DC to RF power conversion efficiency is 50%. In the PA design, the Class A is used most often for the small signal amplifier design. This is a generic case for comparing all other modes of operation. Due to its highly linear characteristics, it is used mostly as front-end amplifier.

2.5.1.2 Reduced Conduction Angle Mode Analysis

The Class A mode of the PA operation is simplest in nature. However, its theoretical efficiency rarely crosses 20-25% due to various practical issues like knee voltage of transistor, different parasitic reactance, definite power loss in impedance matching circuits and nonlinear trans-conductance of the transistor. For a low power PA, it may be acceptable, but for high power transistors it is not feasible to dissipate nearly three fourth of the power (for 25% efficiency) inside the transistor. In order to reduce this dissipation, reduced *current conduction angle* (CCA) modes were devised.

For the general case of CCA modes, the input voltage and the drain current waveform are shown in Fig. 2.12. The transistor is biased above cut-off (V_T). In order for the current to swing up to the idealized saturation point, I_{max}, the RF drive level has to be increased from the Class A mode. It is assumed that as the quiescent point is varied, the drive voltage is also manipulated, so that a peak current of I_{max} is maintained. The V_{ds} swing can be controlled by the selecting R_1 to reach the maximum value of $2V_{DD}$. The resulting I_{ds} is a truncated sine wave and the mean component (I_{DC}) of I_{ds} will decrease as the conduction angle is reduced.

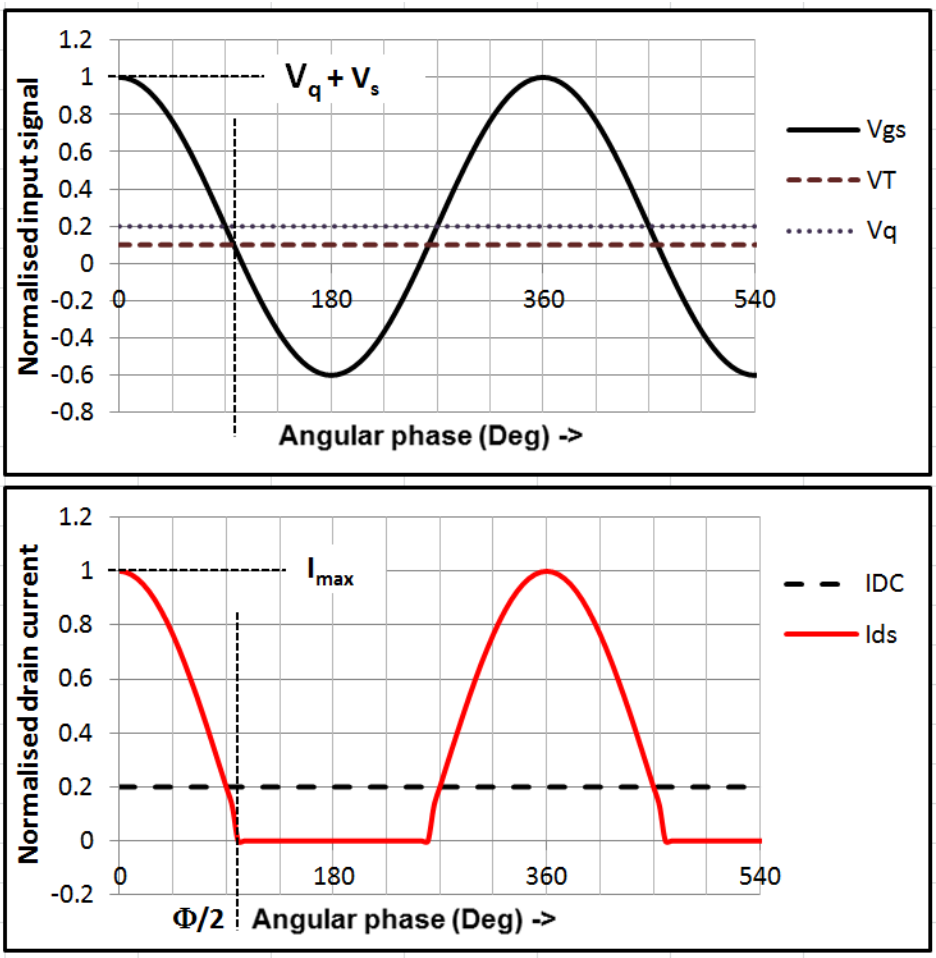


Fig. 2.12: Input voltage and clipped drain current for harmonic shorted PA operation

Thus, the transistor enters into a nonlinear operation regime and harmonics will be generated. In the output circuit, the fundamental load is tuned by shorting these harmonics with the help of a harmonic trap circuit. Due to this reason they are known as the harmonic shorted or tuned load modes. The truncated drain current can be written as

$$I_{ds}(\theta) = I_{DC} + (I_{max} - I_{DC})\cos\theta, \qquad -\frac{\Phi}{2} \leq \theta \leq \frac{\Phi}{2}; \tag{2.36}$$

$$= 0, \qquad -\pi < \theta < -\frac{\Phi}{2};\ \pi > \theta > \frac{\Phi}{2}$$

Thus $\cos\left(\frac{\Phi}{2}\right) = -\left(\frac{I_{DC}}{I_{max}-I_{DC}}\right)$ and drain current can be rewritten as

$$I_{ds}(\theta) = \frac{I_{max}}{1-\cos\frac{\Phi}{2}} \cdot \left(\cos\theta - \cos\frac{\Phi}{2}\right) \tag{2.37}$$

Using Fourier analysis, the mean value (I_{DC}) can be expressed as

$$I_{DC}(\Phi) = \frac{1}{2\pi}\int_{-\frac{\Phi}{2}}^{\frac{\Phi}{2}} \frac{I_{max}}{1-\cos\frac{\alpha}{2}} \cdot \left(\cos\theta - \cos\frac{\Phi}{2}\right) d\theta = \frac{I_{max}}{2\pi} \cdot \frac{\left(2\sin\frac{\Phi}{2} - \Phi\cdot\cos\frac{\Phi}{2}\right)}{1-\cos\frac{\Phi}{2}} \tag{2.38}$$

And amplitudes (I_n) of I_{ds} at n^{th} harmonic can be expressed as

$$I_n(\Phi) = \frac{1}{\pi}\int_{-\frac{\Phi}{2}}^{\frac{\Phi}{2}} \frac{I_{max}}{1-\cos\frac{\Phi}{2}} \cdot \left(\cos\theta - \cos\frac{\Phi}{2}\right) \cdot \cos n\theta \; d\theta \tag{2.39}$$

Fundamental component ($n = 1$) of the drain current is given as

$$I_1(\Phi) = \frac{I_{max}}{2\pi} \cdot \frac{(\Phi - \sin\Phi)}{1-\cos\frac{\Phi}{2}} \tag{2.40}$$

And for $n \geq 2$

$$I_n(\Phi) = \frac{2I_{max}}{\pi} \cdot \frac{\left(\sin n\frac{\Phi}{2}\right)\cdot\cos\left(\frac{\Phi}{2}\right) - n\cdot\left(\sin\frac{\Phi}{2}\right)\cdot\cos\left(n\frac{\Phi}{2}\right)}{n\cdot\ (n^2-1)\cdot\left(1-\cos\frac{\Phi}{2}\right)} \tag{2.41}$$

The power utilisation factor (PUF) is defined as the ratio of fundamental RF output power in operating mode under consideration to output power obtained in the Class A mode. Thus for the Class A it is unity. For optimum condition ($V_1 = V_{DD}$) the fundamental power, from (2.19) and (2.40) is given as

$$P_1(\Phi) = \frac{V_{DD}I_{max}}{4\pi} \cdot \left(\frac{\Phi - \sin\Phi}{1-\cos\frac{\Phi}{2}}\right) \tag{2.42}$$

Similarly using (2.21) and (2.38) DC power supplied to the PA is given by

$$P_{DC}\ (\Phi) = V_{DD}I_{DC} = \frac{V_{DD}I_{max}}{2\pi} \cdot \left(\frac{2\cdot\sin\frac{\Phi}{2} - \Phi\cdot\cos\frac{\Phi}{2}}{1-\cos\frac{\Phi}{2}}\right) \tag{2.43}$$

So the DC to RF power conversion or drain efficiency (η_{pa}), using (2.24) is

$$\eta_{pa,TL} = \frac{1}{2} \cdot \left(\frac{\Phi - \sin\Phi}{2\cdot\sin\frac{\Phi}{2} - \Phi\cdot\cos\frac{\Phi}{2}}\right) \tag{2.44}$$

Also the PUF can be derived from (2.42) and (2.32) as

$$\frac{P_1(\Phi)}{P_{1A}} = \frac{1}{\pi} \cdot \left(\frac{\Phi - \sin\Phi}{1-\cos\frac{\Phi}{2}}\right) \tag{2.45}$$

Using (2.22) the power dissipated in the transistor, $P_{diss}(\Phi)$, is given as

$$P_{diss}(\Phi) = \frac{P_{DCA}}{\pi} \cdot \frac{\sin\frac{\Phi}{2}\left[2+\cos\frac{\Phi}{2}\right] - \frac{\Phi}{2}\left[1+2\cos\frac{\Phi}{2}\right]}{\left(1-\cos\frac{\Phi}{2}\right)} \tag{2.46}$$

The Normalized current components (up to $n = 2$), efficiency and power utilization factor (PUF) are shown in Fig. 2.13. The DC component decreases monotonically as CCA is reduced. For Φ lower than π, corresponding to the Class C operation, the DC component continues to drop, but the fundamental component of current also starts to drop below its Class A level. This results in higher efficiency but a lower PUF.

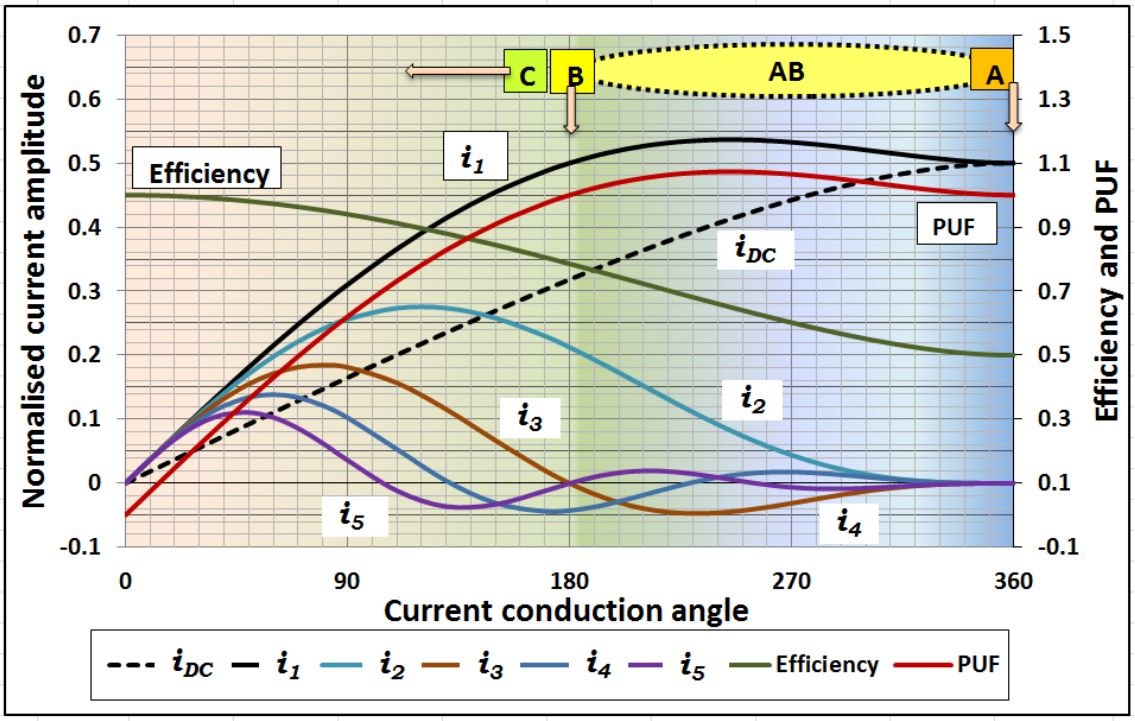


Fig. 2.13: Normalized current components for harmonic shorted modes

Throughout the Class B, the largest harmonic, is the second one. It is in-phase, with the fundamental, and the action of the partially cut-off transistor is to generate a substantial amount of second harmonic, which reduces the dips of the fundamental sine wave and sharpens the peaks, resulting in a lower mean level. The maxima of fundamental current component results in the Class AB mode. The odd harmonics can be seen to pass through zero at the Class B point, but in AB mode, the third harmonic is certainly not negligible.

2.5.1.2.1 Analysis for Back-Off Operation

Different parameters for the harmonic shorted modes, for the full as well as the reduced or backed–off input drive power (by 3 dB), were calculated using above mentioned analysis. These are summarized in Table 2.2. For the Class AB mode, the *deep* bias condition is assumed, corresponding to $V_q = 0.25$ and Φ=218.9°. It is assumed that by filtering harmonics and by tuning load value, peak value of drain voltage at load is always maintained equal to $2V_{DD}$. The value of each parameter is normalised with respect to its respective peak value. For example the total input signal (sum of V_s and V_q) is assumed to be unity, corresponding to I_{max} (also equal to unity). Similarly peak value of $V_{ds}(= 2V_{DD})$ is also equal to unity. So amplitude of the input RF signal can be written as

$$V_s = 1 - V_q \tag{2.47}$$

Table 2.2: Calculated normalised parameters for reduced CCA mode

Major Parameter	**Normalised values- Class A**		**Normalised values- Class AB**		**Normalised values- Class B**	
	Full swing	**3-dB back-off**	**Full Swing**	**3-dB back-off**	**Full Swing**	**3-dB back-off**
CCA (Φ)	360°	360°	218.9°	236.2°	180°	180°
V_q	0.50	0.50	0.25	0.25	0	0
V_s	0.5	0.35	0.75	0.5	1	0.707
I_{DC}	0.50	0.50	0.38	0.31	0.32	0.23
I_1	0.50	0.35	0.53	0.42	0.50	0.35
V_{DD}	0.50	0.50	0.50	0.50	0.50	0.50
R_1	1	1	0.94	0.94	1	1
V_1	0.50	0.35	0.50	0.39	0.50	0.35
P_1	0.125*	0.06	0.13	0.08	0.125	0.06
PUF (dB)	0	-3.0	0.26	-1.82	0	-3.01
P_{DC}	0.25	0.25	0.19	0.16	0.16	0.11
$\eta_{pa,TL}$ (%)	50	25.0	70.3	52.5	78.5	55.5

* This value is equal to P_{1A}.

For AB mode, the value of R_1 is reduced from the one for the Class A, reflecting the higher fundamental current component. The RF output (P_1) shows a small increase from the Class A condition and is accompanied by a significant reduction in I_{DC}. This causes a useful increase in efficiency (70.3%). Such beneficial effects come at the expense of about 3 dB extra input drive power, which can be considered as a reduction in overall power gain from the Class A mode. Thus the PAE is lower in AB mode. The conduction angle changes in Class AB mode in 3-dB back-off condition.

In the Class B mode, the RF power (P_1) has returned to the Class A value, corresponding to a PUF of 0 dB. I_{DC} is reduced by a factor of 2/π compared to the Class A, resulting in an efficiency of about 78.5%. The downside is that 6 dB more drive power is needed to achieve this condition. It can be seen that the Class B shows a proportional decrease in the output power while in AB mode P_1 does not decrease in proportion to V_s. In the Class AB, the CCA is function of the input drive while in B mode it is independent of the input signal variation. The Class-B is a preferred choice in view of the push-pull topology required for the PA design at high power. For avoiding cross-over distortion, the Class AB can also be selected.

2.5.2 Switching Modes

Another Class of operation for efficient PA is switching mode for harmonic tuned power amplifier. Several such approaches [6] have been proposed in literature, all characterised by the basic assumption that the RF transistor operates as an ON/OFF ideal switch. It is heavily saturated by a large input signal, while it is biased near cut-off. The voltage- and current-clipping, caused by this operation, make it possible to operate it as a switch. The output current and voltage waveforms are properly shaped in the nonlinear domain by the load network to prevent an overlap between them, thus minimizing the power dissipation and ensuring the highest efficiency level. The timing of switch opening and closure is controlled by varying the drive level and the bias point at the transistor input. Fig. 2.14 shows a simple

switching amplifier with waveforms for a conduction angle of 2Φ. The maximum current in the switch is controlled entirely by the supply voltage V_{DD} and the RF load resistor, and the voltage toggles between zero and V_{pk}. This circuit converts DC energy to RF energy; at no point in the RF cycle is there a nonzero voltage and current simultaneously, so no energy is wasted as heat in the switch. It is assumed that the DC supply voltage remains constant with the help of electrolytic filter capacitors, as the conduction angle Φ is varied.

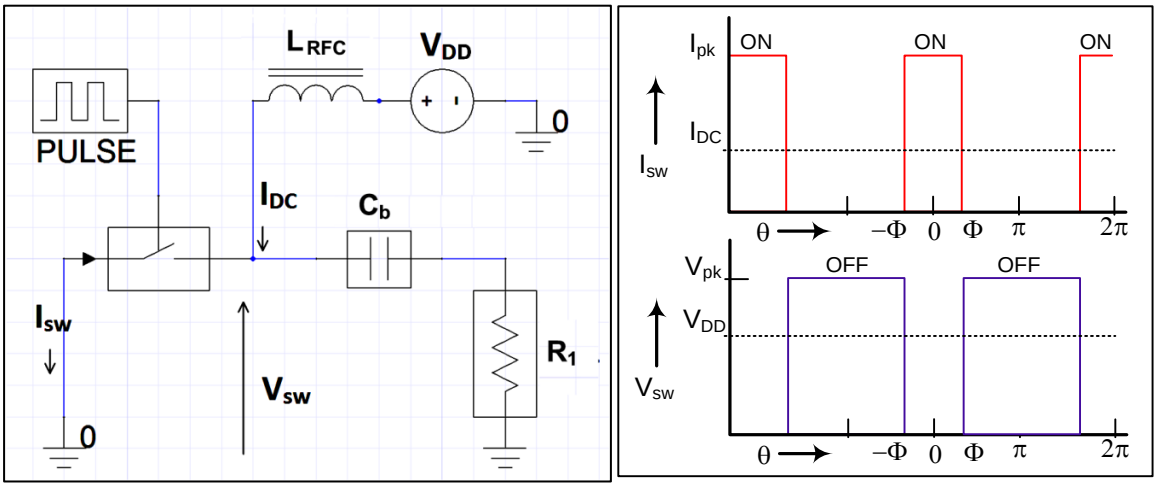


Fig. 2.14: Basic switching mode PA scheme with current and voltage waveforms

With the Fourier analysis of such waveform, the conversion efficiency is derived as

$$\eta_{pa,SW} = \frac{2 \cdot \sin^2 \Phi}{\Phi(\pi - \Phi)} \tag{2.48}$$

So, in the symmetrical square wave case ($\Phi = \pi/2$), the efficiency is about 81%, despite having a device which dissipates no heat. This is because the RF power is being wasted in harmonic frequency components. This harmonic energy is undesirable, and can be removed by placing a harmonic-short/tank-circuit across the load. For such case, by choosing an optimum load resistor it can be ensured that $V_1 = V_{DD}$. Corresponding efficiency is

$$\eta_{pa,SW} = \frac{\sin \Phi}{\Phi} \tag{2.49}$$

From the analysis [73], it can be calculated that the peak in RF power occurs at a conduction angle of π/2. Still the efficiency at this point is a rather modest 63% (2/π). Thus, an

ideal switch does not, by itself, give any instantaneous improvements in the efficiency of more conventional high efficiency circuits, and alternative configurations have to be sought in order to make best use of a switching device. Two such configurations, the Class D and Class E modes are very popular. The Class-D PA is operated in a push-pull configuration. It can be thought of as a modified large-signal Class-B amplifiers, where energy that would be otherwise dissipated in the transistor is stored in the switch capacitor and released into the output circuit. Such amplifier at high power has been reported recently [150] and offer some attractive possibilities without generating excessive voltage swing.

2.5.2.1 Class E Mode Power Amplifier

The Class-E power amplifiers, introduced by the father and son team of Nathan and Alan Sokal in 1975 [151], makes use of harmonic tuning at the output circuit to recycle energy stored in the parasitic output capacitance of the transistor switch (Fig. 2.15). This energy is normally dissipated in the switch resistance if the switch turns on while there is a voltage across the capacitor. However, if the transistor switch voltage goes to zero before the switch turns on, the stored energy is zero and therefore power is not dissipated in the transistor.

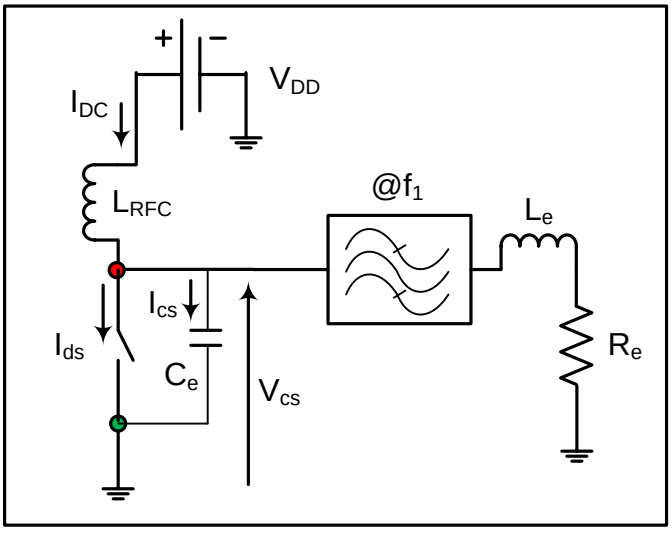


Fig. 2.15: Class E PA scheme with ideal switch

Here an ideal switch is shunted by its output capacitor C_e. It is the combination of the device output capacitance and an external capacitor to fulfil design relationship for the low frequency range. The RF matching network consists of a series resonant circuit tuned at the fundamental frequency, with $L_e - R_e$ combination. The latter one has to be selected to terminate the transistor output so as to produce the desired phase shift [152] between the switch voltage and current. Unlike Classes B and C in which the load network only provides power-matched impedance to the load, in the Class-E it is also used to adjust the phase difference between the switch current and voltage such that no high voltage and high current occur simultaneously across the switch. Its optimum condition, for 50% duty cycle, is uniquely determined by the appropriate load network and the shunt capacitor. If the voltage signal vanishes earlier than the optimum time, it is called suboptimal operation. In order to make the Class E operation, the capacitor voltage $V_{cs}(\theta)$ must return to zero just before the switch turns on and starts conducting current. Thus, shunt capacitor is never discharged through the switch. Similarly the current through the switch must return to zero just before the switch turns off. Another condition for the Class E operation is that at turn-on the voltage across the switch must return to zero with zero slope. In terms of $V_{cs}(\theta)$, these conditions are

$$V_{cs}(\theta = \pi) = 0 \qquad \left.\frac{dV_{cs}(\theta)}{d\theta}\right|_{\theta=\pi} = 0 \tag{2.50}$$

The simulated voltage and current waveforms for 50% duty cycle of a simple low power Class E PA, are shown in Fig. 2.16 and Fig. 2.17. The current $I_{cs}(\theta)$ is charging/discharging the capacitor C_e. For this optimum case, DC power and fundamental RF power are equal, and given as

$$P_{DC,E} = P_{1E} = \frac{V_{DD}^2}{R}\frac{8}{(\pi^2 + 4)} \tag{2.51}$$

Thus, DC to RF conversion efficiency is ideally equal to 100%. The device stress in terms of the peak factors for drain voltage and current are very high for the Class E operation.

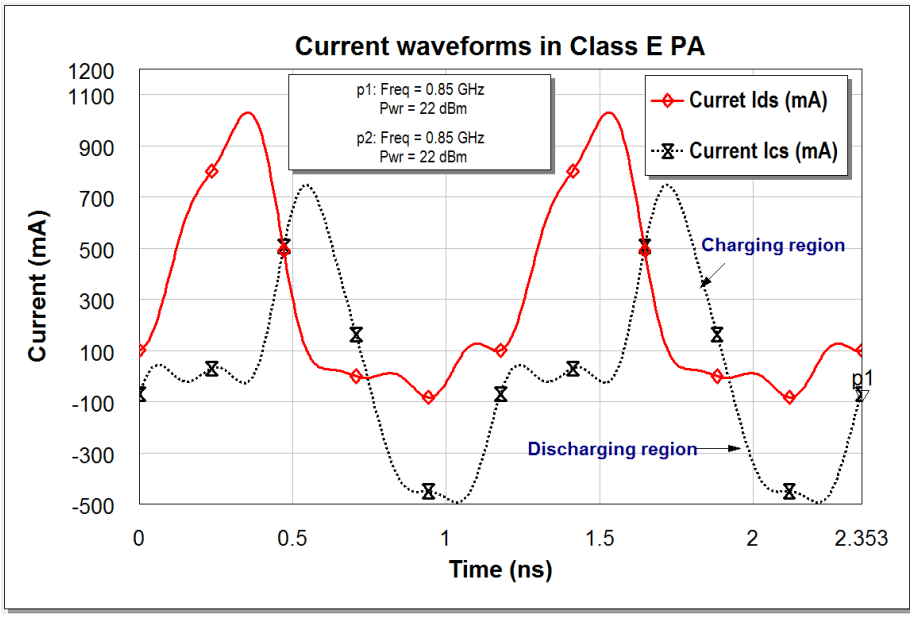


Fig. 2.16: Transistor and capacitor current waveforms in Class E PA

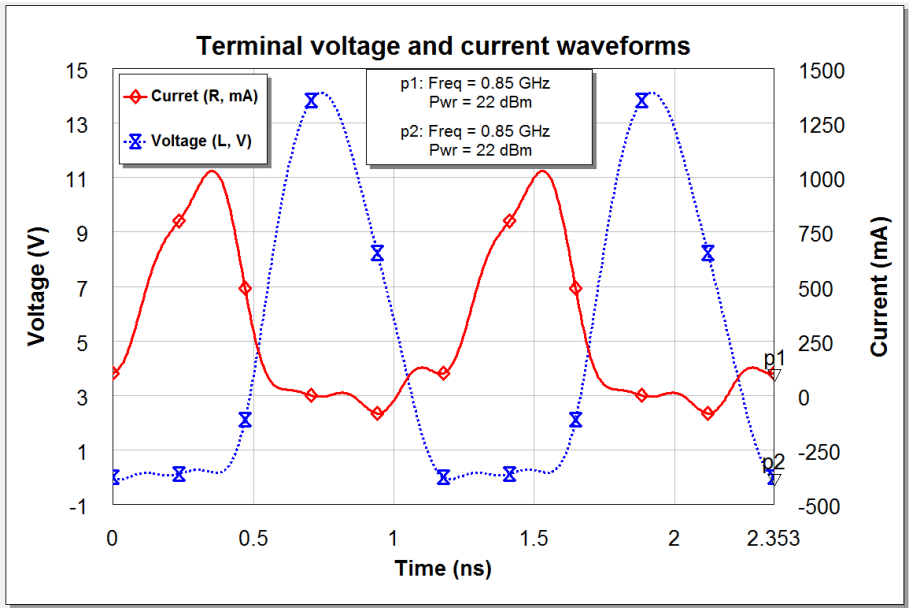


Fig. 2.17: Terminal voltage and current waveforms in Class E PA

The Class-E PA can deliver the highest efficiency among the switching topologies because this amplifier tunes harmonic impedances through the series resonator, making the ideal crossover from the conduction state to the off-state of the transistor without having discharging loss. However, the ideal switching operation is not possible even at a low frequency, because it requires an abrupt charge build-up at the switching off transition. In fact the maximum frequency of the Class-E operation is expressed [153] by the expression

$$f_{max,E} = \frac{I_{DC}}{2\pi^2 V_{DD} C_{out}} \tag{2.52}$$

At a high frequency, above the maximum operation frequency of the ideal Class-E, the discharging process of capacitor is not sufficiently fast and residual charge at the switch-on transition is discharged through the bifurcated current at the saturated operation, thus degrading the overall efficiency significantly. Apart from this, the switch has a finite on-resistance, and the transition times from the off-state to the on-state and vice- versa are not negligible. It results in power dissipation in the switch. To achieve the high efficiency of the Class-E PA, beyond $f_{max,E}$, an optimization of the voltage waveform with the assumption of the conventional Class-E current waveform and linear [154] as well as nonlinear [153] output capacitor is necessary. In practice, the switching device also has stray reactance, saturation resistance, and nonzero switching time, factors which contribute to reduced efficiency.

2.5.3 Practical Issues in the Design of a Power Amplifier

The idealized analysis, presented up to this time, serves as a comparison among different modes of operation. In practice, various issues, as discussed below, often reduce performance and efficiency compared to ideal cases.

2.5.3.1 Effect of Realistic V Characteristic of RF Transistor

The use of a realistic MOSFET IV characteristic (Fig. 2.18), including the knee turn-on region, has a substantial impact on the power and efficiency of a large signal PA. As I_{ds} increases with V_{gs}, device saturation happens at higher and higher drain voltage. This phenomenon gives rise to the knee voltage V_k. It results in a bifurcated I_{ds} when V_{ds} is low. This, in turn, generates lots of unwanted harmonics, resulting in the efficiency degradation and spurious frequencies generation. In transistor amplifiers, V_k will always be a significant percentage of the DC bias supply and in portable battery-powered PAs, its effect can dominate the whole design strategy.

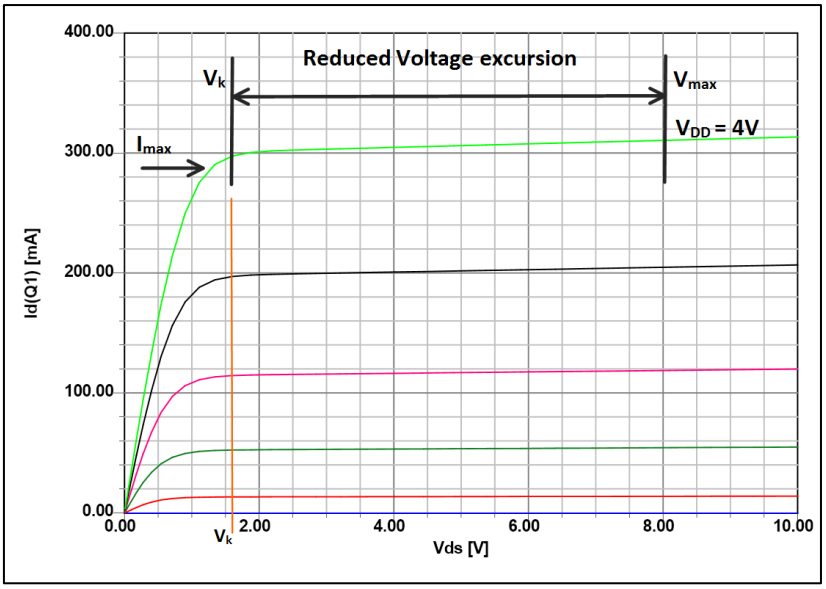


Fig. 2.18: Realistic transistor's output IV characteristics

Due to a small but nonzero knee voltage V_k of the transistor, either voltage excursion needs to be reduced or the V_{DD} needs to be increased. In either case the minima of the voltage waveform is pulled out of the turn-on region. Hence, the fundamental component (V_1) of the voltage waveform reduces from V_{DD} to

$$V_{1,TL} = V_{DD} - V_k \tag{2.53}$$

$V_{1,TL}$ gives actual possible fundamental voltage component in tuned load operation. For accounting the effect of V_k, a degradation factor χ is defined as

$$\chi = \frac{(V_{DD} - V_k)}{V_{DD}} = \frac{V_{1,TL}}{V_{DD}} \tag{2.54}$$

The DC to RF drain conversion efficiency is reduced [155] by this factor as

$$\eta_{pa,k} = \chi \cdot \eta_{pa,TL} \tag{2.55}$$

If V_k is about 10% of V_{DD}, the impact on the efficiency will be a factor of 0.9, or a reduction from 75% to 67.5% for the Class B PA.

Contrary to this, some features in actual IV characteristics have positive influence on efficiency. In the reduced CCA analysis, linear transfer characteristics of MOSFET were assumed. For the Class A condition, the normalised quiescent gate voltage is $V_q = 0.5$.

Hence, assuming such linear characteristics, the drain current (with $g_m = 1$) in the Class A operation is given as

$$I_{ds} = V_{gs} = (0.5 + V_s \cos\theta) \tag{2.56}$$

In practice, this characteristic is soft curved instead of showing an abrupt turn on and saturation. It can be well approximated with a square law device characteristic. For such device, the output current (with $g_m = 1$), is given by

$$\begin{aligned} I_{ds} = V_{gs}^2 &= (V_q + V_s \cos\theta)^2 \\ &= \left(0.25 + 0.5{V_s}^2\right) + V_s \cos\theta + (0.5{V_s}^2 \cos 2\theta) \end{aligned} \tag{2.57}$$

Assuming that the output matching network presents a short circuit at all harmonics, the fundamental output voltage amplitude is a linear function of the input level V_s, despite the square-law device characteristics. The square-law characteristic yields the same fundamental output amplitude, but a dc component reduced by a factor of $\left(0.25 + 0.5{V_s}^2\right)/0.5$. Thus when signal is maximum ($V_s = 0.5$) it corresponds to an increase in efficiency from 50% to 66.7%. This improvement in the efficiency is obtained simultaneously with perfectly linear amplification. It is therefore apparent that to create a device with optimum efficiency and the linearity, it is necessary to tailor its transfer characteristic.

2.5.3.2 Harmonic Trap at the Output

Another departure from the theory is that in the RF circuits, the harmonic trap at the load is rarely explicit. Its function is to short-circuit all harmonics other than the fundamental, at the load. In practice, this corresponds to that the harmonic spectral output powers are below some limit. The output capacitance (C_{out}) of the device and other parasitic also help achieving this. However, for a finite C_{out} the second harmonic voltage component is non-zero, and will be not be in phase with the fundamental. It may result in the second harmonic peaking, and with sufficient drive can cause the voltage to swing even below zero or negative. This reduces the output power and efficiency compared with the ideal (tank circuit) case.

For small output capacitance the remedy it is to use additional output capacitance to supplement that of the device, without perturbing the fundamental match to the load. Unfortunately, this addition at the output may reduce the real part of the output resistance that needs to be matched, and reduce the available bandwidth. Also the harmonic trap, in a practical circuit, can be provided only for first few harmonics.

2.5.3.3 Effect of Nonlinear Output Capacitor

As discussed above, the output capacitor C_{out}, has an important role in the harmonic trapping and voltage waveform shaping. The latter one, discussed in the next chapter, becomes more important as this capacitor exhibit a nonlinear nature, resulting in harmonic generation. For low power transistor (like CGH40006P from Cree) and power transistor (300W BLF 573 from NXP) its behaviour is shown in Fig. 2.19 and Fig. 2.20, respectively.

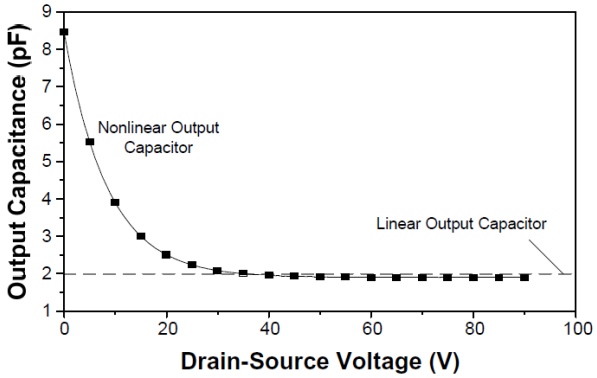


Fig. 2.19: Nonlinear behaviour of output capacitor in a 6 W transistor

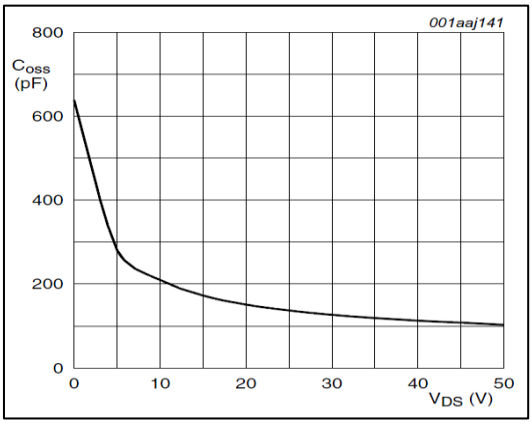


Fig. 2.20: Nonlinear output capacitor for BLF 573 MOSFET

In a high frequency model, C_{out} is the scaled sum of the drain-source capacitor and the capacitor across gate and drain. The voltage across the capacitor C_{out} is proportional to the integral of the current through it, which is the charge in this capacitor, scaled by the capacitance. This nonlinear variation of C_{out} is represented by [114]

$$C_{out} = C_{zero} + c_1 \cdot [1 + \tanh(c_2 \cdot V_{ds} + c_3)] \quad (pF) \tag{2.58}$$

The values of constants c_1, c_2, c_3 and C_{zero} are obtained by the curve fitting techniques for matching resulting nature with one given in manufacturer's data sheet. Resulting waveform's nature is more evident with the help of circuit simulation of linear as well as nonlinear capacitors. Fig. 2.21 shows the values of above constants with the circuit used for simulation using APLAC simulator of Microwave office™ [156].

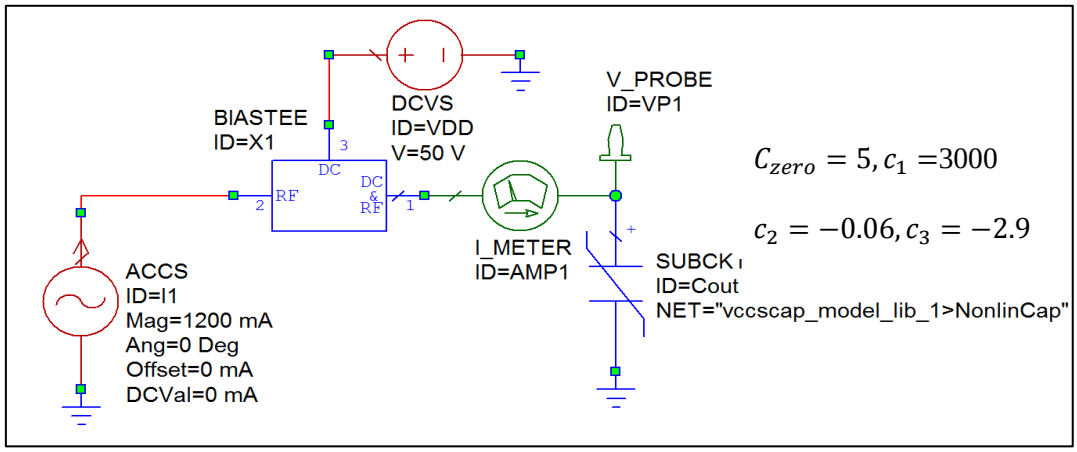


Fig. 2.21: Simulation circuit for calculating effect of the nonlinear capacitor

A bias voltage of 50 V and a frequency of 1 GHz was selected for this simulation. NonlinCap1 in this circuit represents the nonlinear capacitor C_{out}, modulated according to the drain-source voltage. As seen in Fig. 2.22, the nonlinear capacitor generates the harmonic voltage components in response to a fundamental current excitation (ACCS). For comparison, the voltage across the linear capacitor is also shown by a constant value of C_{zero}. This harmonic voltages consist of a large second harmonic component with the smaller higher

order harmonics (the flat bottom and sharp peaking in Fig. 2.22), even though only the fundamental current is injected into the capacitor.

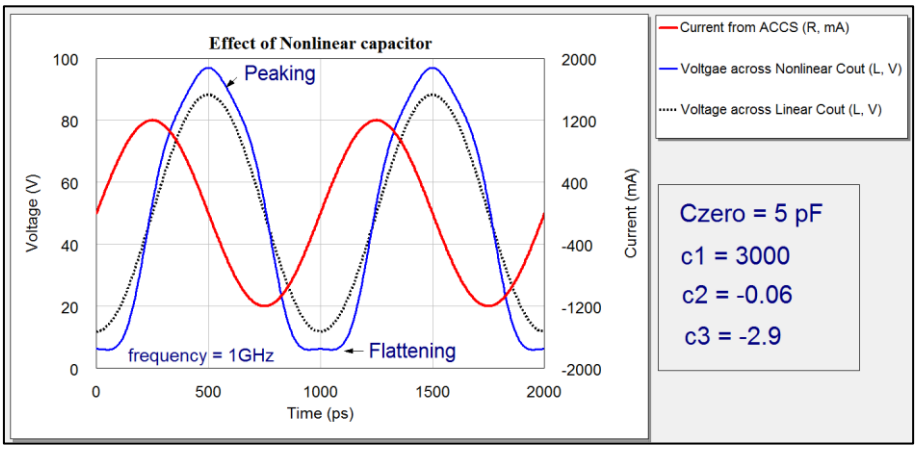


Fig. 2.22: currents and voltages for linear and nonlinear capacitors

The resulting second harmonic impedance is negative, because the second harmonic component in the voltage waveform is generated not by the second harmonic current and load but by the nonlinear C_{out}. This impedance has a large magnitude in comparison to the linear capacitor waveform due to a significant reduction in the second harmonic current and an increase in the second harmonic voltage. This increase in second harmonic voltage causes an enhancement in the overall magnitude of V_{ds}. In fact, the nonlinear C_{out} reduces the phase difference (φ_n) between the fundamental voltage and current and thus helps improving output power while reducing the reactive power. The wave shaping is not much affected by the harmonic generation of nonlinear input capacitor C_{IN}, while considering the nonlinear C_{out}. Thus, the nonlinear C_{out} supports for a favourable wave shaping, which has important implications for the design of harmonic tuned PAs.

2.6 Experimental Investigation of Harmonic Shorted Power Amplifiers

Based on the above discussion, design and experimental investigation of the solid state power amplifiers, operating in harmonic shorted modes, was carried out. The centre frequency for the designed amplifiers was kept in the UHF band (at 352 MHz and 505.8 MHz). They

were selected so as to fulfil the on-going project requirement of the department and to get real time performance by operating the designed PAs as a part of RRCAT particle accelerators. The techniques are described for two low power (10 W) amplifiers (LPA) and two high power (270 and 400 W) amplifiers (HPA). The two LPAs operate in the Class A mode while two HPA operate in the Class B and AB mode, respectively.

2.6.1.1 Low Power Amplifier

An LPA is needed for two purposes. The first purpose is to boost RF signal of commercial signal generator, which is not sufficient for feeding high power module. Hence, it acts as a driver amplifier to the HPA. The second purpose is that various theoretical and experimental investigations, for low power device, pave the way towards high power design. In view of desired good signal fidelity, limited requirement of LPA and low power consumption compared to HPA, the Class A mode was selected for the operation of these LPAs. Using a load line approach and complex conjugate matching, two amplifiers, each one with 10W output power were fabricated; one at 352 MHz and another at 505.8 MHz. For both of these frequencies, LDMOS MRF9030 was selected for the design. As per data sheet, it is designed for the broadband wireless system up to 1 GHz. Its power (30W), gain (15 dB), SOE package and bias supply (28 V) make it a suitable candidate for the present design. These rating are well matched with desired specifications including minimum output power of 10 W, minimum gain of 14 dB at the bias supply of 28 V. Here, the design detail is described for 352 MHz PA. The design procedure for the 505.8 MHz LPA is almost similar. For 352 MHz LPA, the impedance matching design [146] was started with the determination of the optimum load line (R_1), for the output matching circuit design [157]. Taking the effect of V_k into account and using (2.19) with $\cos(\varphi_n) = 1$ we can calculate $Z_1 = R_1$ $(n = 1)$. With a fundamental output power P_1 of 10 W, supply voltage of 28 V and V_k of 9.4 V, the value of R_1 comes equal to 17.3 Ω. This value of R_1 is at intrinsic drain current source without device

package parasitic components. For taking their effect into account, load pull simulation needs to be performed with appropriate circuit model of this LDMOS device. There is no non-linear circuit model readily available for this transistor. Hence MET model, which is available in the circuit library of the circuit simulator Microwave office™, was selected for circuit simulation. In order to match MET model with MRF 9030 device, its transfer characteristics (Fig. 2.23) were generated with the help of slug tuners.

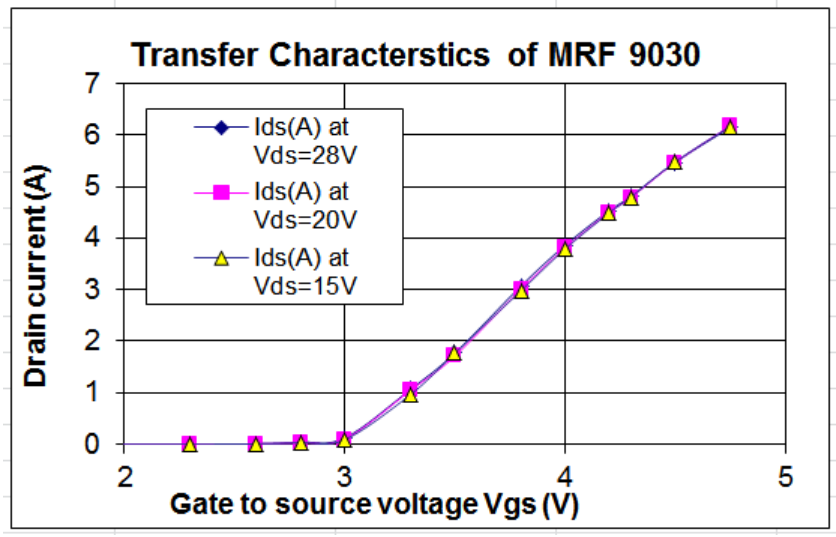


Fig. 2.23: Measured transfer characteristics of MRF 9030 transistor

This characteristics shows the measured I_{ds} as a function of V_{gs}, at three different (drain-source) voltages. From transistor's data sheet and this characteristic, different parameters of the MET model were manipulated to use it in the circuit simulator. Using this model, the simulated IV characteristics with calculated dynamic load line is shown in Fig. 2.24. For the Class A mode with V_{DD} of 28 V, an upper limit of drain-source voltage excursion, is 46.95 V. The simulation circuit used for the dynamic load line calculation and the load pull analysis is shown in Fig. 2.25. The calculated value of R_1 is used to set the fundamental reflection coefficient in the harmonic balance (HB) tuner during simulation. The input side of the MRF 9030 is treated as an ideal voltage controlled current source. Being a Class A mode operation, the harmonic trap is not required.

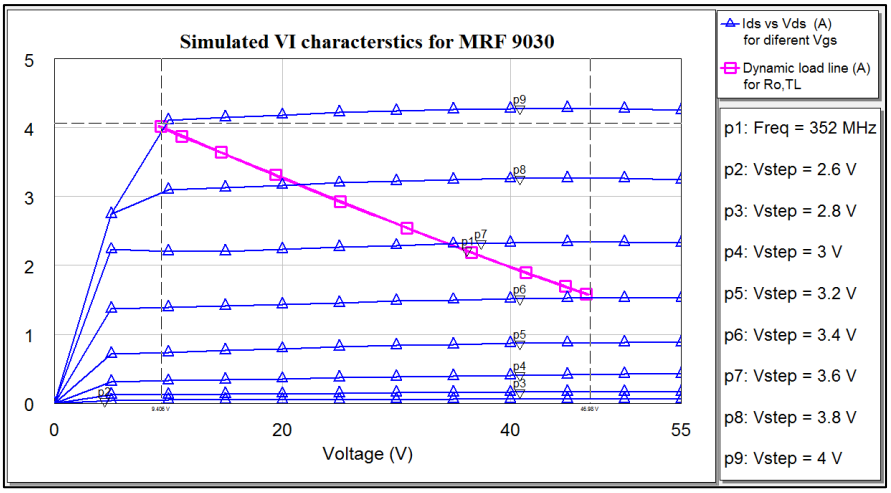


Fig. 2.24: The simulated IV characteristics for MRF 9030 transistor at 352 MHz

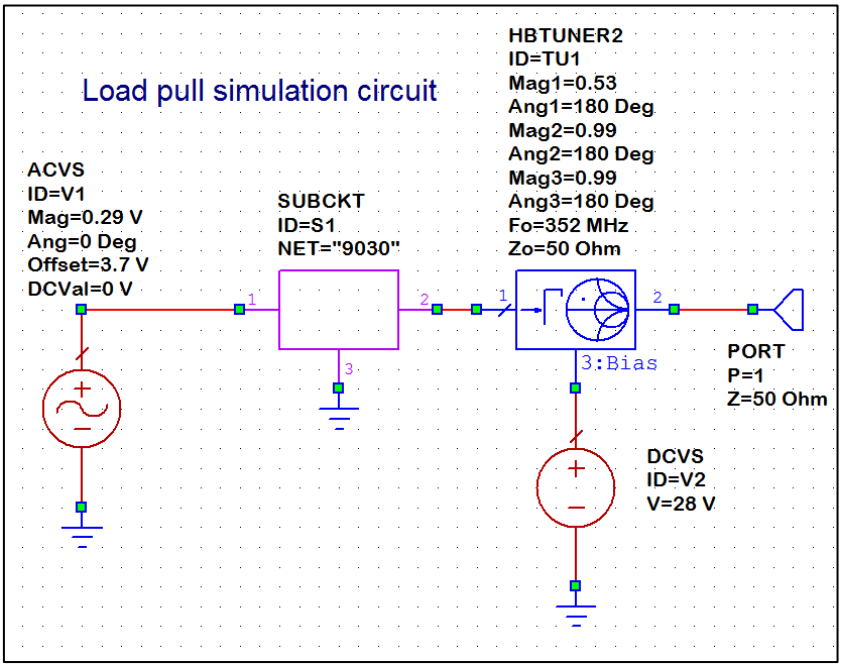


Fig. 2.25: The load-pull simulation circuit for LPA at 352MHz

The corresponding load pull contours drawn on the output impedance plane, for different output powers, are given in Fig. 2.26. From this load pull analysis, the value of output impedance, corresponding to an optimum output power of 40.027 dBm, was obtained as 20.35+j 3.2 Ω.

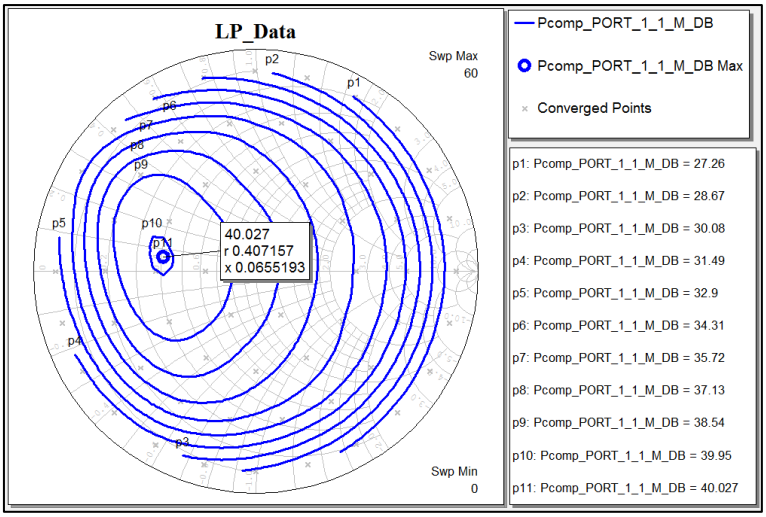


Fig. 2.26: The load-pull simulation results for LPA at 352MHz

In order to match terminal impedances at the gate and drain sides of the transistor to the system impedance of 50 Ω, the coaxial transmission line transformers were selected as the impedance matching unit, along with the L section of lumped capacitors and microstrip line (Fig. 2.27 and Fig. 2.28). At the input side, a combination of two 4:1 transformers was selected. This gives opportunity to tune wide range of impedance for input side. On output side, one 9:1 transformer was employed. On output side effort was made to keep minimum number of components, in order to minimize resistive losses in lumped and distributed RF components. An air core RF choke was connected at the wave-port, is shown in Fig. 2.28.

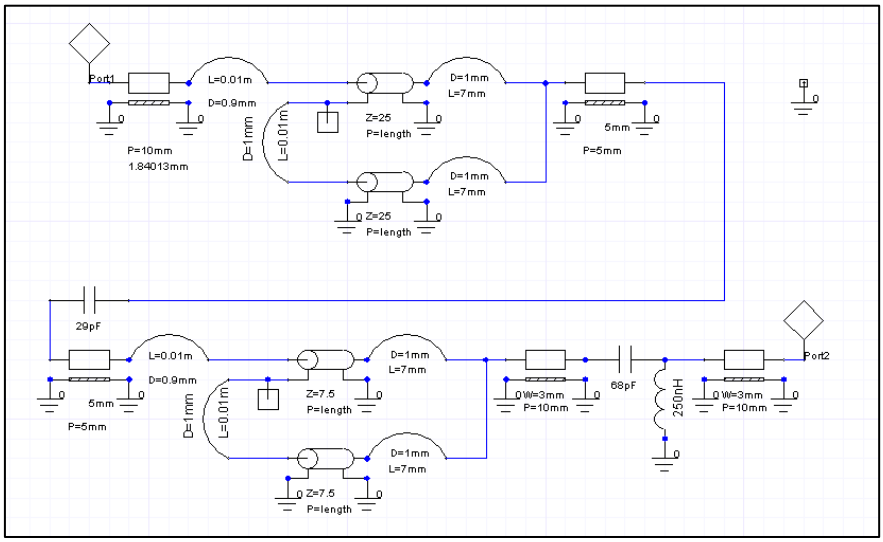


Fig. 2.27: Input impedance matching network for LPA at 352 MHz

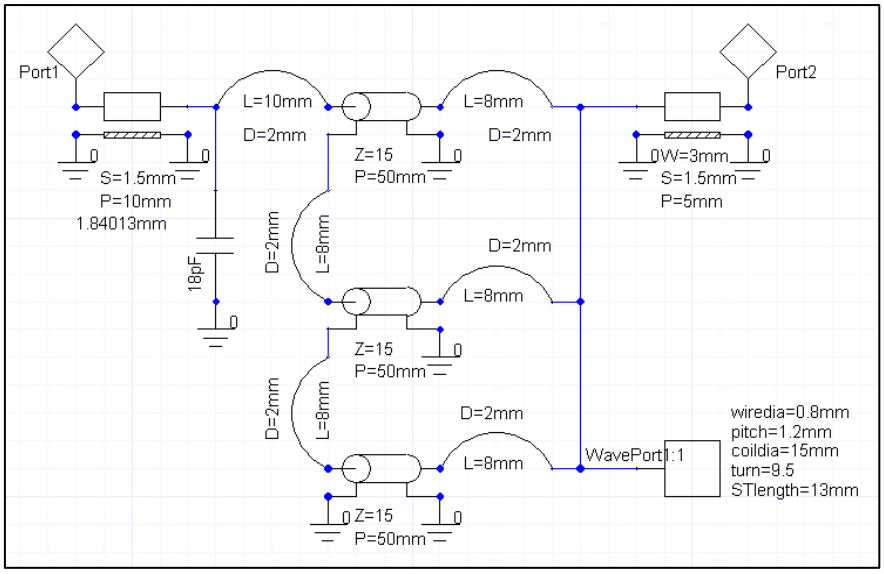


Fig. 2.28: Output impedance matching network for LPA at 352 MHz.

After circuit optimization, a circuit layout was generated and printed on a double sided Cu cladded RF board (Arlon AR32) with a relative permittivity of 3.2 and a thickness of 0.786 mm. At 352 MHz, this layout is 60 mm in length and 175mm in the width. Similar exercise was carried out for designing the LPA, operating at 505.8 MHz, using the same transistor. Fig. 2.29 shows final layouts, for the designed LPAs. The transmission line transformers were properly bended before their assembly.

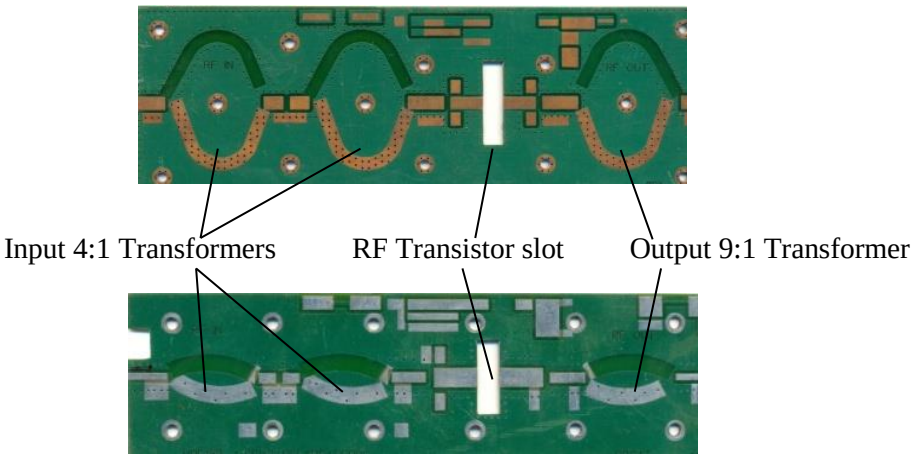


Fig. 2.29: Fabricated circuit layout for LPAs at 352 MHz (left) and at 505.8MHz

The RF characterisation and measurement for each LPA revealed a minimum gain of 15 dB and P_{1dB} point at an output power of nearly 10 W (Fig. 2.30 and Fig. 2.31), at the respective centre frequency. Due to the Class A operation, the DC to RF efficiency is moderate (27-

29%) for both of these LPAs. The power gain and efficiency is little higher for the 352 MHz LPA. This is expected due to roll-off of the transistor characteristics with increasing frequency. The second harmonic and spurious components were lower than -35 dBc, compared to the fundamental component, for both these LPAs. Regarding the circuit stability, no problem was observed as ferrite isolators were connected at the output of these LPAs. The 1-dB bandwidth, measured for each LPA, was nearly 10% around the centre frequency.

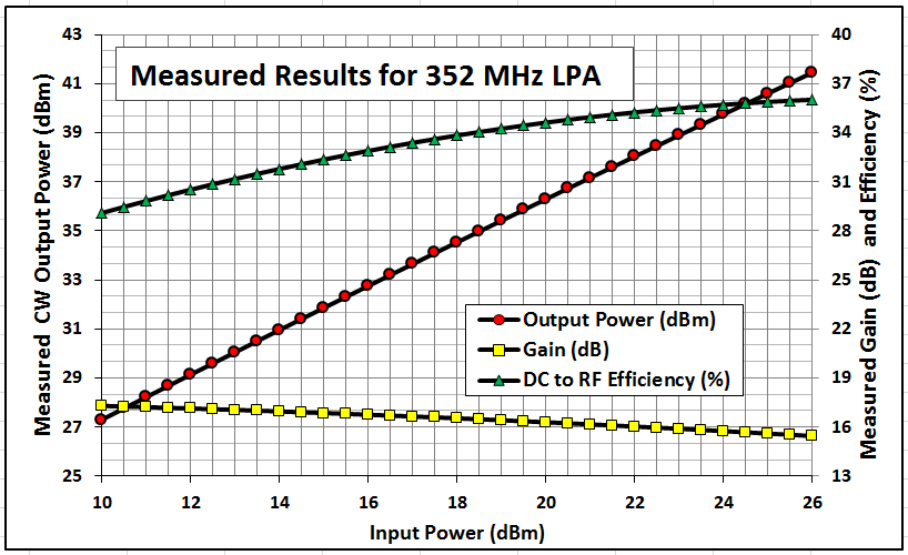


Fig. 2.30: Measured swept power transfer characteristics for 352 MHz LPA

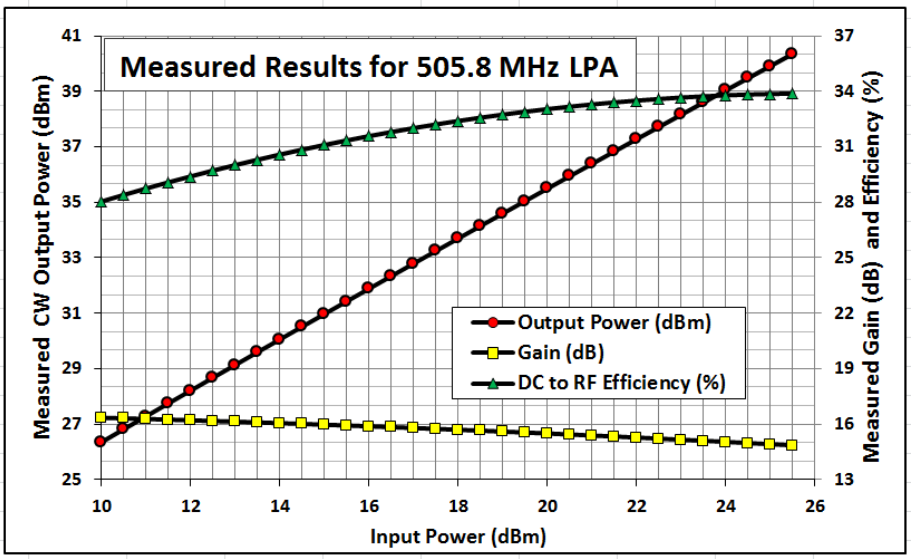


Fig. 2.31: Measured swept power characteristics for 505.8 MHz LPA

2.6.1.2 High Power (270 W) Amplifier at 352 MHz

Following the successful implementation of LPA, another design of a 270 W HPA was carried out using LDMOS transistor LR301, operating at a bias voltage of 28 V DC. This is a push-pull transistor with 300 W of output power at 350 MHz. Its knee voltage, as per IV characteristics given in its data sheet is nearly 4.5V. For designing HPA, the Class B mode was selected due to the push-pull operation required for this transistor. This HPA was intended for using as a gain module in a 2 kW (CW) SSPA system with 8-way combining scheme. Hence, its minimum output power should be 250 W. With some margin for the power loss in interconnecting RF cables, technical specifications for this HPA were takes as 270 W (CW) of output power with 12 dB power gain and conversion efficiency nearly 66%. For this transistor, a Spice level-1 circuit model (Fig. 2.32) along with the package parasitics including bond wire, lead inductance, resistance and capacitances is available from the data sheet. The source and load impedances at 350 MHz are 1.6-j0.4 Ω and 2.4+j1.0 Ω, respectively.

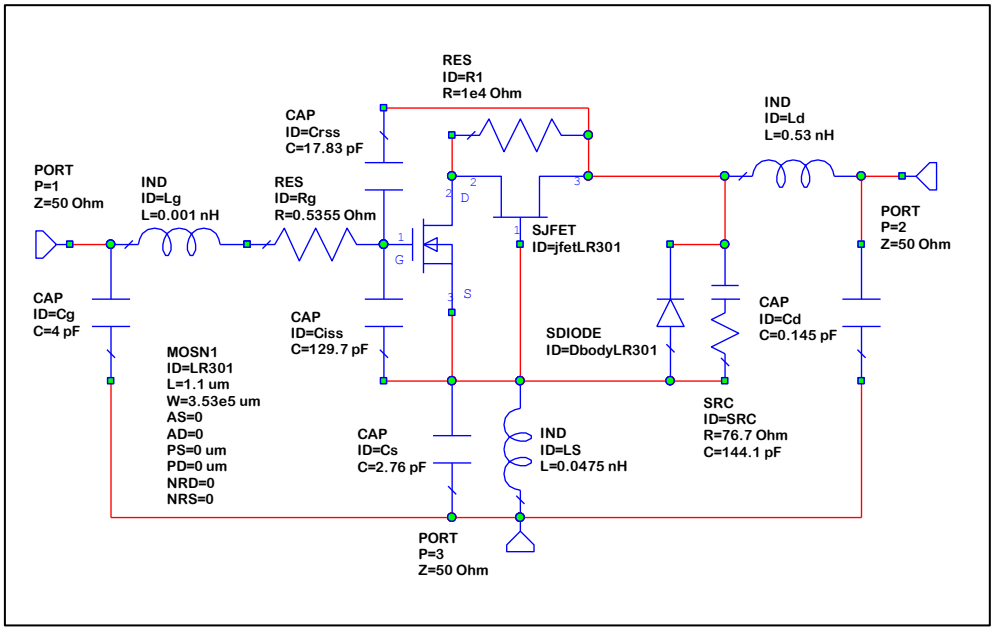


Fig. 2.32: Transistor model used for circuit simulation of 270 W amplifier

The input-output impedance matching networks were designed using the planar microstrip transmission lines and coaxial transmission line balanced-to-unbalanced transformer

(balun). For push-pull design, the balun is an important component affecting PA operation [158]. An identical 50 Ω balun (left part of Fig. 2.33) may be used at the input as well as the output of the transistor. However, for performing impedance transformation as well as balanced to unbalanced conversion, 25 Ω baluns are more popular in the PA designs. With 25 Ω baluns, the impedance matching is easier, as depicted in the right part of Fig. 2.33, due to very low output impedance of this transistor. In power amplifiers, while the input and the output baluns share many similarities, some of the goals are different, so the design approach is also different. For the input balun, the goal is to match the low impedance at the gate to the 50 Ω source. Unlike this, the output balun design may present the desired load impedances at the fundamental frequency as well as at the harmonics. Between the transistor and the balun, there are input and output matching networks.

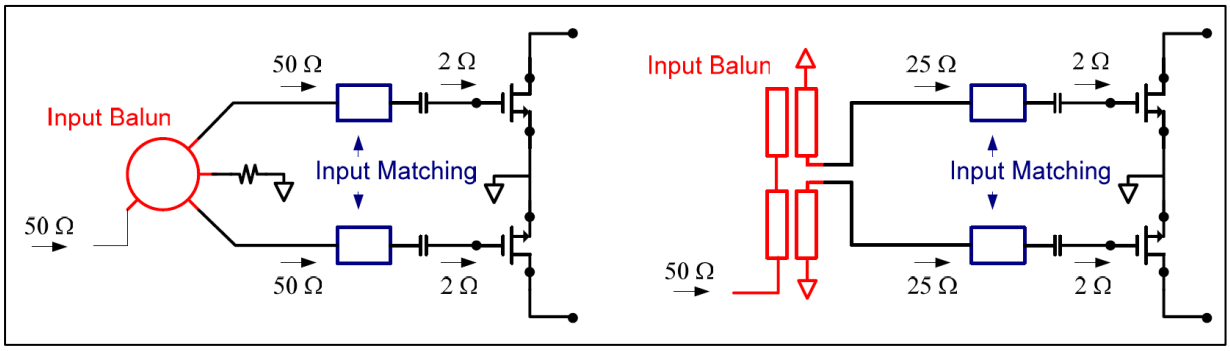


Fig. 2.33: 50 Ω and 25 Ω balanced-to-unbalanced transformer

The complete circuit (Fig. 2.34), including bias circuit, was optimised in Microwave office™ using the harmonic balance analysis. The gate bias was kept at 3.86 V for the Class B operation. The sub-circuits IMNms and OMNms at the gate side and at the drain side respectively, are balanced impedance matching networks with stepped microstrip lines. The harmonic trap was achieved with the output capacitor (equal to 135 pF) of the transistor. During the large signal circuit simulation, the calculated power gain, gain flatness, and input return loss were optimised with increasing input power. At the high input power, the drain efficiency was optimized by tuning output lumped capacitors (C5 and C11).

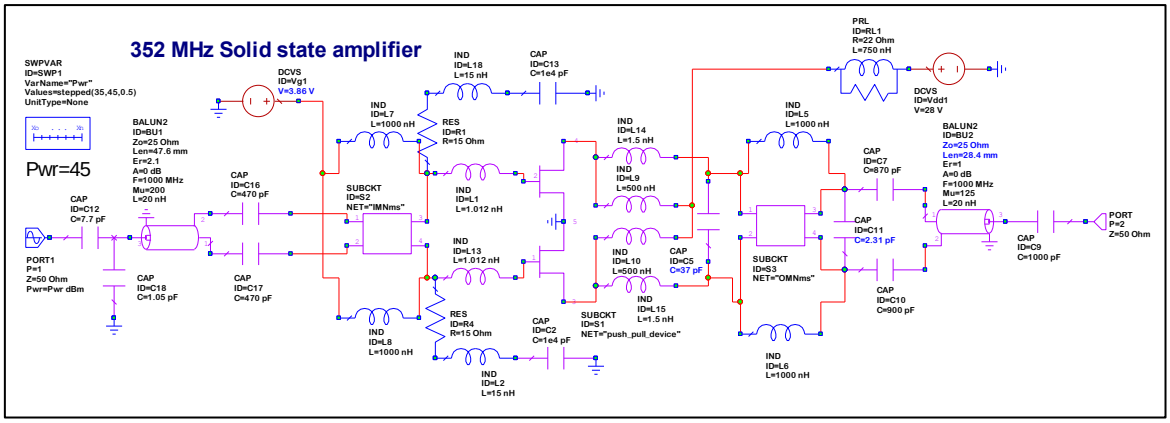


Fig. 2.34: Circuit schematic of 270 W amplifier

The simulation results were further optimized by changing the length of balun lines and microstrip lines while observing their effect on the PA gain and efficiency. In the final circuit, inductors at output were replaced with stepped microstrip line. For coaxial line baluns, at the input as well as output side, balancing planar microstrip lines were added for better isolation among balanced ports. The simulation results for the power gain, return loss and output power are shown in Fig. 2.35 and Fig. 2.36.

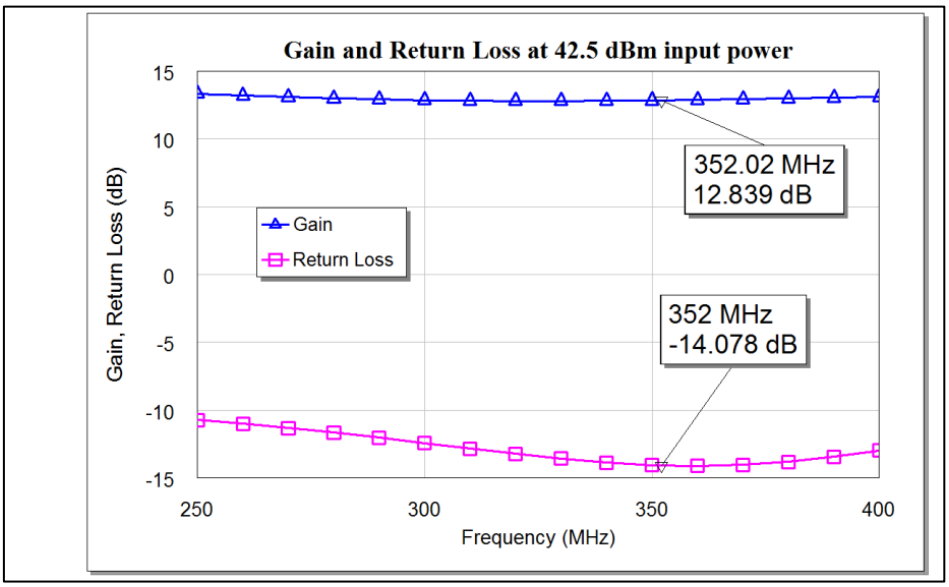


Fig. 2.35: Simulated gain and return loss for the 270 W amplifier at 352 MHz

Simulated swept power response shows a CW output power of 54.42 dBm (276.7 W) and conversion efficiency of 65.68%. This value is lower than the ideal one for the Class B

(78.5%) due to finite knee voltage. The PAE, which takes contribution of input power into account, closely follows the DC to RF efficiency.

The complete circuit was printed on a FR-4 board. The actual fabricated and assembled HPA is shown in Fig. 2.37 along with the DC bias circuit and output circulator. Its layout measures 250 mm and 140 mm in length and width, respectively. It is water cooled with the help of water channels below the transistor seating and drilled through the copper plate.

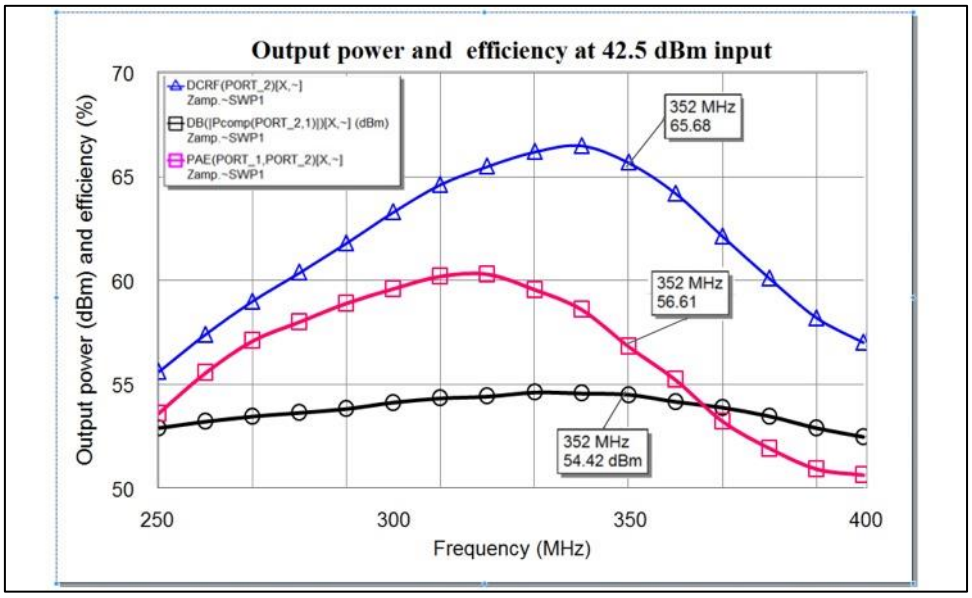
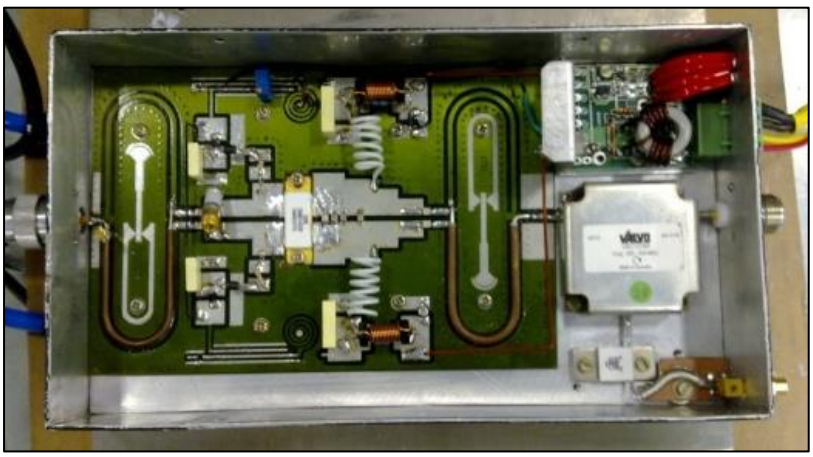


Fig. 2.36: Simulated swept power response of 270 W amplifier



Brief Details

Length, Width: 25 cm, 14 cm

Outer Height: 5 cm

Substrate Type: FR-4

Input Connector: N type

Output Connector: N type

DC Bias: 28 V

Fig. 2.37: Fabricated 270 W solid state amplifier

Fig. 2.38 shows the measured power, gain and efficiency for swept input power. The measured efficiency and output power, at 42.5 dBm of input power, are 62.6% and 281.8 W,

respectively. This value of efficiency is slightly lower than simulated result (65.68%) but output power (54.5 dBm or 281.8 W) is quite satisfactory. In fact, the fine tuning carried out with the help of input and output lumped capacitors was focused for obtaining output power equal to or more than 270 W. At high power, the gain rolls off still maintaining desired value of 12 dB. The PA operation beyond 43 dBm of input power degrades efficiency and gain due to nonlinear harmonic components generation. The return loss at the input port is satisfactory.

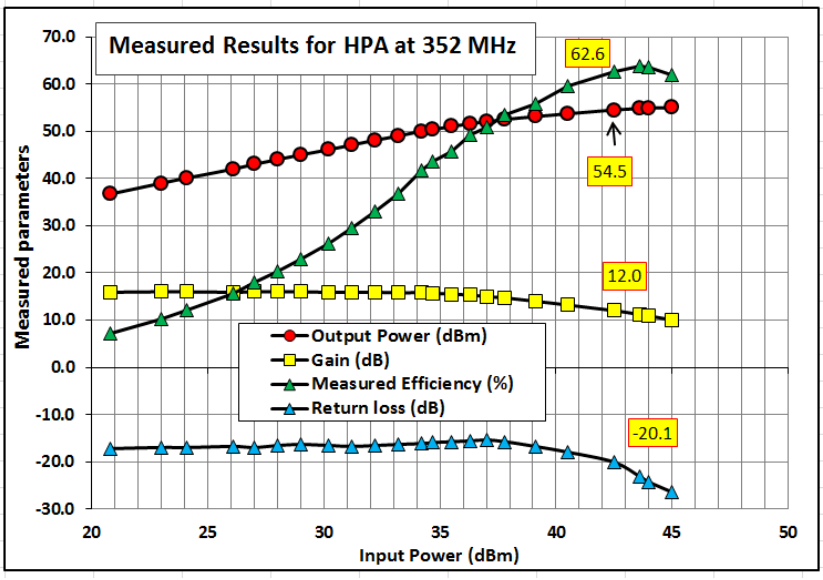


Fig. 2.38: Measured power transfer characteristics of 270 W amplifier at 352 MHz

2.6.1.3 High Power (400 W) Amplifier at 505.8 MHz

With the availability of newer transistors, operating at a drain supply of 50 V, higher power design for PA using the Class AB was examined at 505.8 MHz. For this purpose, LDMOS BLF 573 from NXP was selected, based on the transistor's key parameters and circuit simulation study. As per the data sheet, this transistor is capable of providing 300 W at 225 MHz and 50 V DC bias. Based on the power vs. frequency roll-off simulation studies, carried out in Microwave Office™, an output power of 260 W (at 505.8 MHz) was estimated from this transistor. Compared to the earlier HPA at 270 W, an output power of 400 W was set for the present one, in order to experience higher power design. To fulfil such require-ment, the design was planned with two transistors (BLF 573); power combined using a

Wilkinson divider and a combiner, in the same circuit. Thus, for each transistor, same impedance matching networks and the *deep* Class AB bias circuit needs to be designed. The important design specifications of this amplifier are listed in Table 2.3. This design was started by source and load pull simulation studies for generating dynamic load line for the selected transistor, in the Class AB operating mode. Motorola MET model was used with linear capacitors for gate as well as drain terminal. The simulation circuit (Fig. 2.39) was designed in Microwave office™.

Table 2.3: Specification of 400 W RF power amplifier module

Sr.	Parameter	Value
1	Rated RF Power Output and Power Gain (at 1-dB point)	400 W, 18 dB
2	Operating frequency and 1-dB Bandwidth	505.8 MHz, ± 5 MHz
3	Operating Mode/ Class of operation/Efficiency	CW/ AB/ 58%
4	Harmonic Distortion/ Spurious Output	-25 dBc / -35 dBc
5	Cooling	Water cooled at 30°C

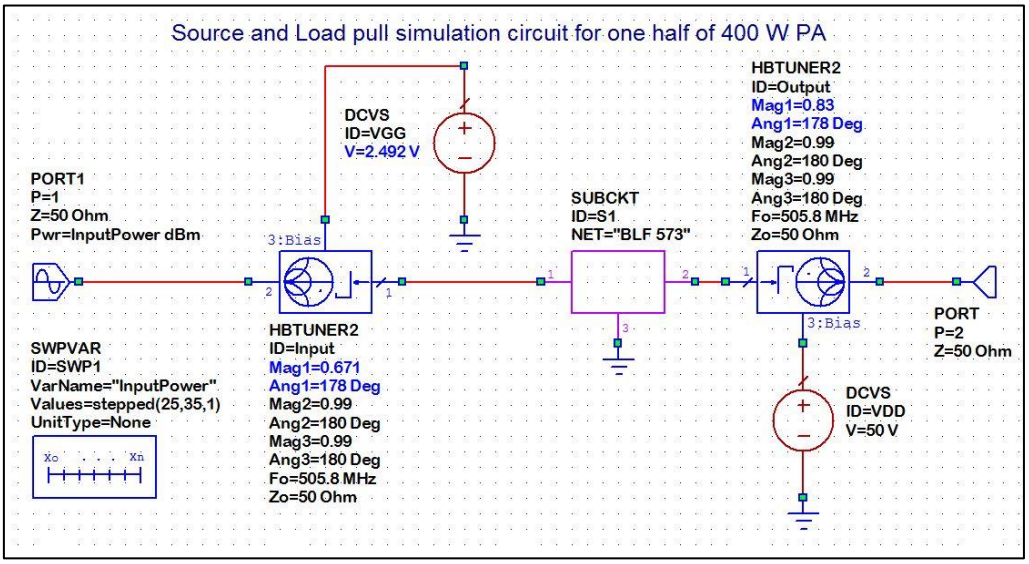


Fig. 2.39: Source and load pull simulation circuit for BLF 573 MOSFET

The harmonic balance tuners at the gate and drain side of the transistor, present necessary fundamental terminations and short circuits for the rest of harmonics. With $V_{DD} = 50V, V_k = 7V$ and $I_{max} = 26.7\,A$, an optimum load line resistance for deep class AB,

considered hereafter Class B, was calculated using (2.29) and (2.53) as 3.03 Ω. Simulated IV characteristics and dynamic load line, based on the calculated value of load resistance, is shown in Fig. 2.40. Due to complex nature of the fundamental load impedance, the load line shows a looping-characteristic. The negative current in the dynamic load-line results from both the energy storage in the drain capacitance and the self-biasing associated with the transistor nonlinearity. The simulated drain voltage and drain current waveform, for one transistor, are shown in Fig. 2.41.

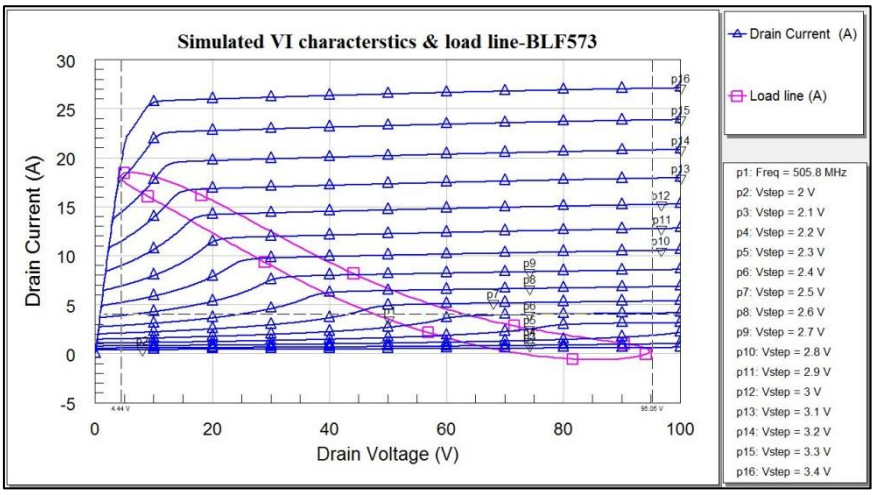


Fig. 2.40: Simulated IV characteristics with load line for BLF 573 MOSFET

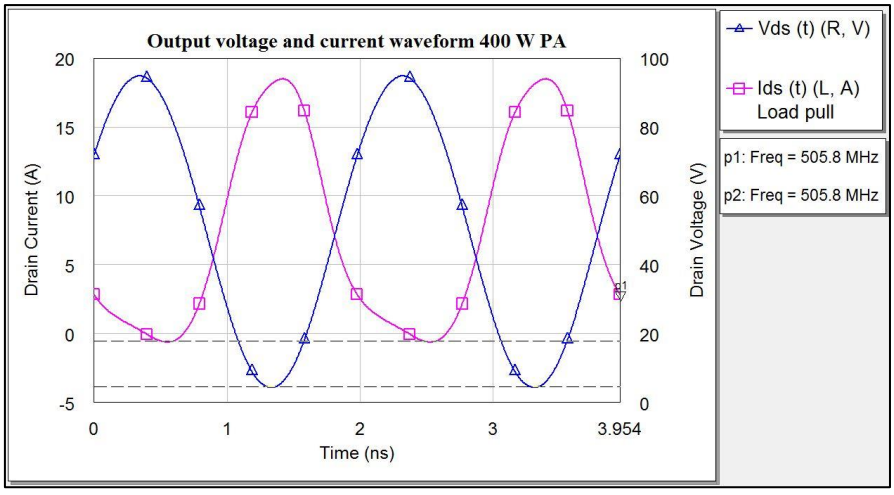


Fig. 2.41: Simulated drain voltage and current for one half of 400 W amplifier

Due to the short circuit of second and third harmonic, the drain voltage is quite sinusoid, making excursion from V_k to 96 V. The drain current, excited in response to gate voltage, is

near to half sinusoidal in shape due to transistor's parasitic components. Its peak value is lower than I_{max}. The simulated frequency response (Fig. 2.42) shows a CW output power of 53.3 dBm or 213.8 W at the centre frequency. The corresponding conversion efficiency is 58.24 % for the Class AB operation. The PAE again closely follows DC to RF efficiency. As seen in the simulated AM-AM plot in Fig. 2.43, 1-dB compression point is beyond 54 dBm. Beyond an input power of 2 W, the nonlinearity of the transistor comes in picture and insertion phase changes with increasing the input excitation.

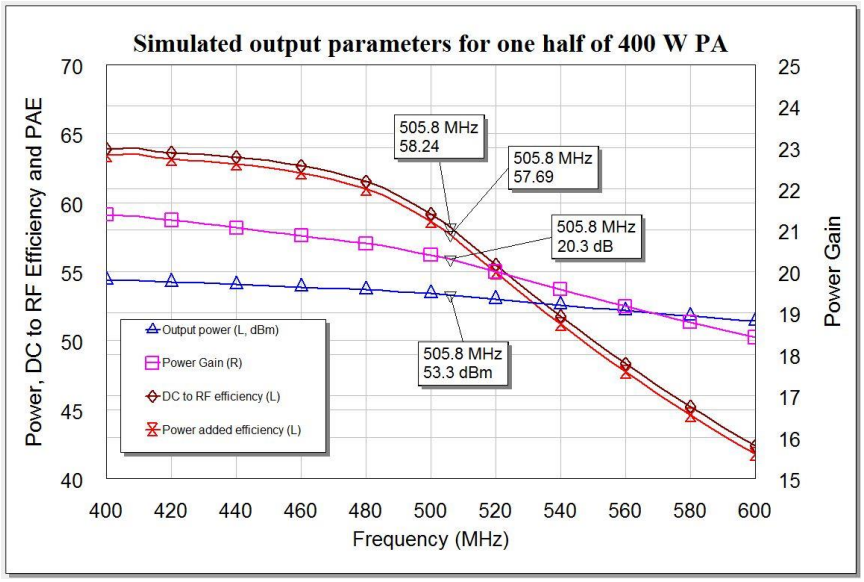


Fig. 2.42: Simulated power, gain and efficiency for one half of 400 W amplifier

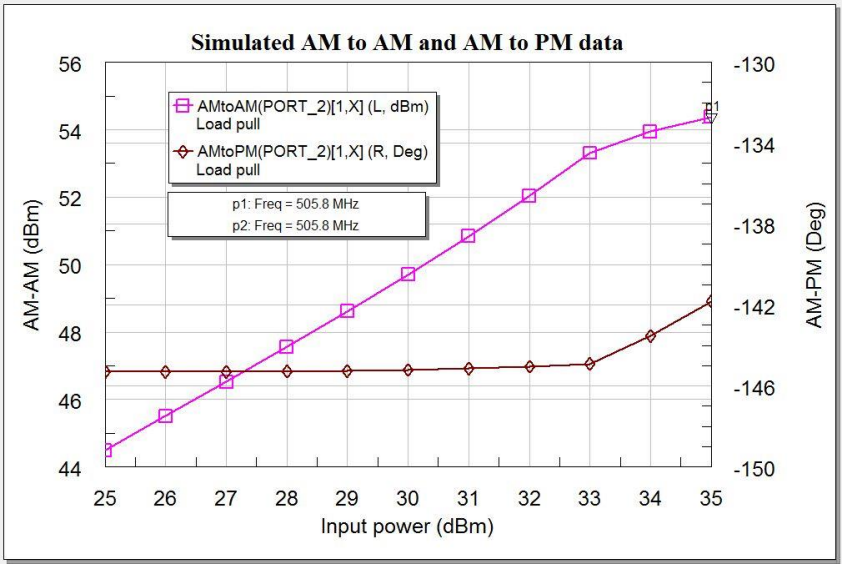


Fig. 2.43: Simulated AM-AM and AM-PM data for one half of 400 W amplifier

The harmonic power at the input power of 33 dBm is shown in Fig. 2.44 as spectral response. The second harmonic is 25 dB below fundamental tone. In order to match the source/load impedance of the transistor, calculated from source/load pull simulation, to the system impedance of 50 Ω, few coaxial transformers were used in the circuit. Fig. 2.45 shows the final bias and output impedance matching circuit (without the Wilkinson divider and combiner), designed for one half of this PA. The quiescent bias at the gate was set at 2.5 V.

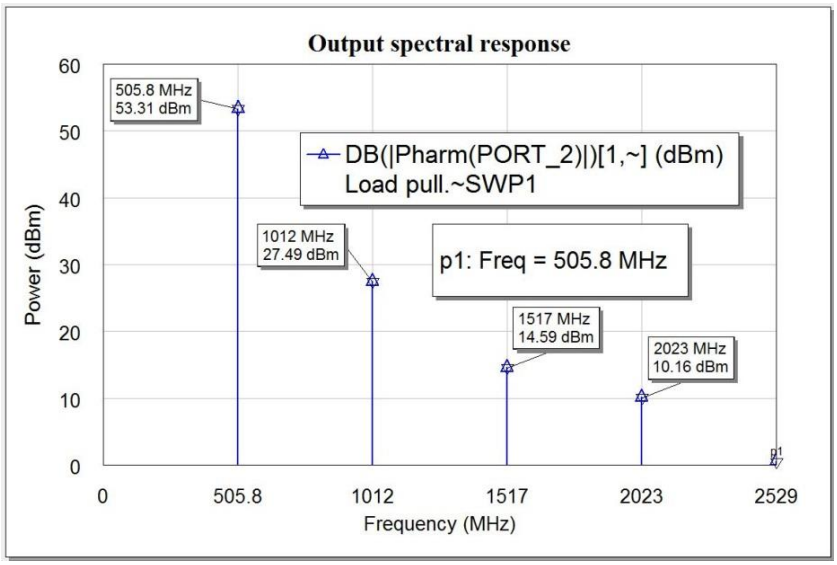


Fig. 2.44: Simulated spectral response for one half of 400 W amplifier

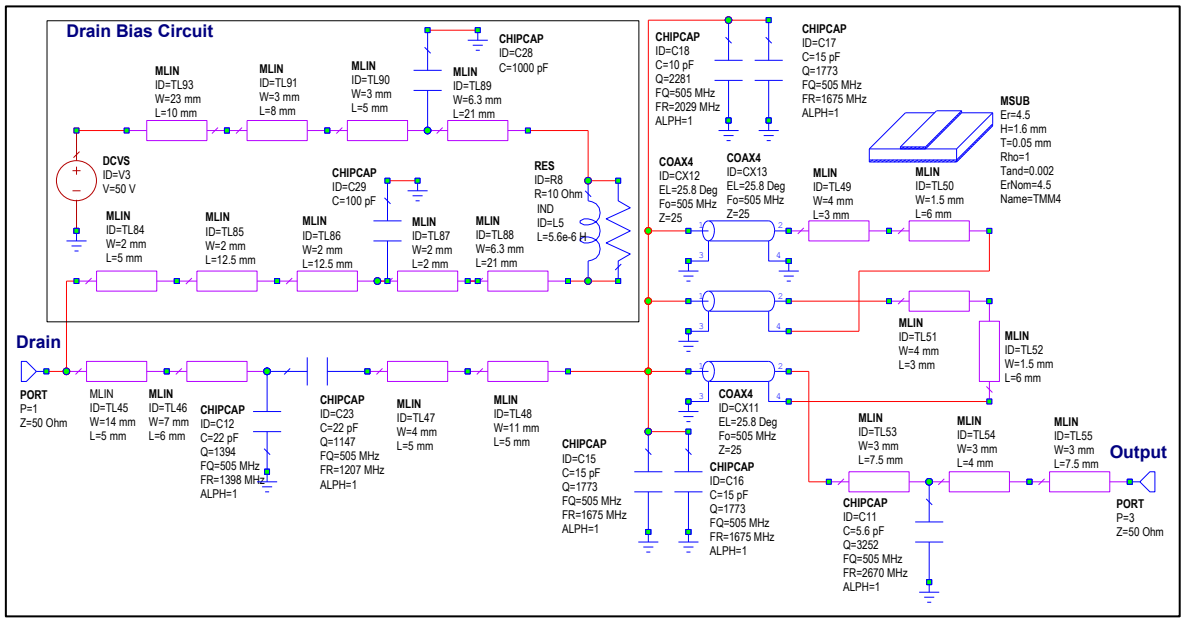
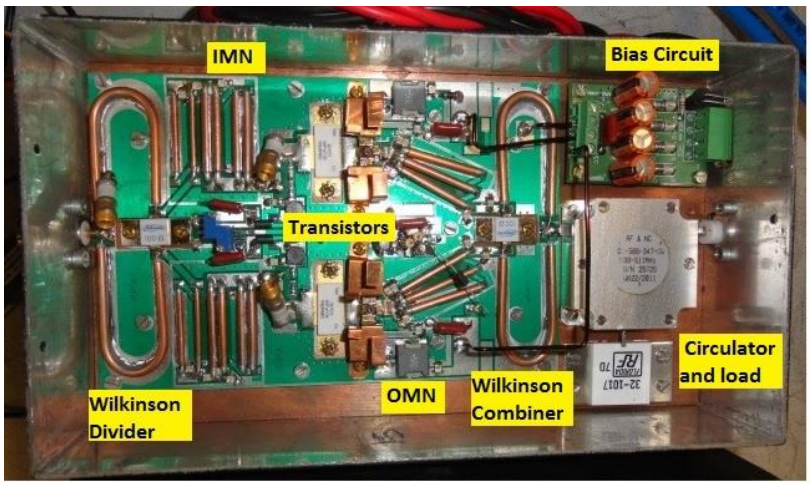


Fig. 2.45: Output impedance matching network for one half of the 400 W amplifier

The simulation results were further improved by operating this module at different gate voltage and testing its effect on gain and power conversion efficiency. The layout of PA circuit was generated and printed on an RF board (TMM4™), having a relative permittivity of 4.5 and substrate thickness of 1.6 mm. A 400 W circulator (from RF & Noise Components Ltd. with insertion loss of 0.2 dB), placed before the final output, protects the transistor from the reflected power. The PCB of this PA was mounted directly on a water cooled cold plate (heat-sink). This scheme allows sitting of LDMOS transistors directly over this plate, improving thermal performance of PAs. Minute air gaps between top of the cold plate surface and bottom of LDMOS metal flange were removed by applying a thin layer of Silicone oil based thermal compound having thermal resistance of only 0.05°C/W (for a 25 μm thick layer with area of 4 cm^2). Fig. 2.46 shows the inner view of this PA module. For cooling of chip capacitors, connected near the drain terminal, small copper heat sinks were used. These heat sinks were realised with copper foil by connecting their one end with the capacitor and another one, bolted to the cold plate. The standard N type connectors were used at its input and output.



Brief Details

Length, Width: 24 cm, 14 cm

Outer Height: 4 cm

Substrate Type: TMM4™

Input Connector: N type

Output Connector: N type

DC Bias: 50 V

Cooling: Water cooled

Fig. 2.46: Fabricated 400 W amplifier

The measured power transfer characteristic (Fig. 2.47) is linear; however, its efficiency and input return loss are lower than the calculated values. This must be due to the fine tuning

of PA with an emphasis on obtaining linear output power with a minimum value of 400 W. The relative phase spread of this module is 12° for an output power excursion from 200 W to 500 W. From this data, the AM to PM conversion was measured as 2°/dB, centred at an input power of 38 dBm and an output power of 56 dBm.

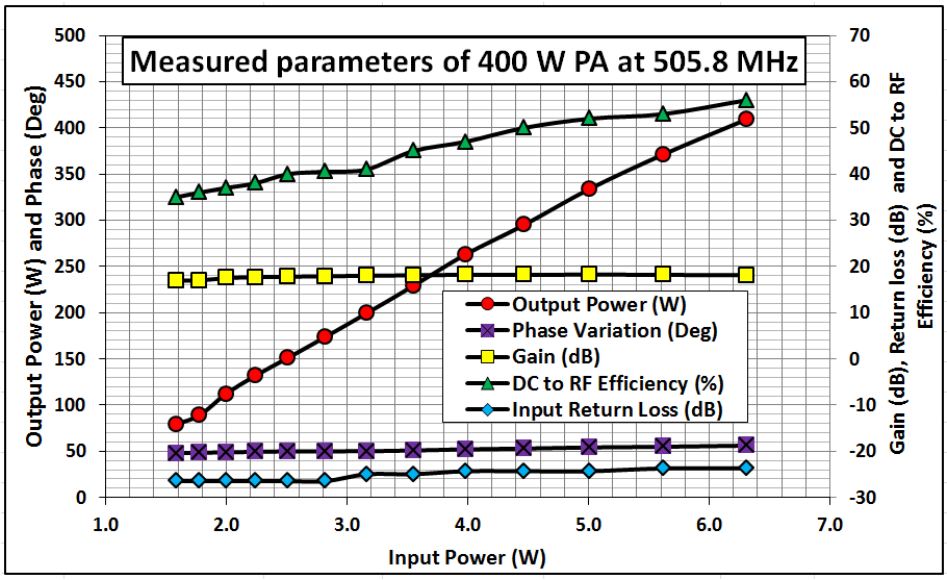


Fig. 2.47: Measured gain, return loss, phase and efficiency for 400 W amplifier

In this chapter, the necessary analysis and experimental investigation was carried out for the harmonic shorted or tuned load PAs, with an output power up to 400 W. The presented designs of the low and high power amplifier modules were based on the Class A, B and AB modes. The PA module, required in multiple in a high power SSPA system, is the main component deciding system efficiency and the output power. The Class A, B and AB mode based PAs are less attractive due to the requirement of a specific and multi-harmonic short circuit. Further, the transistor‘s parasitic component and nonlinear operation at high power prohibit achieving higher power. Hence, it is necessary to explore newer design techniques for achieving higher power, with flexibility in impedance matching circuit design. This led to the study of harmonic tuned techniques, as detailed in the next chapter.

Chapter 3. Harmonic Tuned Solid State Power Amplifier

The general philosophy for the design of a PA consists in minimising the power dissipation inside the transistor and simultaneously maximising the output RF power and DC to RF conversion efficiency. The conventional modes of operation, studied in the last chapter, try to achieve this goal by tuning the fundamental load with the help of harmonic traps in the output impedance matching network. In doing so, the output voltage waveform is preserved as a sinusoid and it is made to excurse equally around the bias point. For the power transistors, the device/package parasitics, specially the nonlinear output capacitor, are appreciable to reshape this waveform. As a matter of fact, this waveform that does not fall under a single mode. It then becomes a judgment of the designer to ascertain whether it complies with the intended Class or specific mode. Hence, instead of shorting harmonics, they may be terminated in suitable loads to improve efficiency and output power levels [159]. The choice of such harmonic terminations plays a fundamental role and hence, their potential benefits need to be exploited, by developing new design processes that are completely founded on the theoretical waveform analysis. The desired output power, with proper trade off of efficiency within physical constraints of the device, can be obtained with this analysis. The resulting Harmonic Tuned (HT) PA represents a hot discussion topic for the academic world due to their benefits in terms of efficiency, the ease of network design and enhanced output power. In this chapter, the harmonic tuned design space is explored for such advanced modes of PA operation. The presented designs were well supported by the experimental work for PAs, operating in continuous Class J, mixed mode and extended continuous Class F modes, respectively.

3.1 Efficiency Enhancement Conditions

In order to explore the harmonic tuned designs for the PA, it is necessary to start with the conditions governing the physical power equilibrium involved in the amplifying process.

With reference to the mathematical formulation developed in section 2.4, the total DC power, supplied to the PA, must equal the RF power delivered to the fundamental termination and harmonic frequencies plus the dissipated power in the transistor, i.e.

$$P_{DC} = P_{diss} + P_1 + \sum_{n=2}^{\infty} P_n \tag{3.1}$$

And the drain efficiency η_{pa} of the PA under consideration is

$$\eta_{pa} = \frac{P_1}{P_{DC}} = \frac{P_1}{P_{diss} + P_1 + \sum_{n=2}^{\infty} P_n} \tag{3.2}$$

The theoretical maximum drain efficiency (η_{pa} = 100%) is obtained if the following condition is satisfied:

$$P_{diss} + \sum_{n=2}^{\infty} P_n = 0 \tag{3.3}$$

As both of these functions can have zero or positive value, this equation results in

$$P_{diss} = \frac{1}{2\pi} \int_0^{2\pi} V_{ds}(\theta).I_{ds}(\theta) d\theta = 0 \tag{3.4}$$

$$\sum_{n=2}^{\infty} P_n = \frac{1}{2} \sum_{n=2}^{\infty} V_n I_n \cos(\varphi_n) = 0 \tag{3.5}$$

Equation (3.4) is a mathematical counterpart of the non-overlapping condition between the output voltage and current waveforms. It can be accomplished by proper wave shaping [160], i.e. by forcing the current on the device to vanish for a non-zero voltage and vice versa. However, the fulfilment of the condition (3.4) alone is not sufficient to achieve maximum theoretical drain efficiency; (3.5) or zeroing of the output power dissipated at harmonic frequencies has to be simultaneously enforced. Such condition is fulfilled in tuned load operation by shorting all of the harmonics. A different possibility to achieve a theoretical 100% efficiency is to resort to reactive harmonic terminations. In this way it is possible to ensure a proper phase shift between voltage and current harmonics. Such a condition is obtained in the classical Class E configuration, discussed in the last chapter. In harmonic

tuned amplifiers, similar effort is done by selective tuning of harmonics generated by the drain current stimulus with the help of a set of terminations at the output. In such waveform shaping voltage and current overlap is minimised, while no active power is delivered to such terminations. At the same time, the simultaneous maximization of output current and voltage swings within transistor physical limitations actually guarantees a maximum output power delivered to the fundamental load.

This advantage can be illustrated for the Class F mode with only odd harmonics. For such case, the drain voltage takes the shape of a square-wave [64], with peak-peak voltage swing of $2V_{DD}$. The corresponding fundamental voltage component V_1 is equal to $\frac{4}{\pi}V_{DD}$. This is nearly 27% higher than the corresponding voltage when biased in the Class-A, with the zero to peak output voltage swing is just V_{DD}. Because the fundamental component of the output current remains the same, with a zero to-peak value of $I_{max}/2$, the output power from the Class-F amplifier is about 1 dB higher than that for the Class-A. Furthermore, being efficient design, the transistor can run at a cooler temperature with more reliability. In practice, it is difficult to control more than 5^{th} harmonic and resonators are lossy and additional losses present diminishing returns on efficiency and output power. Hence, harmonic tuned PA with finite harmonics is an optimum choice for practical circuits.

3.2 Harmonic Tuned Amplifier with a Finite Number of Harmonics

In a low frequency PA, a large number of harmonic terminations can be controlled. However, at RF and microwave only a limited number of harmonics can be effectively controlled. For UHF power transistors, operating in a power regime of 300-500 W, the output shunt capacitance is of the order of 100-200 pF. Being such a large capacitor, it provides a short circuit to the higher order harmonics generated at the transistor plane. Also sometimes the benefits achieved by managing the higher-order harmonics become negligible, if they are compared to the growing circuit complexity and the resulting power loss. Thus at RF and

microwave, PA design techniques should make use of limited harmonic components to result the best possible performance. Hence, the analysis can be performed by limiting the index n below or equal to 4. The corresponding drain voltage, given by (2.13) becomes

$$V_{ds}(\theta) = V_{DD} - V_1 \cos(\theta + \psi_1) - V_2 \cos(2\theta + \psi_2) - V_3 \cos(3\theta + \psi_3) - V_4 \cos(4\theta + \psi_4) \tag{3.6}$$

For the voltage driven current source model of the MOSFET, $I_{ds}(\theta)$ depends on the input (gate) drive and the bias, thus allowing it to be coupled to drain voltage (V_{ds}) through the load impedances (Z_n). Hence, the fundamental and harmonic impedances, required for the design of output matching network (OMN) of the PA, can be calculated from the knowledge of voltage and current waveforms. For such case, OMN can be divided into different parts as shown in Fig. 3.1.

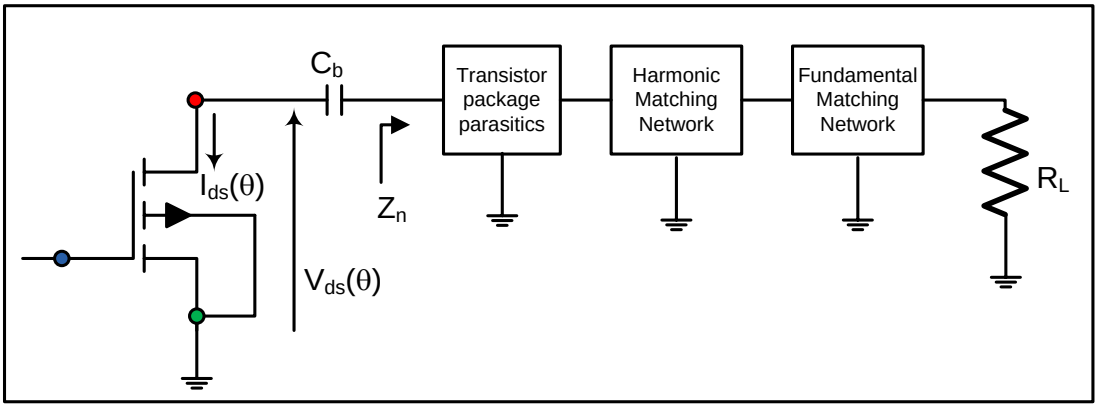


Fig. 3.1: Output matching network for harmonic tuned RF amplifier

In majority of the cases, the Class B mode is used to set the drain current waveform, given by modifying (2.6) for the half sinusoid as

$$I_{ds}(\theta) = I_{max}\left(\frac{1}{\pi} + \frac{1}{2}\cos\theta + \frac{2}{\pi}\sum_{n,even}\frac{(-1)^{\frac{n}{2}+1}}{n^2-1}\cos n\theta\right) \tag{3.7}$$

Some other choices for $I_{ds}(\theta)$ are listed in the appendix B. In order to enhance the performance by harmonic tuning, it is necessary to increase the fundamental voltage amplitude (V_1) by tuning or manipulating harmonics (V_n) in proper phase and amplitude. There may be

many choices or unlimited design space for achieving this goal. The resulting wave shaped voltage is a different non-sinusoidal voltage waveform, with the enhanced fundamental component.

3.2.1 Analysis and Design Goal

The primary goal of the harmonic tuned techniques is to increase the output power by enhancing the fundamental voltage component with selected mixing (in proper amplitude and phase) of the harmonic components. To focus the goal of the analysis, the voltage amplitudes at the fundamental and harmonic frequencies in (3.6) can be replaced by useful design coefficients as

$$V_{ds}(\theta) = V_{DD} - \delta \cdot V_{1,TL}\cos(\theta + \psi_1) - \delta \cdot k_2 \cdot V_{1,TL}\cos(2\theta + \psi_2) - \delta \cdot k_3 \cdot V_{1,TL}\cos(3\theta + \psi_3) - \delta \cdot k_4 \cdot V_{1,TL}\cos(4\theta + \psi_4) \tag{3.8}$$

Voltage gain function δ and the design coefficients k_n are defined as

$$\delta \equiv \frac{V_1}{V_{1,TL}} \qquad k_n \equiv \frac{V_n}{V_1} \quad n = 1,2,3,4 \tag{3.9}$$

The suitable choice of design coefficients k_n and ψ_n provides a voltage gain of δ, for the fundamental component V_1, compared to the un-manipulated or tuned load case ($V_{1,TL}$), for the same bias conditions. The effect of the knee voltage can be included by substituting the value of $V_{1,TL}$ from (2.54) in (3.8) as

$$V_{ds}(\theta) = V_{DD}[1 - \delta\chi \cdot \{\cos(\theta + \psi_1) + k_2\cos(2\theta + \psi_2) + k_3\cos(3\theta + \psi_3) + k_4\cos(4\theta + \psi_4)\}] \tag{3.10}$$

For plotting the waveforms, during the analysis, the normalised drain voltage waveform (with respect to V_{DD}) is more useful. It can be defined as

$$v_{ds}(\theta) = \frac{V_{ds}(\theta)}{V_{DD}} = [1 - \delta\chi \cdot \{\cos(\theta + \psi_1) + k_2\cos(2\theta + \psi_2) + k_3\cos(3\theta + \psi_3) + k_4\cos(4\theta + \psi_4)\}] \tag{3.11}$$

The design procedure for the harmonic tuned PA includes the optimisation of δ as a function of design coefficients (k_n and ψ_n); subject to constraints on the drain voltage excursion. These constraints are dictated by the transistor's physical limits *viz.* V_k (lower limit) and V_{max} (upper limit). The simple expression (3.8) for the drain voltage does generate a rather diverse set of waveforms, depending on the values of the coefficients. The key point is the zero crossing of the voltage waveform depending upon the actual values of the coefficients. If this waveform crosses zero at any point the device current will drop immediately, resulting in a drastic reduction in the output power and efficiency. Also this current may try to collapse and it may trigger a whole range of highly undesirable effects, like clipping, compression and so on. Hence, as a PA designer, out of two physical limits, the lower limit is of a particular interest. Hence, for each combination of k_n and ψ_n, the voltage waveform $V_{ds}(\theta)$ is kept equal to zero or above a global minima (for non-zero V_k). Such *zero-grazing* operation [161], where a relationship can be established between the coefficients causing the voltage waveform to touch but not cross zero, is a necessary condition for all harmonic tuned modes. In harmonic shorted modes, it is implicitly achieved due to harmonic traps.

For design purpose, it is necessary to compute a set of positive definite or *zero grazing* waveform and corresponding impedances for a given current excitation. The procedure can be illustrated for the simple case of tuned load modes (Class A, B and AB.), having complex termination at the fundamental frequency, instead of real one. For such case, $V_{ds}(\theta)$ is given from (3.6) as

$$V_{ds}(\theta) = V_{DD} - V_1 \cos(\theta + \psi_1) \tag{3.12}$$

The choice of V_1 and ψ_1 confirming non-zero-crossing, results in a set of fundamental impedances for a given stimulus. The specific result, plotted on Smith chart for the Class B mode with normalised load equal to 0.6, is shown in Fig. 3.2. The fundamental impedance Z_1 contour, plotted here, sets the diving line between desired (left side) or unclipped and clipped

(right side) drain voltage waveforms. In order to choose specific impedance in the left part, the computed efficiency is also shown on the same plot. The area enclosed by the curves A and B represents the impedances, which can deliver efficiency equal or greater than 50%. Similar analysis can be performed by addition of a second harmonic reactive component to the drain voltage waveform, given by (3.12)

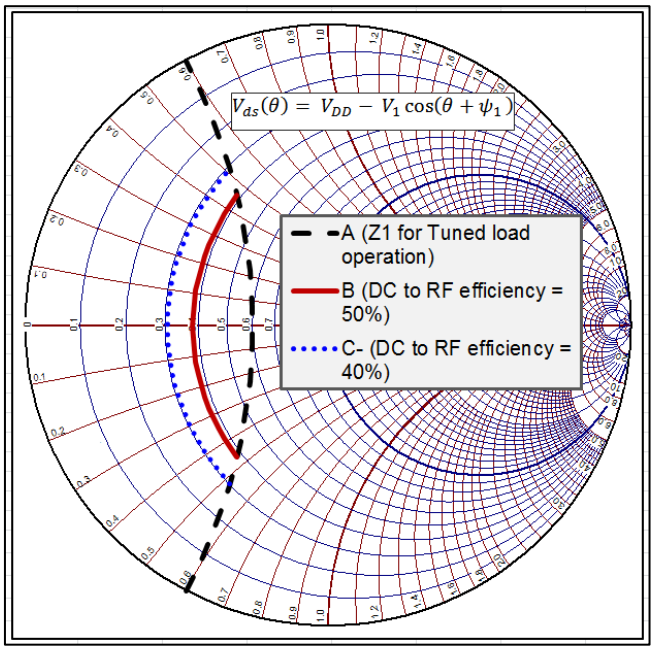


Fig. 3.2: Design curves for non-zero crossing drain voltage waveform

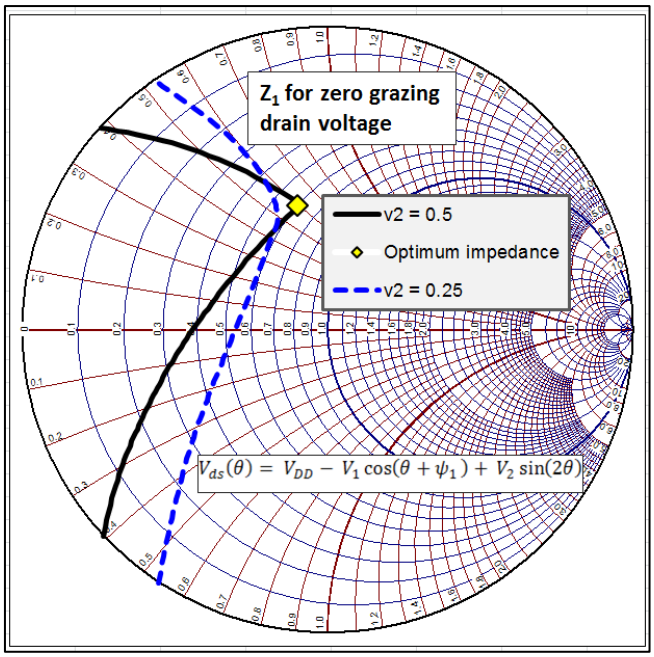


Fig. 3.3: Design curves for non-zero drain voltage with second harmonic reactance

The corresponding waveform is given as

$$V_{ds}(\theta) = V_{DD} - V_1 \cos(\theta + \psi_1) + V_2 \sin(2\theta) \tag{3.13}$$

The Z_1 computed by using this equation and the Class B drain current excitation is shown in Fig. 3.3, for two values of V_2/V_{DD}. Compared to Fig. 3.2, it can be seen that with the addition of a reactive termination at second harmonic, there is reduction in the region of usable design impedance for the output matching network. The optimum impedance point, shown here, corresponds to a conversion efficiency of 78.5%. Such design curves are useful aids while studying harmonic tuned PAs. However, for structured HT modes including higher order harmonics, computation is not so straightforward.

Nevertheless, the design analysis for such modes can be conveniently explored if the drain voltage waveform is shifted by the drain supply (V_{DD}) and normalized with respect to V_1 so that (3.6) becomes

$$\begin{aligned} v_{ds,sn}(\theta) = &-\cos(\theta + \psi_1) - k_2 \cdot \cos(2\theta + \psi_2) \\ &- k_3 \cos(3\theta + \psi_3) - k_4 \cos(4\theta + \psi_4) \end{aligned} \tag{3.14}$$

The lower limit of $v_{ds,sn}(\theta)$, governed by the knee voltage, gets translated as

$$v_{ds,sn}(\theta) \geq -1 \tag{3.15}$$

This limiting value of (-1) corresponds to the tuned load operation with fundamental component of drain voltage waveform, equal to $V_{1,TL}$. Taking this value as a reference for HT modes, the voltage gain or efficiency enhancement occurs when $v_{ds,sn}(\theta)$ takes values greater than (-1). The corresponding $v_{ds,sn}(\theta)$ is a global minimum point, where $dv_{ds,sn}/d\theta = 0$. Thus, quantitatively the voltage gain function can be expressed [80] as

$$\delta = -\frac{1}{min[v_{ds,sn}(k_n, \psi_n)]} \tag{3.16}$$

For simple cases, the calculation of the δ is possible analytically [162] by applying the condition (3.16) on (3.14) . However, for the higher order HT analysis, the trigonometric

complexity escalates rapidly as one solves these equations for the specific coefficients. For such cases, computation of can be carried out numerically or graphically by using the factorized expression, as suggested by Cripps [112].

Comparing to the tuned load operation, an enhancement in the efficiency for harmonic tuned PA, in term of δ, tuned load efficiency and the power factor ($\cos\varphi_1$) is given by

$$\eta_{pa,HT} = \delta \cdot \eta_{pa,TL} \cdot \cos(\varphi_1) \tag{3.17}$$

For calculating the harmonic terminations, the excitation (I_{ds}) waveform needs to be specified. For a practical PA design, it should be remembered that these impedances correspond to their values at the current generator plane of the MOSFET. The frequency dependent parasitics, due to the device as well as its package, need to be incorporated before designing OMN at the accessible reference planes of the MOSFET. To determine the continuous optimum load impedances at such physical plane, the large-signal model of the packaged transistor should be used in the computer simulation.

Some specific cases of HT operation, by adding only third or second or mixture of these components to drain voltage waveform, are analysed in next sections with an introduction of Cripps's factorization approach.

3.3 Third Harmonic Tuned Case and Class F mode

This Class of PA is based on the idea of finding the proper termination for the third harmonic component ($k_3 \neq 0$) only, while assuming the even ones to be short-circuited ($k_2 = k_4 = 0$). It is also assumed that phase shift of individual voltage components are zero ($\psi_n = 0$). Consequently, the voltage waveform in (3.11) can be written as

$$v_{ds}(\theta) = [1 - \delta\chi \cdot \{\cos(\theta) + k_3 \cos(3\theta)\}] \tag{3.18}$$

Thus, proper mixing of third harmonic component results in the value of δ above unity. Its graphical interpretation, with $\chi = 1$, is depicted in Fig. 3.4. The composite waveform

$v_{ds}(\theta)$ (shown by v_{ds}) is made up of the third harmonic component $v_3 \cos(3\theta)$ and the fundamental part $v_1 \cos(\theta)$, shown by $v_{1,HT}$ and $v_{3,HT}$ respectively. For convenience, the tuned load fundamental voltage component $v_{1,TL}\left(= V_{1,TL}/V_{DD}\right)$, is also shown here. Since an odd harmonic component is introduced, the voltage waveform remains symmetrical around its average value. The drain current, shown in this graph, is for the Class B excitation. This is a limiting case of the popular Class F mode [163].

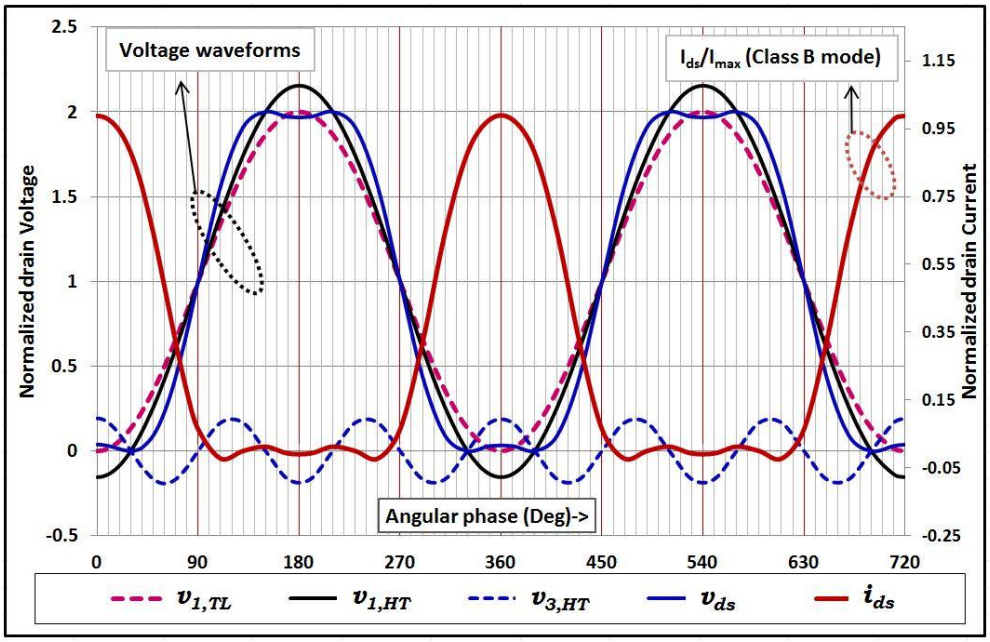


Fig. 3.4: Drain voltage and current waveforms for correct mixing of third harmonic

The purpose of adding this third harmonic component to the output voltage is to increase the waveform's minimum value, thereby flattening the voltage when approaching the device's physical limit. This results in a net voltage gain in V_1 compared to $V_{1,TL}$. On the contrary, a third harmonic component mixed in improper phase, produces a detrimental effect, as depicted in Fig. 3.5, resulting in a lower value of V_1, as compared to the tuned load case (i.e. $\delta < 1$). The Class-F amplifier, a special variant of Class-B, utilizes such plan. The reactive tuning of harmonics, or the replacement of a sinusoidal output voltage at the output with a flatter, squarer periodic waveform provide benefits in both power and efficiency.

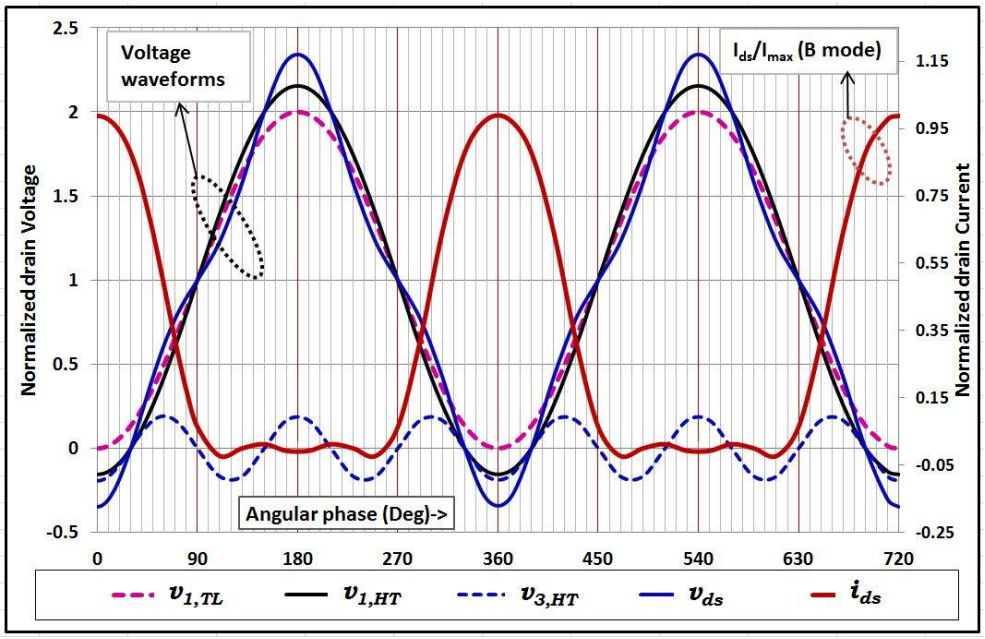


Fig. 3.5: Drain voltage and current waveforms for incorrect mixing of third harmonic

The shifted and normalised version of (3.18) is given as

$$v_{ds,sn}(\theta) = -\cos\theta \cdot [1 - 3k_3 + 4\,k_3 \cdot \cos^2(\theta)]\,] \tag{3.19}$$

For determining voltage gain function in terms of design coefficient, the values of θ where the first derivative of (3.19) becomes zero must be identified, i.e.

$$\frac{dv_{ds,sn}(\theta)}{d\theta} = \sin\theta \cdot [12\,k_3 \cdot \cos^2(\theta) - 3k_3 + 1] = 0 \tag{3.20}$$

The possible solutions of this equation are

$$\begin{aligned} \theta_1 &= 0 \\ \theta_2 &= \pi \\ \theta_3 &= \cos^{-1}\left(\frac{1}{2}\sqrt{\frac{3k_3 - 1}{3k_3}}\right) \\ \theta_4 &= \cos^{-1}\left(-\frac{1}{2}\sqrt{\frac{3k_3 - 1}{3k_3}}\right) \end{aligned} \tag{3.21}$$

The interesting solutions are obviously θ_3 and θ_4, while θ_1 and θ_2 are not interesting extrema. θ_3 and θ_4 will exist if and only if [68]

$$\left[k_3 \leq -\frac{1}{9}\right] \cup \left[k_3 \geq \frac{1}{3}\right] \tag{3.22}$$

A proper flattening of the voltage waveform occurs if and only if $k_3 < 0$. For $k_3 > 0$ a deleterious peaking of the waveform occurs. For $k_3 \leq -\frac{1}{9}$ the resulting δ becomes

$$\delta = -\frac{1}{\frac{3k_3-1}{3} \cdot \sqrt{\frac{3k_3-1}{3k_3}}} \tag{3.23}$$

It exhibits a maximum value of $(2/\sqrt{3})$ corresponding to k_3 equal to (-1/6). Substituting these values of δ and k_3 in (3.18) and by setting $\chi = 1$, we get

$$v_{ds}(\theta) = \left(1 - \frac{2}{\sqrt{3}} \cos\theta + \frac{1}{3\sqrt{3}} \cos 3\theta\right) \tag{3.24}$$

Another interesting value of k_3 is (−1/9). In this case, the derivate of $v_{ds}(\theta)$ has a double coincident zero in θ = 0, so that the second-order derivative also becomes zero. For this maximally flat condition value of δ comes out equal to 1.125.

3.3.1 Efficiency Enhancement and Harmonic Termination

With a half sine wave conduction of I_{ds} (Class B), the maximum theoretical DC to RF efficiency, calculated by (2.44) is 78.5%. With optimum third harmonic tuning ($\delta = 1.1547$, $\varphi_1 = 0$) this efficiency gets enhanced, expressed by (3.17) as

$$\eta_{pa,HT} = \delta \cdot 78.5\ \% = 90.64\% \tag{3.25}$$

This is an optimum value of the efficiency. By using (2.28) and (2.40) the resulting terminations at the current generator plane of the transistor are expressed as

$$Z_1 = \left(\frac{2}{\sqrt{3}}\right) \cdot \frac{V_{DD}}{I_1(\Phi)} \tag{3.26}$$

$$Z_2 = 0$$

$$Z_3 = \infty$$

From a practical point of view, the need to impose these values of Z_2 and Z_3 at the intrinsic transistor's terminals, poses significant restrictions. While, it is relatively simple to

compensate reactive parasitic elements to realize a short-circuit termination for Z_2, the requirement of infinite Z_3 is much more cumbersome. It is well known that the UHF power transistors have a substantial output capacitance. Even if this capacitance is effectively resonated by using an external inductive element, the device output shunt resistance cannot be removed, thus representing an upper limit for Z_3, that can be synthesized across the current source. For such a case, if a pure Class B bias condition is considered, no third harmonic component of the output current is generated. Hence, bias condition need to be changed to the Class deep AB. The knee voltage effect can also be used with proper drive level to contribute third harmonic component in the output drain current. The action of the knee region is to clip the peaks of the current wave, thus generating substantial amounts of third harmonic. There are many choices of the output matching network [164]. One possible realization for achieving open for third harmonic and short for second harmonic using transmission lines is shown in Fig. 3.6. In this circuit, the bias voltage at the drain is supplied with the help of a quarter wave transmission line.

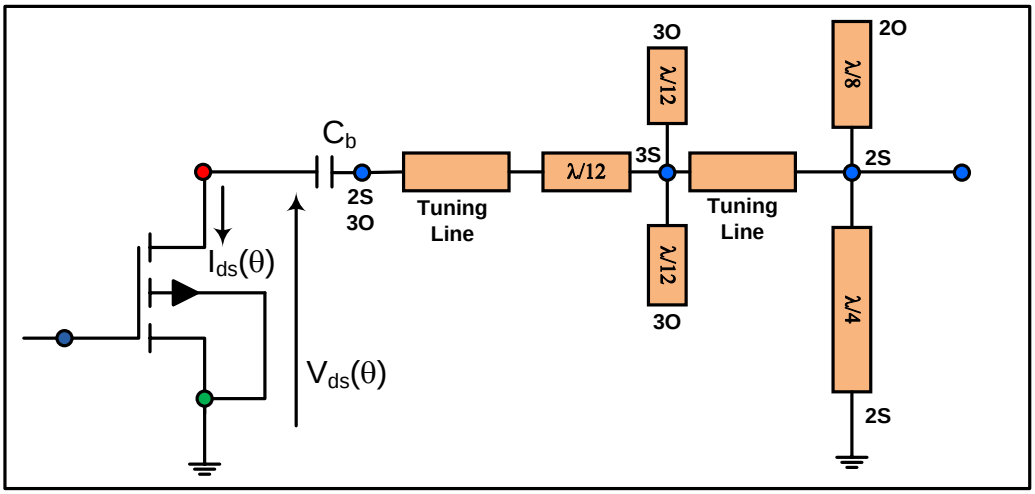


Fig. 3.6: Microstrip output matching network for third harmonic tuning

This line provides a harmonic short for even harmonics at the junction, represented by 2S. An open stub, with length of $\lambda/8$, connected at this point helps in further shorting of even harmonics. Here, λ is the guide wavelength of the RF signal. Two open stubs, each one

having length of $\lambda/12$, connected at 3S, provide shorted third harmonic at this junction. Finally series transmission line, with a length of $\lambda/12$, converts this shorted third harmonic component to the required amplitude signal at 2S3O point. The third harmonic tuned power amplifiers are usually considered as efficient [165] amplifiers. However, the output capacitance of the MOSFET device is not naturally absorbed into network. It needs inductor to tune it out, restricting the bandwidth of the PA. In practice, a perfect harmonic shorting for Z_2 is hard to achieve. Similarly presenting open circuit to Z_3 is another difficult task due to the transistor parasitics.

3.4 Second Harmonic Tuned Case and Class J mode

In this mode of operation, necessary measures are taken to control the second harmonic voltage component only, while short-circuiting the other coefficients ($k_3 = k_4 = 0$). Initially it is assumed that phase shift of individual voltage components are zero ($\psi_n = 0$). Consequently, the voltage waveform (3.8) can be expressed as

$$v_{ds}(\theta) = [1 - \delta\chi \cdot \{\cos(\theta) + k_2 \cos(2\theta)\}] \tag{3.27}$$

Again, to deduce the voltage gain function δ, it is necessary to find the minimum value of shifted and normalized voltage $v_{ds,sn}(\theta)$. It is given as

$$v_{ds,sn}(\theta) = -\cos\theta - k_2 \cdot \cos 2\theta \tag{3.28}$$

Values of θ where the first derivative of (3.28) vanishes are the solutions of

$$\frac{dv_{ds,sn}(\theta)}{d\theta} = \sin\theta + 2\,k_2 \cdot \sin 2\theta = 0 \tag{3.29}$$

It result in following two equations

$$\begin{gathered} \sin\theta = 0 \\ 1 + 4\,k_2 \cos\theta = 0 \end{gathered} \tag{3.30}$$

Solutions from the first equation are not useful whereas, from the second one we get

$$\theta = \cos^{-1}\left(\frac{-1}{4\,k_2}\right) \tag{3.31}$$

It can be deduced that, a proper flattening of the voltage waveform occurs if and only if $k_2 < 0$. Voltage gain function for specified range of $k_2 < -\frac{1}{4}$ becomes

$$\delta = -\frac{1}{k_2 + \frac{1}{8k_2}} \tag{3.32}$$

It exhibits a maximum value of ($\sqrt{2}$) corresponding to k_2 equal to (-1/2$\sqrt{2}$). Expression of $v_{ds}(\theta)$ for this optimum case, with $\chi = 1$, is

$$v_{ds}(\theta) = \left(1 - \sqrt{2}\,\cos\theta + \frac{1}{2}\cos 2\theta\right) \tag{3.33}$$

Fig. 3.7 shows $v_{ds}(\theta)$ for such mixing of second harmonic.

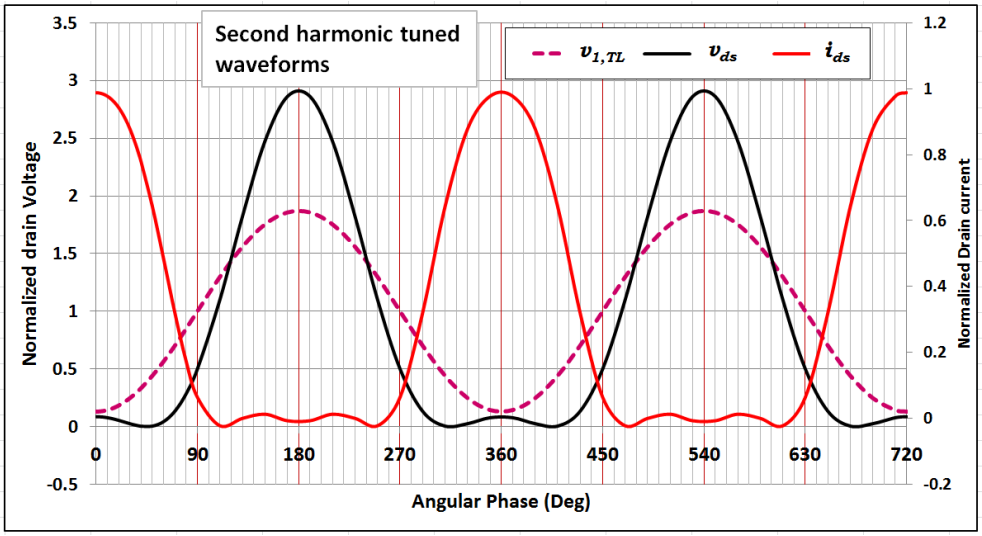


Fig. 3.7: Drain voltage and current waveforms with second harmonic tuning

It is possible to identify a maximally flat condition, arising for $k_2 = -1/4$ and δ equal to 1.333. Comparing to a Class B PA, having maximum theoretical efficiency of 78.5%, it is interesting to calculate the enhancement in the efficiency.

Using (3.17) the enhanced DC to RF conversion efficiency for the present case of second HT efficiency, is given by

$$\eta_{pa,HT} = \delta \cdot 78.5\,\% = \sim 111\%$$

Thus in this case, the efficiency exceeds 100%, indicating that the waveform cannot be generated. Such a waveform can be obtained with the negative second harmonic load. This negative impedance implies that the external second harmonic power should be excited because the passive circuit cannot offer the negative impedance. The Injection Power Amplifier (IPA), reported recently [166], makes use of the active harmonic injection, presenting this negative impedance at the second harmonic.

However, for the present case, to eliminate the negative second harmonic load, the voltage waveform should be shifted by some angle ψ_1 with respect to the drain current waveform. This phase shift is possible with the help of a complex fundamental (capacitive) second harmonic load as shown in Fig. 3.8 for ψ_1 equal to 45°. Such operating mode was reported in 2009 by Cripps [74] , named as a Class-J mode. The normalised drain voltage waveform for the Class J mode thus becomes

$$v_{ds}(\theta) = \left(1 - \sqrt{2}\cos(\theta + \frac{\pi}{4}) + \left(\frac{1}{2}\right)\cos(2\theta + \frac{\pi}{2})\right) \tag{3.34}$$

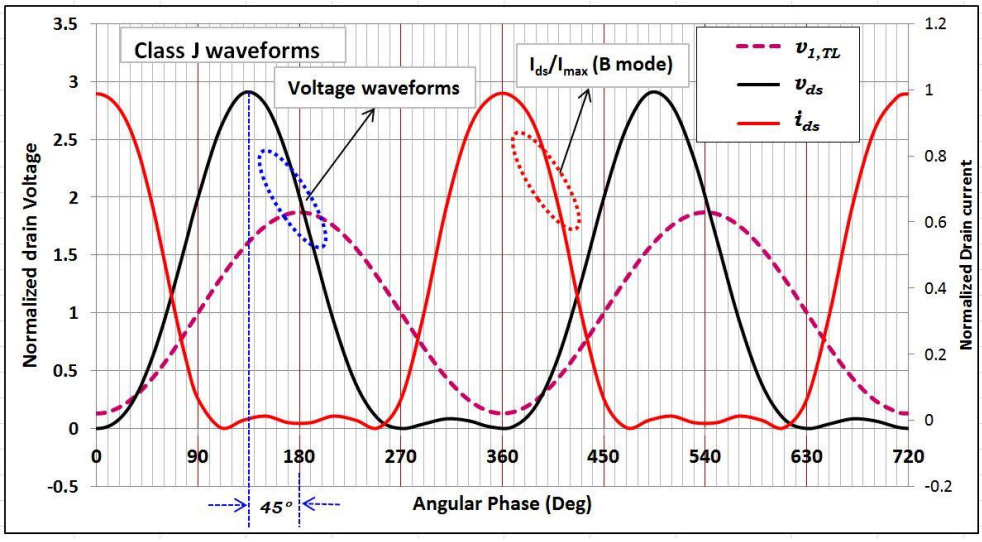


Fig. 3.8: Drain voltage and current waveforms with phase shifted second harmonic

This Class-J operation for PA provides the same efficiency and linearity as Class AB or Class B amplifiers, across a broad frequency range due to the absence of a resonance imped-

ance condition. The corresponding terminating impedances for the Class B drain current excitation are

$$Z_1 = (1 + j) \cdot \frac{V_{DD}}{I_1(\Phi)} \tag{3.35}$$

$$Z_2 = -j\frac{1}{2} \cdot \frac{V_{DD}}{I_2(\Phi)} \tag{3.36}$$

The key difference between Class-J and familiar Class-A, AB and F modes, is the requirement for a reactive component at the fundamental load. Suitability of this operation for the wireless and UHF power amplifier is due to the requirement of a capacitive load at the second harmonic. This capacitor is a part of the transistors (LDMOS) and thus provided by the device itself. In fact, most of the 50V UHF MOSFETs (Table 3.1) have significant value of drain-source capacitor. It provides nearly a short circuit at the third harmonic and above.

Table 3.1: Typical value of output capacitor for high power UHF transistors

Sr.	Device, its power, operational frequency and maximum $\mathbf{V_{ds}}$	Output capacitance	Reactance at 500 MHz (Xc)	Load line resistance at $\mathbf{V_{DD}}$=50V
1	MRFE6VP8600, 600 W, 860 MHz, 130V	80 pF	3.98 Ω	1.6 Ω
2	BLF888B, 650 W, 860 MHz, 110V	67 pF	4.75 Ω	1.6 Ω
3	MRF6V4300N, 300 W, 450 MHz, 110V	105 pF	3.03 Ω	1.6 Ω
4	MRF6VP41KH, 1000 W (Pulse), 500 MHz, 110V	147 pF	2.17 Ω	1.6 Ω
5	BLF573, 300 W, 230 MHz, 110V	103 pF	3.09 Ω	3.2 Ω
6	MRF6VP61KH, 1250 W (Pulse), 500 MHz, 125V	185 pF	1.72 Ω	1.6 Ω

Thus for the Class J wave shaping, this capacitor is naturally absorbed in the circuit (OMN) without its tuning as required in the Class F mode. Due to a natural treatment of the nonlinear output capacitor of RF transistors and ease in the design of wideband output matching network, the Class J is a good choice [167] for the PA designers. However, for

some requirements, instead of pure Class F or Class J operation, continuous or mixed harmonic design is more suitable, as discussed next.

3.5 Continuous and Mixed Mode Design Space

The Class-J is inherently a mode that supports a wide band operation and simplicity in designing the output matching network. It is inherently a linear mode as the design methodology used and the voltage waveform that can be engineered away from the knee region boundary. Nevertheless, this operation requires a high peak voltage at the drain terminal of the transistor (> $3V_{DD}$). The present device technology (Table 3.1) for the UHF power MOSFETs, hardly permits this voltage to be more than twice of the rated power supply voltage (V_{DD}). Other sub optimum solutions to resolves this problem, lies in the selection of angle ψ_1 other than the optimum one. Such solutions present a design space for a given device with its practicalities. The resulting operation modes, from such solutions, are known as *continuous* modes [72] or *mixed-modes* [113] of transistor operation. For high power amplifier design, these sub optimum operations are more advantageous in view of transistor's physical limitations. Its introduction and formulation have provided an alternative design route, for the realization of high efficiency power amplifiers, over a wide bandwidth. They deliver nearly the same power and efficiency as the popular modes (Class, J, Class F, etc.), on which they are based. Similarly the mixed mode of operation, with even as well as odd harmonics [168], has also drawn attention in the research community [112]. The formulation of these types of modes provides a mathematical framework, to describe sets of the fundamental/harmonic impedance reactive loci. Three such formulations are discussed here in view of designing high power solid-state amplifiers with practical limits of the RF transistor. The first two formulations incorporate a continuous design space for the Class J and Class F operations of the PA. The last one is a mixed mode approach discussed with the incorporation

of the third as well as second harmonic. After this, for the sake of the completeness, the inverse Class F mode which became popular recently, is also disused in brief.

3.5.1 Continuous Class J Design Space

For exploring a continuous mode of the Class J operation, the drain-source voltage waveform can be represented in a *non-crossing-zero* factored expression. Each of the factors in such expression can ever take on a negative value, regardless of the value of θ. Noting that such condition includes a *zero-grazing* double root, Cripps [161] encapsulated this condition by expressing $v_{ds}(\theta)$ as

$$v_{ds}(\theta) = (1 + \alpha \sin\theta) \cdot (1 - \beta \cos\theta) \tag{3.37}$$

This equation represents a continuous Class J family of zero-grazing waveforms, which retain the constant fundamental power, as the parameter α is varied from -1 to $+1$. Fig. 3.9 shows these waveforms, for a single (ideal) value of β. With α equal to zero, this waveform represents the familiar Class B case. The upper limit of α represents the Class J operation whereas the lower limit represents the inverse Class J operation.

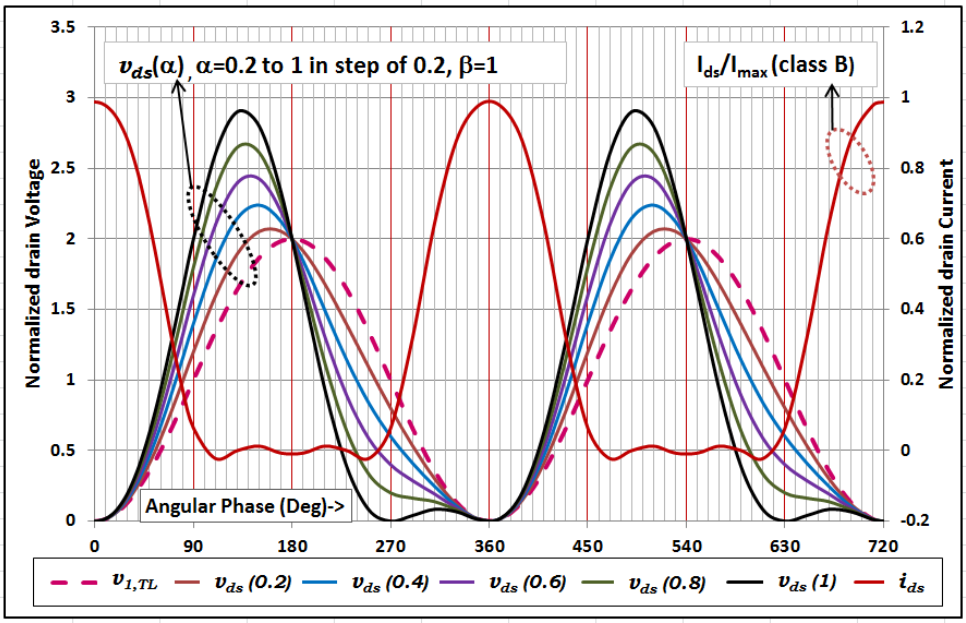


Fig. 3.9: Drain voltage waveform for different values of α and ideal value of β

The value of β is linked with V_k parameter of the transistor. Values of α and β control extrema points of V_{ds}. The peak voltage for each waveform is different and it increases with increasing value of α.The drain current is calculated for 180° of conduction angle. The $v_{1,TL}$ waveform, shown here, is the drain voltage in the Class B with optimum load resistor, giving maximum possible drain voltage excursion. Fig. 3.10 shows similar graph for another value of β (practical LDMOS).

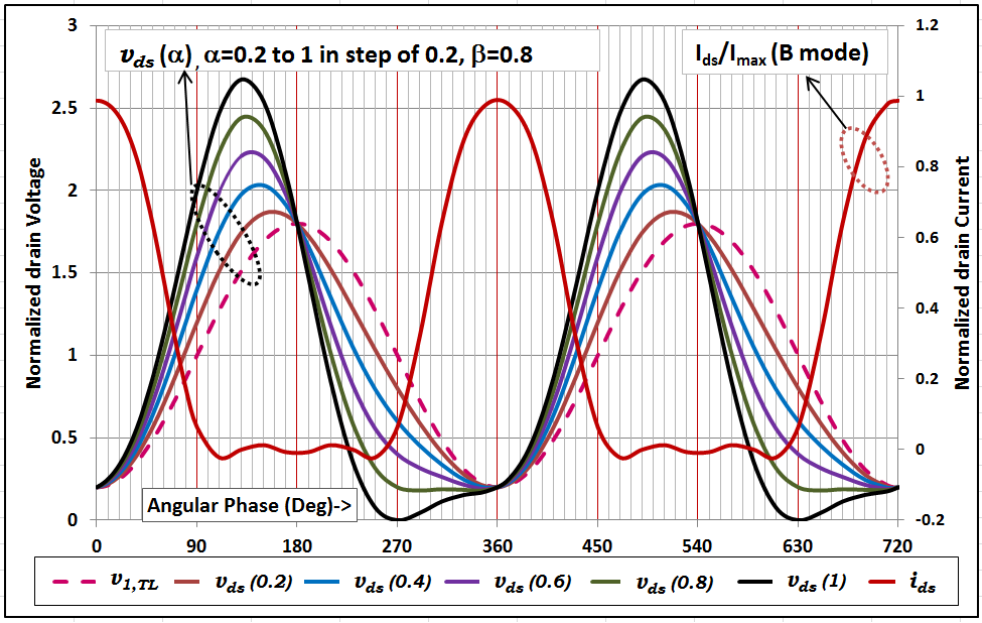


Fig. 3.10: Drain voltage waveform for different values of α and β (both =0.8)

Equation (3.37) can be expanded and rearranged as

$$v_{ds}(\theta) = \left[1 - \sqrt{\alpha^2+\beta^2}\cos\left\{\theta + \tan^{-1}\left(\frac{\alpha}{\beta}\right)\right\} - \frac{\alpha\beta}{2}\cos(2\theta + \pi/2)\right] \qquad (3.38)$$

The design parameters k_2, ψ_1 and ψ_2 are obtained by comparing (3.38) with (3.27) as

$$k_2 = -\frac{\alpha\beta}{2\sqrt{\alpha^2+\beta^2}}, \quad \psi_1 = \tan^{-1}\left(\frac{\alpha}{\beta}\right), \quad \psi_2 = \frac{\pi}{2} \qquad (3.39)$$

$$\delta\chi = \sqrt{\alpha^2+\beta^2} \qquad (3.40)$$

Thus for a given knee voltage and bias supply rating, suitable selection of α and β need to be made so that the resulting V_{ds} has its maximum value less than its maximum rating (V_{max}), and the voltage gain δ also has an acceptable value. Thus continuous Class J design

space is manageable for design, in terms of α and β. For design purpose, δ can also be deduced graphically from the shifted and normalized drain voltage waveform $v_{ds,sn}(\theta)$, for the selected values of α and β. Using (3.14) , $v_{ds,sn}(\theta)$ can be expressed as

$$v_{ds,sn}(\theta) = -\cos(\theta + \psi_1) - k_2 \cdot \cos(2\theta + \psi_2) \tag{3.41}$$

By substituting values from (3.39) in (3.41) a family of $v_{ds,sn}(\theta)$ can be plotted as shown in Fig. 3.11. Here, $v_{1,TL,sn}$ corresponds to the normalized and scaled version of $V_{1,TL}$. Taking the minimum value of $v_{1,TL,sn}$ as a reference, the voltage gain for different waveforms is depicted here. For highlighting this gain, the variation is shown only for a small interval of the angular phase from 180° to 450°.

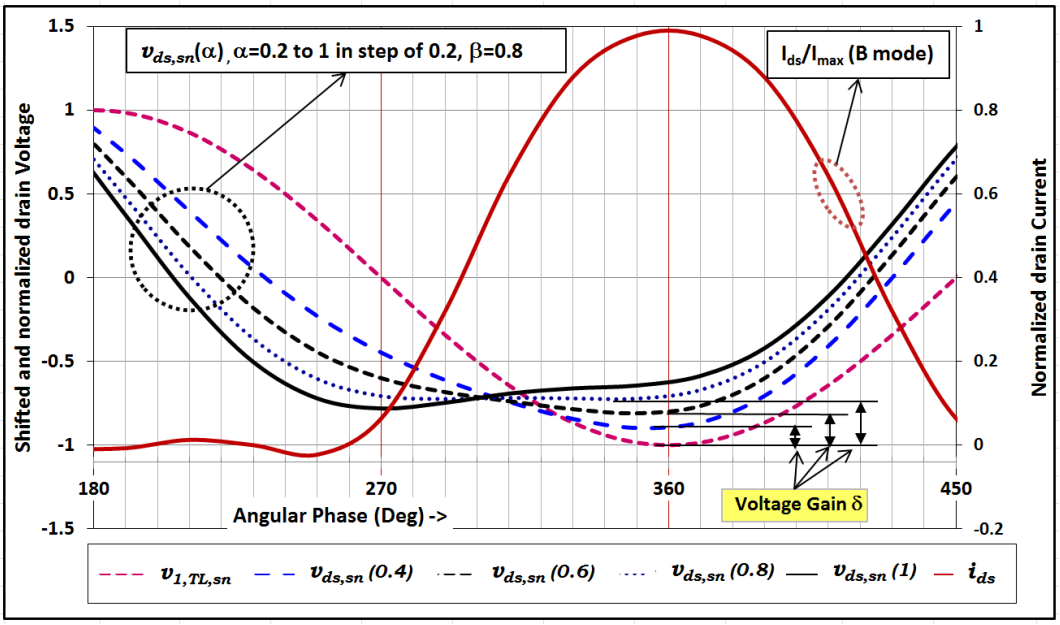


Fig. 3.11: Scaled and normalized drain voltage waveform for different values of α

The selection of α and β depends upon practicalities of the transistor. α has a dominant effect on the overlapping angle of drain current and voltage waveform. β is usually taken as unity for the transistor having zero knee voltage. For a finite knee voltage, β should be reduced below unity. Their relevance becomes clearer during the experimental investigation.

3.5.1.1 Drain Efficiency and Impedance Terminations

By using (3.17) (2.28) and (2.40) the drain efficiency, fundamental termination and second harmonic termination can be expressed with $\varphi_1 = \psi_1$, in terms of α and β, as

$$\eta_{pa,HT} = \delta \cdot \eta_{pa,TL} \cdot \cos(\psi_1) \tag{3.42}$$

$$Z_1 = (\beta + j\alpha) \cdot \frac{V_{DD}}{I_1(\Phi)} \tag{3.43}$$

$$Z_2 = -j\frac{\alpha\beta}{2} \cdot \frac{V_{DD}}{I_2(\Phi)} \tag{3.44}$$

The values of $\eta_{pa,TL}$ and $I_n(\Phi)$ is determined by the selected excitation of I_{ds}. For the Class B mode ($\Phi = 180°$), these terminations are plotted on the Smith chart in Fig. 3.12.

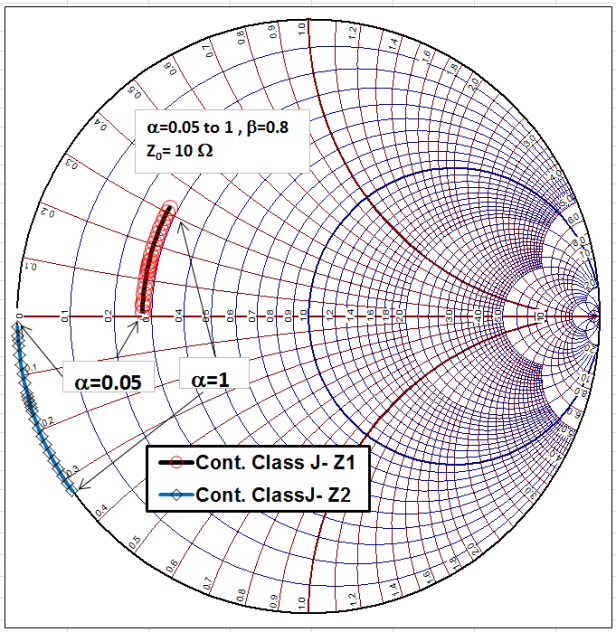


Fig. 3.12: Fundamental and second harmonic terminations for continuous Class J

3.5.2 Continuous and Extended Continuous Class F Design Spaces

The ideal requirement of shorting the second harmonic impedance for classical Class F PA, becomes quite a challenge with UHF power transistors, having good amount of device parasitics. To overcome this difficulty, two possibilities are continuous Class F (CF) and extended continuous Class F (XCF) modes, where flexibly in designing output matching network is provided by a Class F-B/AB mode continuum. Due to an additional freedom,

obtained for a wide range of voltage waveforms (impedance terminations), their efficiency and power can be traded-off for a wide band performance. These modes are studied next.

3.5.2.1 Continuous Class F Design Space

For exploring continuous Class F design space, the drain voltage waveform can be expressed in the factored form, as suggested by Cripps [29], as

$$v_{ds}(\theta) = (1 - \alpha\cos\theta)^2 \cdot (1 + \beta\cos\theta) \cdot (1 - \gamma\sin\theta) \tag{3.45}$$

On expanding this equation and after rearranging in a form similar to the expanded version of (3.11) we get

$$\begin{aligned} v_{ds}(\theta) = \Big[(1 + A_1) + A_2\cos\theta + A_1\cos 2\theta + A_3\cos 3\theta - \frac{\gamma}{2}(2 + A_1)\sin\theta \\ - \frac{\gamma}{2}(A_2 + A_3)\sin 2\theta - \frac{\gamma}{2}A_1\sin 3\theta - \frac{\gamma}{2}A_3\sin 4\theta\Big] \end{aligned} \tag{3.46}$$

Where

$$A_1 = \frac{\alpha^2}{2} - \alpha\beta \tag{3.47}$$

$$A_2 = -2\alpha + \beta + \frac{3}{4}\alpha^2\beta \tag{3.48}$$

$$A_3 = \frac{\alpha^2\beta}{4} \tag{3.49}$$

By comparing these equations with similar cosine and sine terms in the expanded version of (3.11) the design coefficients can be determined in terms of α, β, and γ. Comparison of DC terms yields

$$\beta = \frac{\alpha}{2} \tag{3.50}$$

This condition (3.50) can be applied to simplify (3.48) to (3.49) so that

$$A_1 = 0, \qquad A_2 = \frac{3}{2}\alpha\left(\frac{\alpha^2}{4} - 1\right), \qquad A_3 = \frac{\alpha^3}{8} \tag{3.51}$$

The χ and ψ_1 can be derived as

$$\delta = \frac{1}{\chi}\sqrt{\gamma^2 + A_2^2} \tag{3.52}$$

$$\psi_1 = \tan^{-1}\left(\frac{\gamma}{A_2}\right)$$

Next to this, k_2 and ψ_2 can be evaluated as

$$k_2 = \frac{1}{\delta\chi}\cdot\frac{\alpha\gamma}{4}\left(3-\frac{\alpha^2}{2}\right) \tag{3.53}$$

$$\psi_2 = \tan^{-1}\left(\frac{\pi}{2}\right)$$

The value of ψ_2 implies that the second harmonic termination for $\beta = \frac{\alpha}{2}$ is imaginary. Finally, the coefficient k_4 can be deduced as

$$k_4 = -\frac{1}{\delta\chi}\cdot\frac{\alpha^3}{16}\gamma \tag{3.54}$$

The optimum value of α, obtained by differentiating (3.52) with respect to α, is

$$\alpha = \frac{2}{\sqrt{3}} \tag{3.55}$$

Substituting the values of α and β from Eqns. (3.55) and (3.50) in (3.45) we get

$$v_{ds}(\theta) = \left(1-\frac{2}{\sqrt{3}}\cos\theta\right)^2.\left(1+\frac{1}{\sqrt{3}}\cos\theta\right).(1-\gamma\sin\theta) \tag{3.56}$$

This equation represents Continuous Class F mode. By keeping the parameters α and β constant and changing only γ $(-1 \le \gamma \le 1)$ results in such PA operation. The equation (3.56) resembles (3.24) derived in the section 3.3, except the augmentation of the factor $(1-\gamma\sin\theta)$. The fundamental termination and harmonic terminations [70], required for Class B excitation of current, are shown in Fig. 3.13 with optimum value of α and β $(=\frac{\alpha}{2})$ and with value of γ, changing from -1 to 1. The second harmonic reactance varies along the edge of Smith chart, while the fundamental impedance moves on a circle of constant resistance. Only resistive termination exists at the third harmonic. This situation is in close requirement with the Class F case, where infinite third harmonic impedance is desired. This set of realizable terminations present a better design space to the designer. The important aspect is that one need not to provide an ideal short circuit for the second harmonic. For few specific values of γ, IV waveforms are plotted in Fig. 3.14.

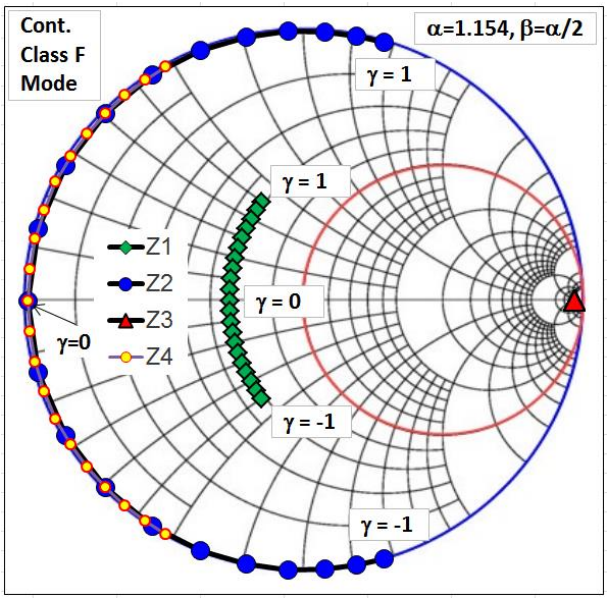


Fig. 3.13: Impedance plot on Smith chart for different value of γ

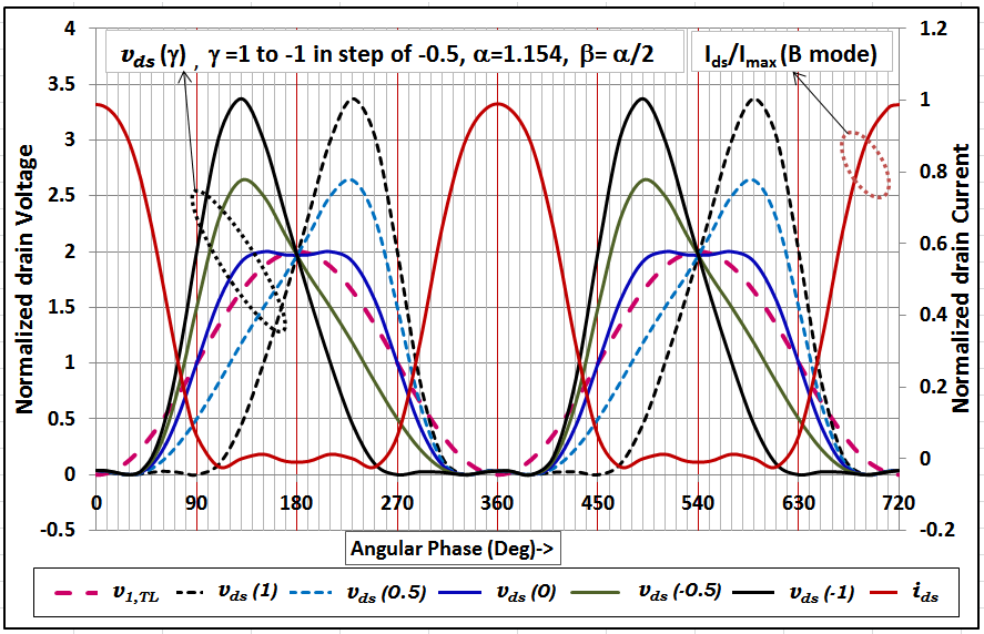


Fig. 3.14: Drain voltage and current waveforms for continuous Class F design space

Here $v_{ds}(\gamma = 0)$ waveform corresponds to normal Class F operation. The variation in γ controls the phase shift between voltage and current. An increase in magnitude of this parameter, increases peak value of drain voltage also. For all values of γ, the new voltage waveforms still maintains the class F power and efficiency performance but have significantly modified waveforms. The price, one needs to pay, for this modified continuous mode design, is in the form of excessive drain-source voltage (Fig. 3.14), often exceeding the

maximum rating of the transistor. For bringing down this limit, this mode can be further extended, as investigated next.

3.5.2.2 Extended Continuous Class F Design Space

In the CF operation, α and β were constant and design space was explored in terms of γ only. In general, α or β can also be varied, to get an additional degree of freedom, for the PA design. Such variations result in extended continuous Class F [148] or XCF design space. Compared to the CF, this mode provides an additional flexibility which can be used to maintain acceptable fundamental power and DC to RF conversion efficiency, without crossing the voltage breakdown limit of the transistor. Hence, this mode of operation seems suitable for high power PA designs with UHF power transistors. Obviously, the efficiency will be lower than the maximum value obtained in the CF mode. The XCF design can be performed by selecting suitable values of $\alpha,\ \beta,$ and γ.

For keeping DC bias at V_{DD}, the parameters α and β are coupled by (3.50) . Hence, the design space for this mode can be explored in terms of α and γ. For $\gamma = 0$. the drain voltage waveforms, from (3.45) , are shown in Fig. 3.15.

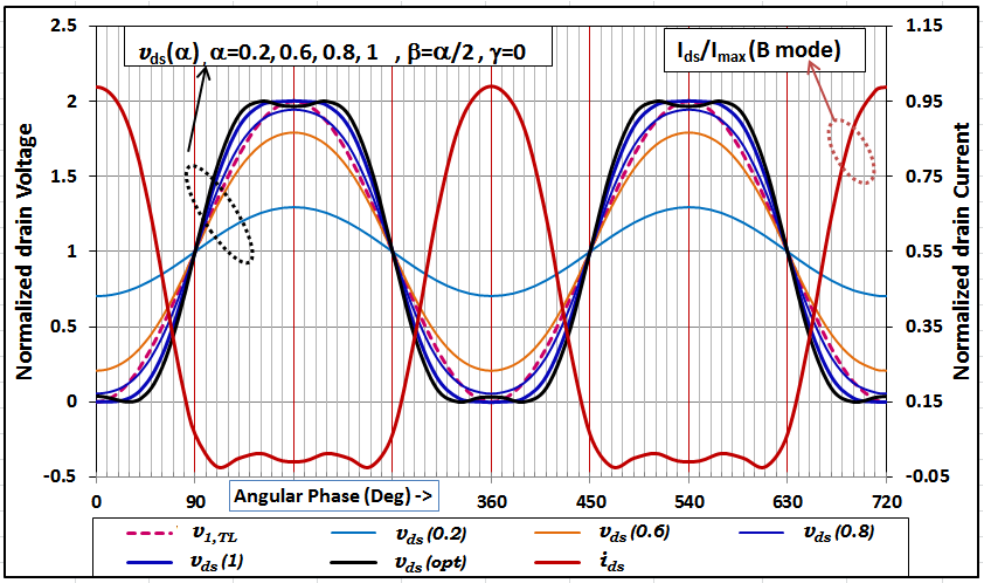


Fig. 3.15: Normalized drain voltage waveform for different values of α

The variation in α controls the maxima and minima of the drain voltage. For variation in both α and γ, the drain voltage is plotted with Class B current, for selected values, in Fig. 3.16. As seen here, γ manages the phase shift between voltage and current. It can be seen that with the selected values of α and γ, the peak voltage at the drain terminal can be controlled within desired limit.

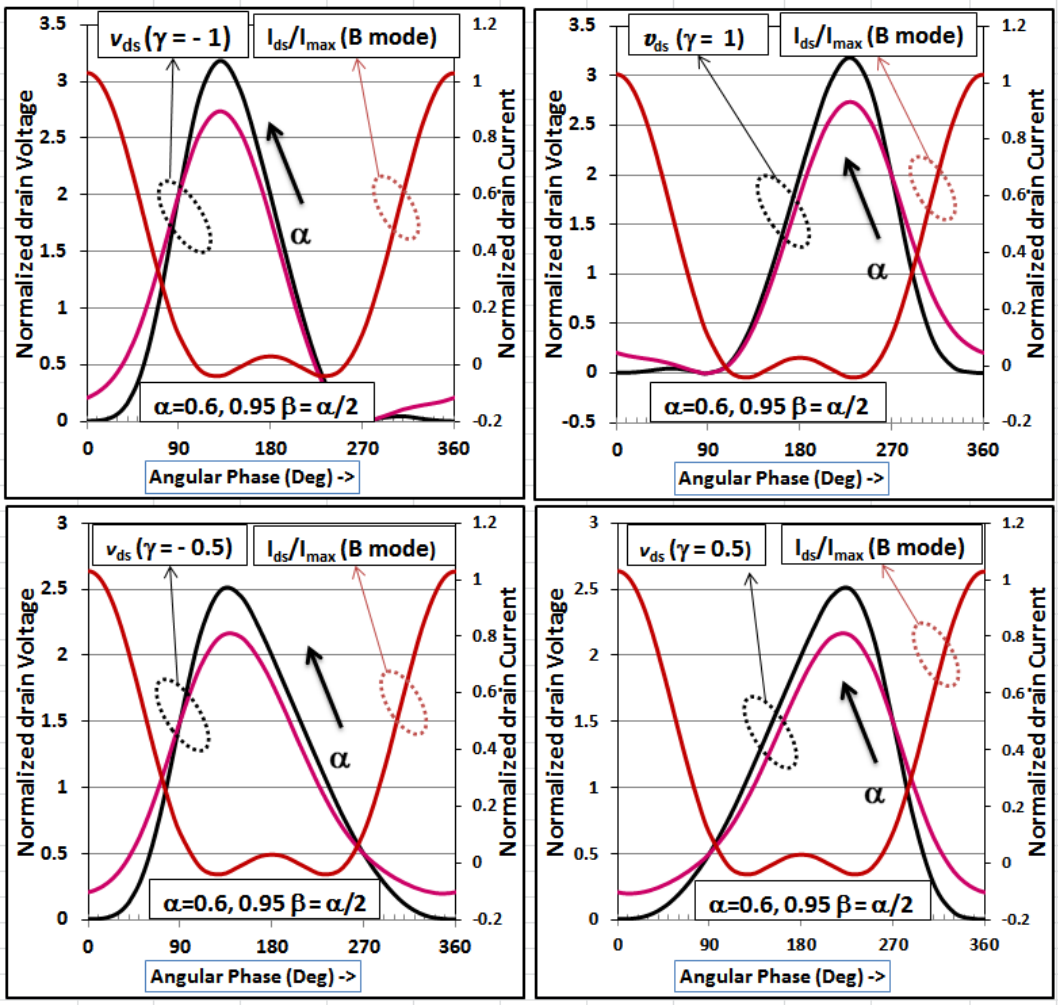


Fig. 3.16: Different drain voltage waveform for extended continuous Class F space

The advantage of varying α as well as γ can be seen here. For example the peak value of the waveform in Fig. 3.14, for $\gamma = 0.5$, is between 2.5 and 3. In present plot this peak limit has come down to nearly 2.5 for $\alpha = 0.95$. Being a function of the design parameters, the DC to RF efficiency is plotted as a function of α, as shown in Fig. 3.17. This is not dependant on γ. Its maximum value, as evident, results for CF mode with $\alpha = 1.154$.

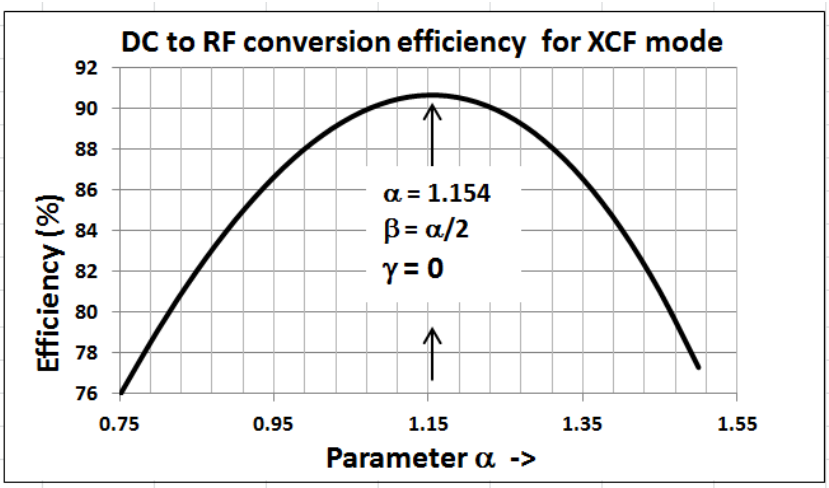


Fig. 3.17: DC to RF conversion efficiency as a function of α

In this XCF mode, in order to avoid negative value of drain voltage waveforms, the value of α and γ should be varied in the following range.

$$-2 \leq \alpha \leq 2 \quad \alpha \neq 0 \tag{3.57}$$

$$-1 \leq \gamma \leq 1 \tag{3.58}$$

For design purpose, depending upon the admissible drain voltage rating of the transistor, a particular set of α and γ can be selected. For the general case, including all three design space parameters, different terminations for XCF mode can be derived, by using (2.28) and (2.40) as

$$Z_1 = \left[\left(2\alpha - \beta - \frac{3\alpha^2\beta}{4}\right) - j\gamma\left(\frac{\alpha\beta}{2} - 1 - \frac{\alpha^2}{4}\right)\right] \cdot \frac{V_{DD}}{I_1(\Phi)} \tag{3.59}$$

$$Z_2 = \left[\left(\alpha\beta - \frac{\alpha^2}{2}\right) + j\gamma\left(\alpha - \frac{\beta}{2} - \frac{\alpha^2\beta}{4}\right)\right] \cdot \frac{V_{DD}}{I_2(\Phi)} \tag{3.60}$$

$$Z_3 = -\left[\left(\frac{\alpha^2\beta}{4}\right) + j\gamma\left(\frac{\alpha^2}{4} - \frac{\alpha\beta}{2}\right)\right] \cdot \frac{V_{DD}}{I_3(\Phi)} \tag{3.61}$$

$$Z_4 = j\gamma\left(\frac{\alpha^2\beta}{8}\right) \cdot \frac{V_{DD}}{I_4(\Phi)} \tag{3.62}$$

It is clear that pure the Class B mode for I_{ds} excitation is not sufficient in order to make a presence of Z_3. Hence, the Class AB mode is useful, capable of generating the third harmonic

current $I_3(\Phi)$. The nonlinear output capacitor also helps producing this third harmonic component of the current. The fundamental power in this mode is given by

$$P_1 = \left(\alpha - \frac{\beta}{2} - \frac{3\alpha^2\beta}{8}\right) \cdot V_{DD} I_1(\Phi) \tag{3.63}$$

In this case it is better to study the functional effects of three design parameters *viz*. $\alpha,\ \beta,$ and γ on voltage gain by graphical results. There may be many solutions that guarantee high output power and efficiency. This design space for high power amplifiers can provide more flexibility for selecting an output matching network so that the resulting device stress for voltage and current can be kept within the safe limit.

3.5.3 Class J Design Space with Third Harmonic

The third harmonic, which is not taken into consideration in the Class J mode, may be present in the output matching network due to the practical circuit realisation and the inability of the output capacitor to short this harmonic perfectly. It may affect the output power and efficiency. For the design analysis, voltage waveforms of the Class J family with third harmonic (will be referred to as J3 now onwards) can be expressed as

$$v_{ds}(\theta) = 1 - \delta\chi \cdot [\cos(\theta + \psi_1) + k_2 \cos(2\theta + \psi_2) + k_3 \cos(3\theta + \psi_3)] \tag{3.64}$$

As earlier detailed, the design procedure include calculation of δ as a function of the parameters k_2, k_3, ψ_2 and ψ_3; subject to constraints on drain voltage excursion dictated by device physical limits. In general this calculation of voltage gain function δ involves rigorous numerical analysis. However, by using factorization, for drain voltage waveform $V_{ds}(\theta)$ it can be simplified. For the Class J3 design family this waveform is represented by

$$v_{ds}(\theta) = (1 - \beta\cos\theta).(1 - \alpha \sin n\theta) \quad \text{for} \quad -1 < \alpha < 1 \tag{3.65}$$

Here n is any positive integer, deciding the degree of complexity. This represents a wider continuum of PA modes, having the same power and efficiency as the Class B, but with reactive, rather than short circuited, harmonics. For $n = 2$, the voltage waveform is

$$v_{ds}(\theta) = (1 - \beta\cos\theta).(1 - \alpha\sin 2\theta) \tag{3.66}$$

This can be expanded into

$$v_{ds}(\theta) = \left(1 - \beta\cos\theta + \frac{\alpha\beta}{2}\sin\theta - \alpha\sin 2\theta + \frac{\alpha\beta}{2}\sin 3\theta\right) \tag{3.67}$$

This set of waveforms demonstrates that optimum Class B like performance can be obtained over a wide range of harmonic terminations, representing an important paradigm shift in the design of PA. A family of drain waveforms, generated from (3.67) for different values of parameter α, is shown in Fig. 3.18. The drain current (at $\Phi = 200°$) is normalized with respect to maximum drain current I_{max}), as before. The selection of α and β depends upon practicalities of the device. The first parameter α has a dominant effect on the overlapping angle of drain current and voltage waveform.

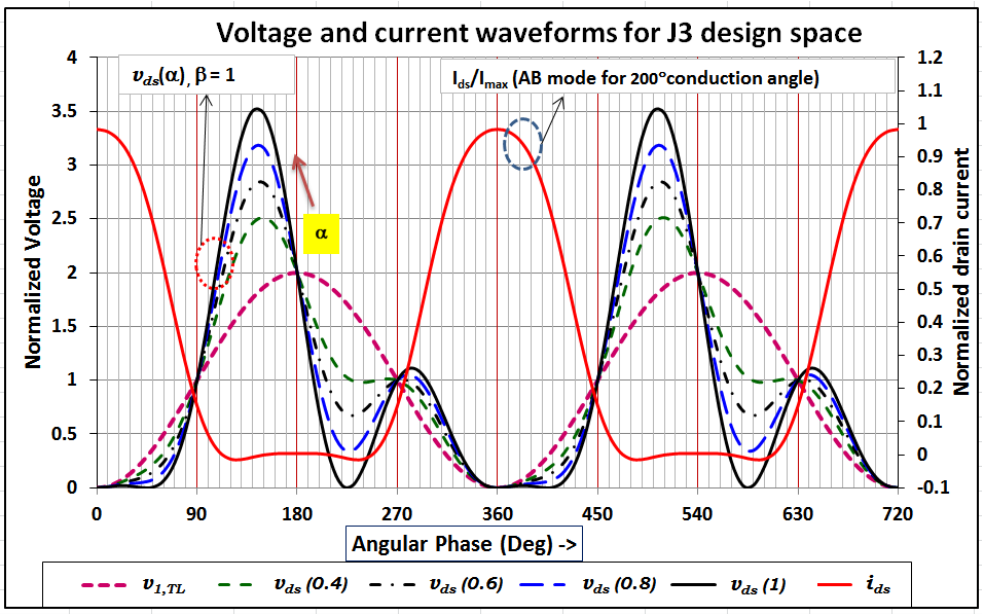


Fig. 3.18: Simulated J3 design space showing drain voltage and current waveforms

Comparing (3.64) and (3.67) following relations can be derived.

$$k_2 = -\frac{2\alpha}{\beta\sqrt{4+\alpha^2}} \qquad k_3 = \frac{\alpha}{\sqrt{4+\alpha^2}} \tag{3.68}$$

$$\psi_1 = \tan^{-1}\left(\frac{\alpha}{2}\right) \qquad \psi_2 = \psi_3 \equiv \frac{\pi}{2} \tag{3.69}$$

The voltage gain can be expressed in terms of α and β as

$$\delta = \frac{\beta}{2\chi}\sqrt{4+\alpha^2} \tag{3.70}$$

Next to this, the fundamental, second and third harmonic terminations required for design can be expressed as

$$Z_1 = -\frac{\beta}{2}\sqrt{4+\alpha^2}\cdot\frac{V_{DD}}{I_1(\Phi)}\cdot(2+j\alpha) \tag{3.71}$$

$$Z_2 = -j\alpha\cdot\frac{V_{DD}}{I_2(\Phi)}$$

$$Z_3 = j\frac{\alpha\beta}{2}\cdot\frac{V_{DD}}{I_3(\Phi)}$$

Here drain current components $I_1(\Phi), I_2(\Phi)$ and $I_3(\Phi)$ are obtained from Fourier expansion of the reduced conduction current as a function of current conduction angle (Φ).

3.5.4 Continuous Inverse Class F mode

Most of the classical modes and HT modes can be inverted [169], which means that the current and voltage waveforms can be reversed. For example, an inverted Class B mode consists of a transistor having a sinusoidal current waveform and a half-wave rectified voltage waveform. In the ideal case, the power and efficiency would be the same at the peak power level, but the power back-off efficiency characteristic would replicate the Class A curve, and as such this mode is not much used. A more interesting case is the inverted Class F mode, which has received considerable attention [170] in the literature over the last few years for low power mobile handset PAs. The invers Class F PA require a square current waveform and a half wave rectified sinusoidal waveform at the device intrinsic current generator plane. In line with the Class F results, this waveform shaping is achieved by offering the fundamental impedance, an open circuit second harmonic impedance and a short circuit third harmonic termination. For such case, the current and voltage waveforms are

$$V_{ds}(\theta) = V_{DD}\left(\frac{1}{\sqrt{2}} + \cos\theta\right)^2 = \left(1 + \sqrt{2}\cos\theta + \frac{1}{2}\cos 2\theta\right) \tag{3.72}$$

$$I_{ds}(\theta) = I_{DC} - I_1\cos\theta - I_3\cos 3\theta \tag{3.73}$$

The resulting waveforms (Fig. 3.19) show one useful potential advantage. Due to the fact that the DC component of the half-wave rectified voltage sine-wave has a value of V_{pk}/π, the fundamental component can be increased by a factor of $\pi/2$, assuming that the peak voltage of πV_{DD} can be safely accommodated. This corresponds to a potential increase of fundamental power nearly 2 dB in comparison to a Class F configuration, and about a 2.5 dB increase in comparison to a Class B PA using the same transistor at the same supply voltage.

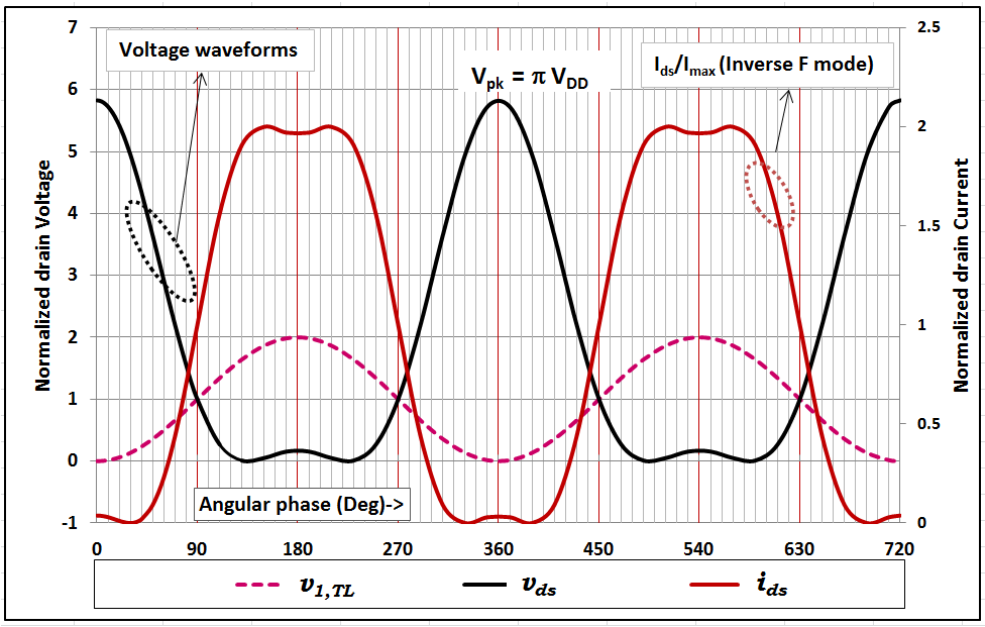


Fig. 3.19: Drain voltage and current waveforms for F^{-1} Class

In practice, however, this extra peak voltage, which is much higher than earlier discussed continuous modes, may exceed the breakdown specification of the device. Recent studies [71] have shown that continuous design space can also be explored for inverse Class F mode in line with continuous Class F mode. For such case, modified drain current waveform becomes

$$I_{ds}(\theta) = (I_{DC} - I_1\cos\theta - I_3\cos 3\theta)(1 + \alpha\cos\theta).(1 - \gamma\sin\theta) \tag{3.74}$$

The parameter α and γ, as earlier, are parametric coefficient useful for exploring the design space. From above equation two cases can be readily identified. The first one corresponds to α equal to zero. For this case, the second coefficient should be in the range of -1 to 1, in order to maintain the current waveforms for *zero grazing*. The second case is general case with nonzero α and γ. For such case Carruba [71] has suggested a new mathematical formulation using a resistive second harmonic load. In order to maintain a positive value of this impedance, α should be between 0 and 1. This load is either a short circuit or an open circuit for commonly used operating modes. The corresponding waveforms are still difficult to realize in practice in view of large rating required for the drain-source voltage. Compared to the Class F mode, this inverse F mode is superior for low power handset PAs due to its larger fundamental drain voltage. For such PAs, devices are available with relatively high breakdown voltage due to a low value of drain supply V_{DD} used. However, in power devices this rating is hardly 2.5 times V_{DD} against the required 5-6 times in inverse Class F mode. Addition of α and γ further increase this requirement up to 12 times of V_{DD}. Further in this mode, current clipping is realized by over-driving the device so that it saturates on the peaks and cuts off in the dips. This mode of operation, in practice, requires additional treatment of harmonics along with necessary waveforms. Hence, this mode is not suitable for power devices and not discussed in detail here.

3.6 Experimental Investigation of Harmonic Tuned Amplifier

In order to verify the theoretical analysis carried out in previous sections, three PAs were designed and experimentally tested for various figures of merit. The amplifiers, delivering RF power below 500 W (CW), were designed, as described in the previous chapter. For investigating the design improvement achieved with the harmonic tuning, the present target line for RF power was set as above 500 W. The first harmonic tuned PA module was designed with the continuous Class J mode at 505.8 MHz with its output power up to 550 W. The second

PA was designed using the manipulation of the second as well as third harmonic, to provide 700 W at 505.8 MHz. The third amplifier was designed at 650 MHz using extended continuous Class F operation, to deliver 600 W. These frequencies of operation were useful for the particle accelerator projects of the institute. As per our knowledge, this type of design for power transistors has not been reported in the literature. Most of the HT designs for PA at different power and frequency, reported therein, are aimed for cellular phones and base stations, requiring an average RF power of less than 100 W.

3.6.1 Continuous Class J Mode Power Amplifier

For the continuous Class-J based PA design, BLF 573 LDMOS was selected on the basis of the load-line calculation [73] and preliminary simulation studies, carried out in Microwave Office™. It is an LDMOS transistor for broadcast, industrial, scientific and medical applications in 30 to 500 MHz band. As per the data sheet, its typical CW performance at 225 MHz include an average output power of 300 W with a power gain of 27.2 dB and a drain efficiency of 70%; all at a supply voltage of 50 V and a bias current of 900 mA. Hence, in order to achieve the power of 500 W and above, from a single PA, two such transistors were power combined in a single PA with the help of on-board Wilkinson divider and combiner. With suitable simulation study, carried out for the large signal gain roll-off, a power of 550W at 505.8 MHz was fixed as the target goal. For each half of the PA, DC IV characteristics (Fig. 2.40) for different gate bias voltages, were generated using Microwave office™ by using the nonlinear MET model of BLF 573, provided by the vendor. It can be seen here that the knee voltage is nearly 7 V ($\chi = 0.86$) at I_{max} of nearly 26.7 A and V_{DD} of 50 V. Such appreciable value of V_k reduces drain efficiency, for the Class B, from 78.5% to 67.51%. Hence, after accounting for the power losses due to passive lumped components, the target efficiency for the present design was set at 67%.

With these preliminary studies, important design specifications of this PA were fixed as listed in Table 3.2. The selected frequency of operation was useful for making it as a work-horse in a 50 kW SSPA system, described in the chapter 6.

Table 3.2: Technical specification of 550 W RF power amplifier module

Sr.	**Parameter**	**Value**
1	RF Power Output/ Power Gain	550 W CW/ 18 dB
2	Operating frequency and 1-dB bandwidth	505.8 MHz, ± 5 MHz
3	Operating mode/ DC-RF efficiency	Continuous Class J / 67%
5	Harmonic distortion/ Spurious output	-30 dBc / -35 dBc
6	PA Cooling / Drain bias supply	Water cooled / 50 V (DC)

As per the data sheet, the peak voltage at drain terminal for this transistor cannot exceed beyond 110 V. Thus values of α and β need to be calculated, for other than the Class J mode, so as to keep the maximum drain voltage V_{max} below 2.2 times that of the drain supply of 50 V (DC). Table 3.3 gives different calculated parameters (voltage gain function δ, upper and lower limits of the drain voltage), calculated for $\chi = 0.86$ ($V_k = 7\ V$) and different values of α and β, using the analysis presented in 3.5.1.

Table 3.3: Calculated voltage gain, maximum and minimum drain voltages

Sr.	**Parameter α**	**Parameterβ**	**Voltage Gain δ**	**V_{max} (V)**	**V_{min} (V)**
1	0.20	0.80	0.96	93.1	10.0
2	0.30	0.80	0.99	97.3	10.0
3	0.40	0.80	1.04	101.6	9.9
4	0.50	0.80	1.16	105.8	9.7
5	0.50	0.86	1.16	109.0	7.0
6	0.60	0.80	1.16	110.5	9.5
7	0.70	0.80	1.24	116.3	9.3
8	0.80	0.80	1.32	122.1	9.0

The design set, comprising of $\alpha = 0.5$ and $\beta = 0.86$, fulfils the PA requirement with a normalised peak drain voltage of 2.18 (V_{max} =109 V). The value of β equal to 0.86 was found by graphical iterative calculations. For this design set, the phase shift in the fundamental components of drain voltage and current is 30.17°, instead of 45° required in the Class J

operation. Using (3.43) and (3.44) Z_1 and Z_2 were calculated and the first order topology for the impedance matching network (IMN) and output matching network (OMN) were designed for single transistor. During the course of the simulation open stubs were replaced with chip capacitors. Including the package effect and nonlinear capacitor effect, IMN and OMN were improved for this PA (Fig. 3.20).

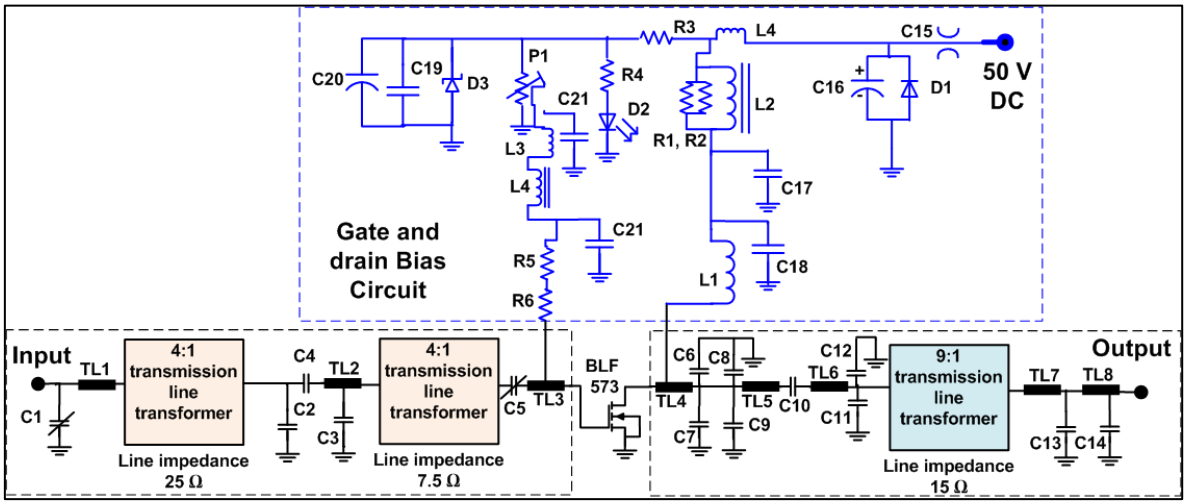


Fig. 3.20: Impedance matching circuit for one half of the 550 W amplifier

The nonlinear output capacitor (C_{out}) was estimated by following relation

$$C_{out}(V_{ds}) = 50.[1.9 + 1212\{1 + \tanh(-0.0465V_{ds} - 2.7)\}]\ (pF) \qquad (3.75)$$

In harmonic matching part of OMN, the Class J requirement was fulfilled with the help of microstrip transmission line (TL4, TL5) and combination of chip capacitors (C6-C10). Also the impedance plane at the fundamental frequency was transformed to the system impedance of 50 Ω with the help of a 9:1 semi-rigid transmission line transformer and chip capacitors, (C13, C14). For IMN, a combination of two 4:1 transformers was used for impedance conversion. Fig. 3.21 shows the complete PA with Wilkinson divider, combiner, IMN and OMN, the last two as sub-circuits. The harmonic balance power analysis and simulation was performed under desired source/load impedances to fine tune the PA circuit. The simulated voltage and current waveforms, for one half of the PA, are shown in Fig. 3.22.

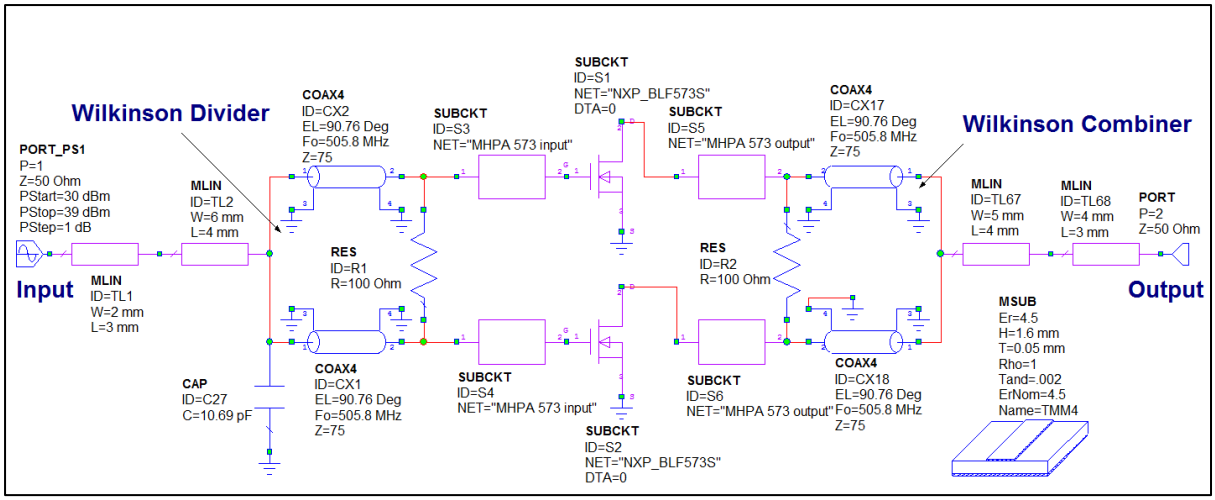


Fig. 3.21: Complete impedance matching circuit for 550 W PA

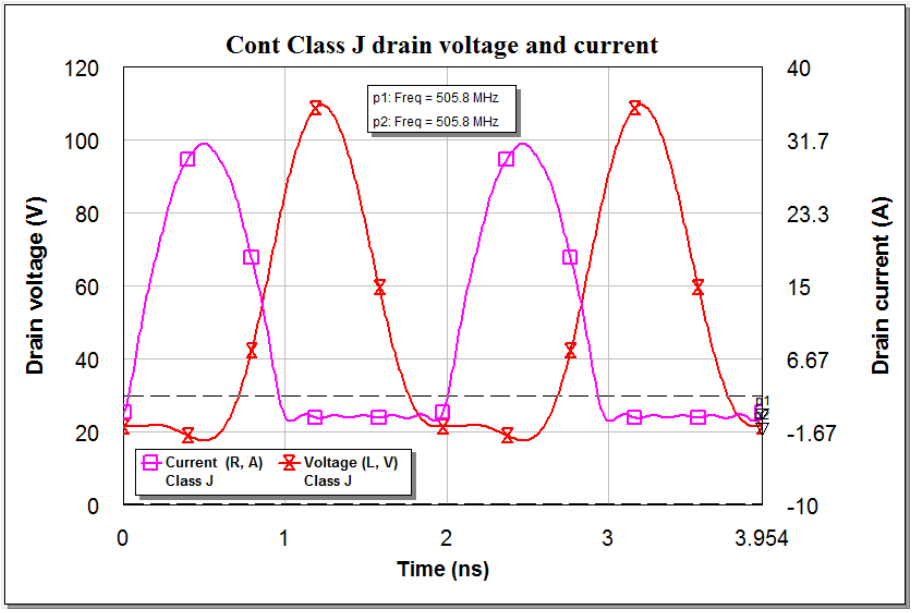
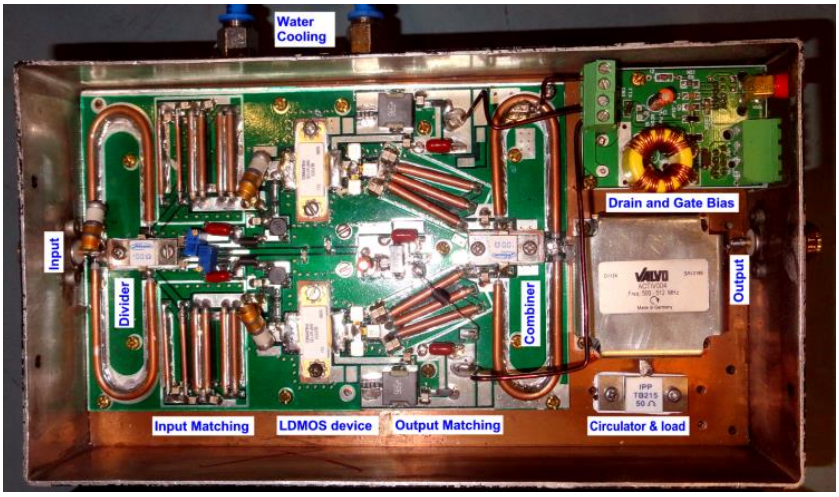


Fig. 3.22: Simulated drain voltage and current for one half of the 550 W amplifier

The PA circuit layout was generated and printed on an RF substrate (TMM4™) with the relative permittivity of 4.5 and a thickness of 1.6 mm. It consists of Wilkinson divider and combiner using semi-rigid coaxial lines from Micro-coax. A 700 W circulator (with insertion loss of 0.2 dB), placed before the final output, protect the RF devices from reflected power. The fabricated amplifier board (Fig. 3.23) was mounted directly on a water-cooled copper plate.



Brief Details

Length, Width: 24 cm, 14 cm

Outer Height: 4 cm

Substrate Type: TMM4™

Input Connector: N type

Output Connector: N type

DC Bias: 50 V

Cooling: Water cooled

Fig. 3.23: Fabricated 550 W amplifier

3.6.1.1 Measured Results

The designed PA was fully characterized on an RF test bench including RF instruments and data acquisition controller. The RF measurement, performed earlier for the tuned load PAs, was carried out using various RF instruments, operated manually. It was time consuming job and affects accuracy due to error involved in manual calibration setup of different instruments. Hence for high power RF characterization, an automated RF test bench [171] was setup. This bench encompasses measuring instruments including signal generator, driver amplifier, power meter, DC power supply, spectrum analyser and dummy load. As shown in Fig. 3.24, the RF power level from signal generator is supplied to the device under test (DUT) through a driver amplifier. Fig. 3.25 shows the actual test bench.

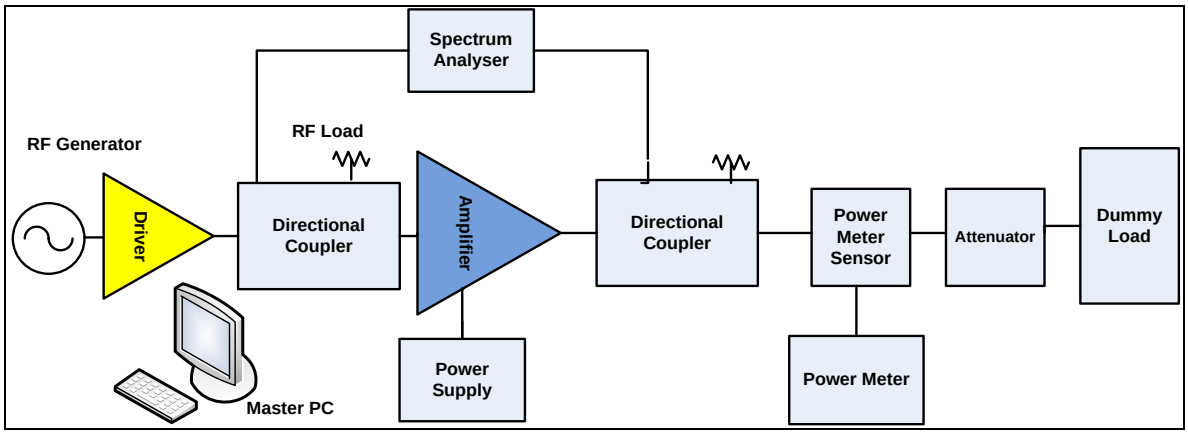


Fig. 3.24: Test setup for power gain and intermodulation measurement

Fig. 3.25: Automated test bench with RF instruments and data acquisition controller

The incident and the transmitted signals are sampled with the help of directional couplers. All of these instruments act as slaves to a master computer. This computer with the help of a data acquisition card, communicates with the instruments, using different protocols like serial (RS232 and USB), GPIB and TCP/IP. A human machine graphic interface application, developed in LabVIEW™, performs different measurements like swept power transfer characteristics, linearity and spectral response of DUT. The measurement data is displayed as a graphic user friendly (GUI) screen on the computer. A snapshot captured from this test bench for designed PA (DUT) is shown in Fig. 3.26. It can be seen that at 546.5 W of the output power efficiency is 66%. The RF power gain and the input VSWR are 18.4 dB and 1.13 respectively. In addition to this single point testing, the swept power parameters, measured using this test bench, are shown in Fig. 3.27. The power transfer characteristic with a CW signal excitation is linear; however the drain efficiency (66%), de-embedded so as to exclude circulator's insertion loss, is slightly lower than calculated value. This may be due to the associated circuit losses of the RF components used here. The PAE is nearly similar to the

drain efficiency at 18 dB of gain. The saturated power is in excess of 550W. The transducer power gain is nearly constant and more than 18 dB for nearly the entire operational regime of input power. The measurement of output power was performed up to 574 W with a measured gain of 17.8 dB. The exact measurement up to P_{1dB} point could not be performed due to possible damage of the PA. This point must be above 600 W of output power. For insertion phase measurement, a vector network analyser was used as shown in Fig. 3.28.

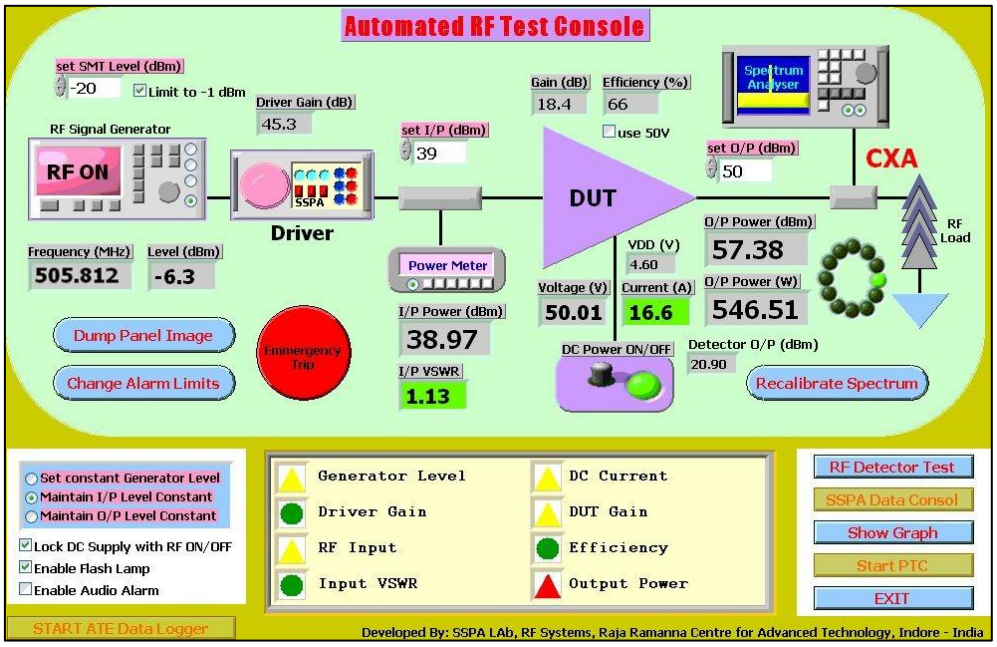


Fig. 3.26: Measurement data at 505.8 MHz for 550 W PA at full output RF power

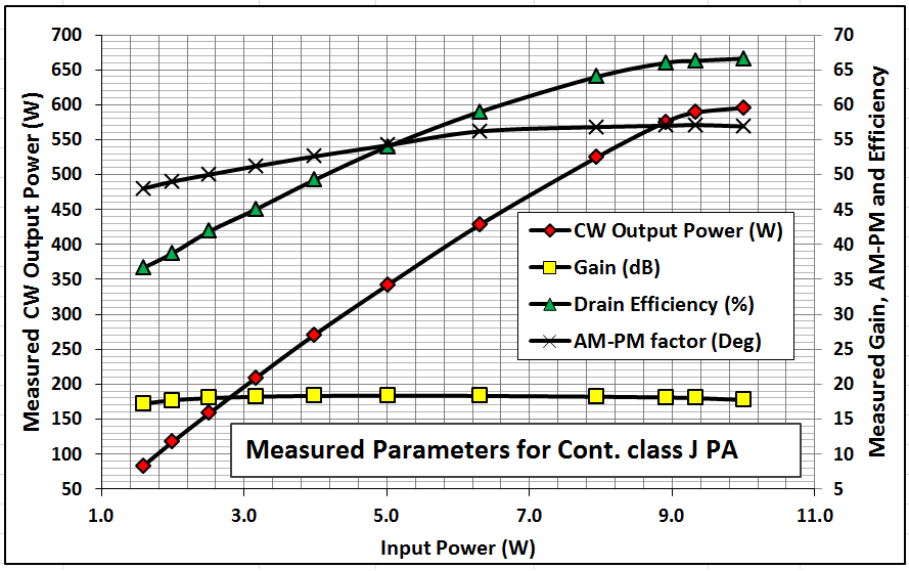


Fig. 3.27: Measured RF performance of 550 W PA module

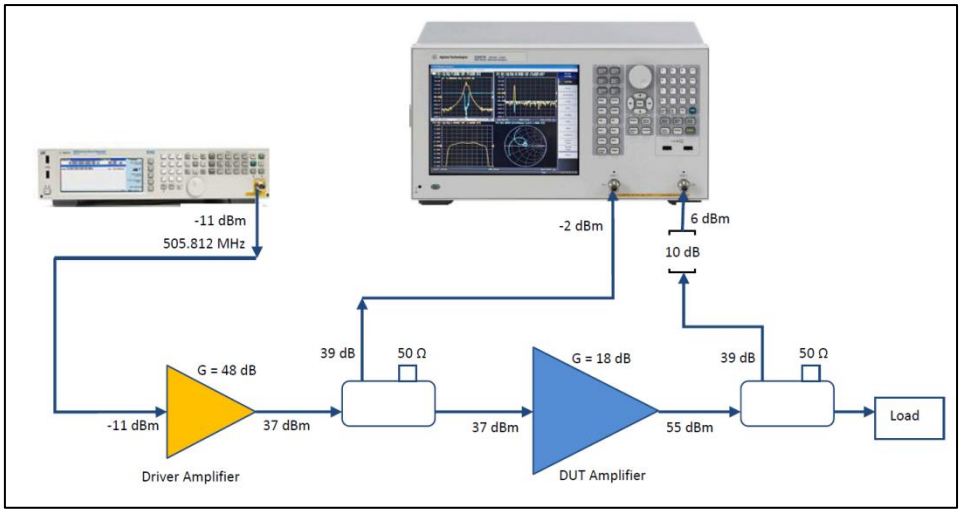


Fig. 3.28: Test setup for insertion phase measurement

The insertion phase measurement setup, with estimated power budget (coupling of directional coupler, power from different blocks), is also shown here. The measured insertion phase spread of this module was less than 12° for entire power sweep. From this data, AM to PM conversion was measured as nearly 2°/dB, centred at an input power of 38 dBm. The measured 1-dB bandwidth for this PA was 10 MHz. Fig. 3.29 shows the measured spectrum of the designed PA, driven with a CW signal, at the centre frequency of 505.8 MHz. The second harmonic component, is 35.78 dB below the fundamental signal at 57 dBm.

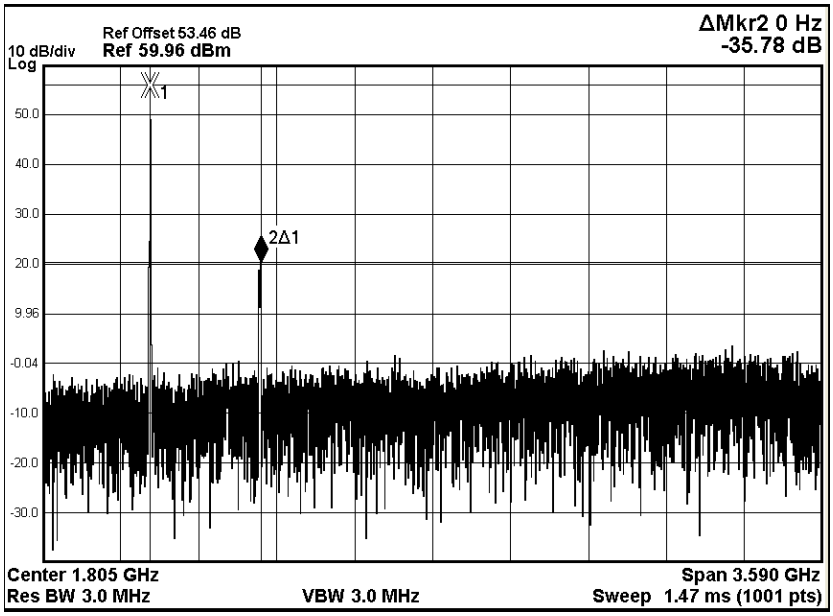


Fig. 3.29: Measured single tone spectral response of 550 W PA at full power

All other harmonics and spurious components were lower than the fundamental by more than 55 dB. The Class J is usually used for broadband applications. However the particle accelerator, for which this PA has been designed, does not require the RF amplifiers with bandwidth more than 5 MHz around centre frequency. Hence, this design was focused for optimising the output power and drain efficiency, instead of bandwidth enhancement.

Since the output power of this PA is quite high, large signal operation was studied with the help of X parameter™ [117] measurement of this PA. These parameters are based on the Poly-Harmonic Distortion (PHD) approach [172]. The X parameters are discussed in Appendix C. For nonlinear X parameters' measurement [173] PNA-X instrument from Agilent technology was used. Fig. 3.30 shows measured large signal output reflection coefficient. A measurement was performed at fundamental tone (A_{11}) and the first harmonic. Large signal output reflection coefficient $X_{22,11}^{(S)}$ and $X_{22,11}^{(T)}$ provide description of large signal output match, sometimes referred to as hot s_{22}. The classic hot s_{22} approache ignore the existence of $X_{22,11}^{(T)}$. As seen in this figure, for small as well large input amplitude, the output match is pretty good. $X_{22,11}^{(T)}$ is appreciable only for large-signal (nonlinear) operating conditions.

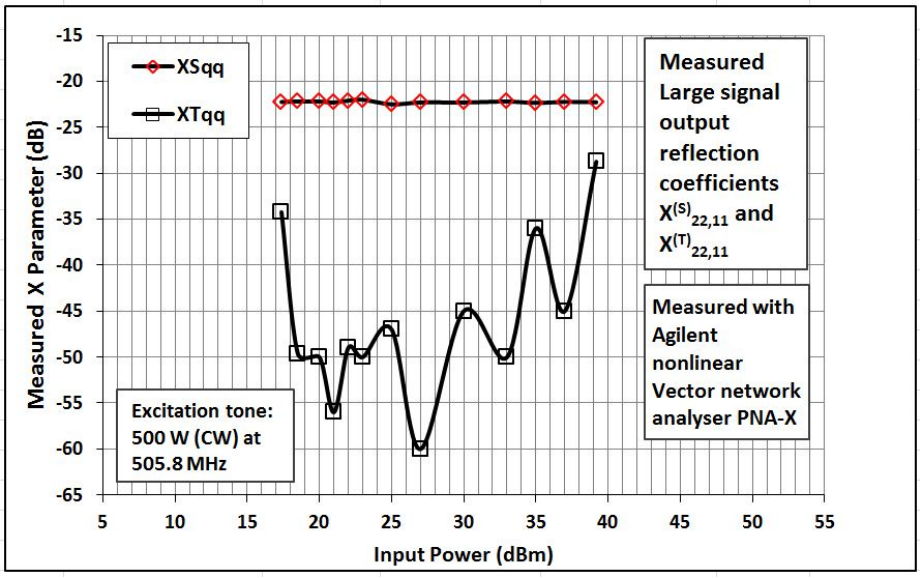


Fig. 3.30: X parameter response measured at 500 W of RF power

3.6.2 Continuous Class J Mode Amplifier with Third Harmonic

To verify the design technique discussed in the section 3.5.2, an RF amplifier, operating in Class J with the inclusion of the third harmonic, was designed and experimentally tested. In due course of the time, more powerful push-pull RF transistors like BLF 578, MRFE6VP41KH, MRFE6VP61K25H and BLF 888 were available in the market. Hence, unlike previous design with two separate single ended transistors, a push-pull device was used for the present design.

The technical parameters of the PA, to be designed, include a power gain of 18 dB, a bandwidth of 5 MHz and its spurious response below 30 dB from the fundamental signal. It needs to operate at the centre frequency of 505.8 MHz with a maximum output power of 700 W (CW) using a 48 V (DC) drain supply. The bias supply was lowered from the normal 50 V for accommodating high peak value of drain voltage in J3 design space. Based on the results of circuit simulation studies and transistors' data sheet, an LDMOS MRFE6VP61K25H, from Freescale semiconductor, was selected for this design. Being a push pull device, it can be used for obtaining a pulse power of 1000 W with efficiency of 58% at 500 MHz. Due to the CW power required in the present design, maximum deliverable output power from this transistor was de-rated in order to keep the maximum thermal dissipation and maximum junction temperature of the device within safe limit.

With the help of the nonlinear model provided by the vendor, DC IV characteristics of this transistor were generated using Microwave office™. In order to avoid cross over distortion Class AB mode ($\Phi = 200°$) was selected for drain current excitation. From this IV graph, a value of 5.5 V ($\chi = 0.87$) for the knee voltage was estimated. This appreciable value of knee voltage reduces drain efficiency, to 64.73%. Adding some other circuit losses, the target efficiency for present design was set at 63%. For this device, peak voltage at the drain cannot exceed beyond 125 V (as per data sheet). Thus, values of α and β need to be calculat-

ed, other than the optimum one, so as to keep maximum drain voltage below 125 V using a 48 V (DC) drain supply.

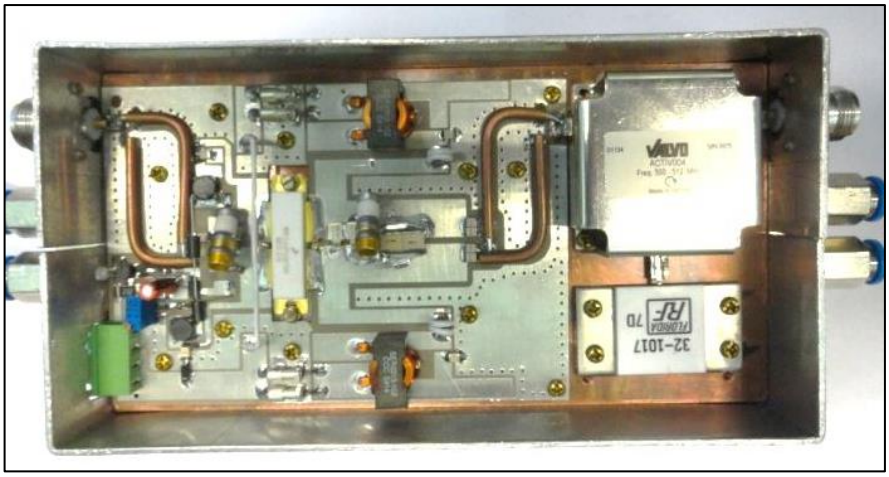
From the analysis presented in section 3.5.2, design values for the peak voltage, efficiency degradation factor and δ were calculated as a function of α and β, while satisfying upper (maximum drain voltage) and lower (knee voltage) physical limits of the device. The final design values of α and β comes out equal to 0.45 and 0.87, respectively. The corresponding voltage gain and conversion efficiency are 1.013 and 64%, respectively. Having calculated design parameters, different terminations were calculated using (3.71) These terminations are at the current generator plane of the transistor. Including the package parasitic and the effect of the nonlinear output capacitor [114], an impedance matching network was designed for this PA.

The dependence of output capacitor (C_{out}) on drain-source voltage was taken care by the following relation

$$C_{out}(V_{ds}) = 88[2 + 1212\{1 + \tanh(-0.0465V_{ds} + 2.7)\}] \text{ (pF)}$$

The input and output impedance matching networks are based on the balanced push pull configuration with transmission line balun; all on the same substrate (Arlon™ TC350 with thickness of 0.786 mm and ε_r of 3.5). The final circuit design and layout were optimized with the help of Microwave office™ software.

The complete fabricated PA was mounted over a water cooled copper plate (Fig. 3.31). Two water channels were provided just below RF transistor. Input and output baluns were realised using semi-rigid coaxial cables. An 800 W circulator from Valvo, was used to protect the PA against excessive VSWR. The bias circuit was implemented on the RF amplifier board itself. The dimensions of the layout of this J3 mode PA are smaller than earlier designed Continuous Class J PA.



Brief Details

Length, Width, Height:

20 cm, 10 cm, 4 cm

Substrate: TC350™

Connectors: N type

DC Bias: 48 V

Cooling: Water cooled

Fig. 3.31: Designed and fabricated Class J3 PA

3.6.2.1 Measured Results

The designed PA was put for a series of RF measurements, including the power gain, linearity, efficiency and VSWR at input side. The single point snapshot (measured at 505.8 MHz), captured from high power test bench, is shown in Fig. 3.32.

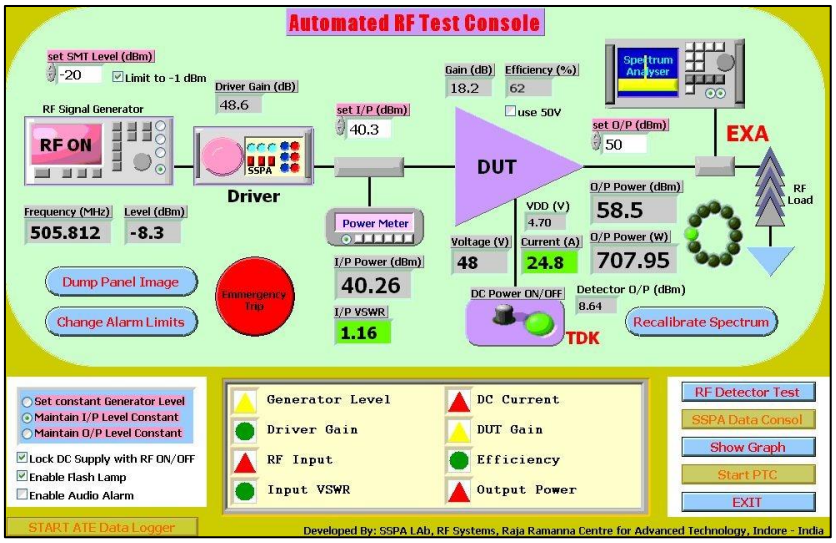


Fig. 3.32: Captured measured data for for Class J3 PA

It shows a power gain of 18.2 dB and an efficiency of 62% at the output power of 707.95 W. The DC operating point for this measurement is 48V with 24.8 A. The swept power measurements for different parameters are shown in Fig. 3.33. The drain efficiency (after de-embedding circulator loss) is 62% which is lower than the calculated value by nearly 2%. It must be due to associated circuit losses of RF components, especially of N connectors coaxial

to microstrip/stripline discontinuity, used here. The 1-dB bandwidth measured for this PA was 10 MHz. Spectral harmonics and spurious components, measured at the full output power of 700 W, were -35 dBc.

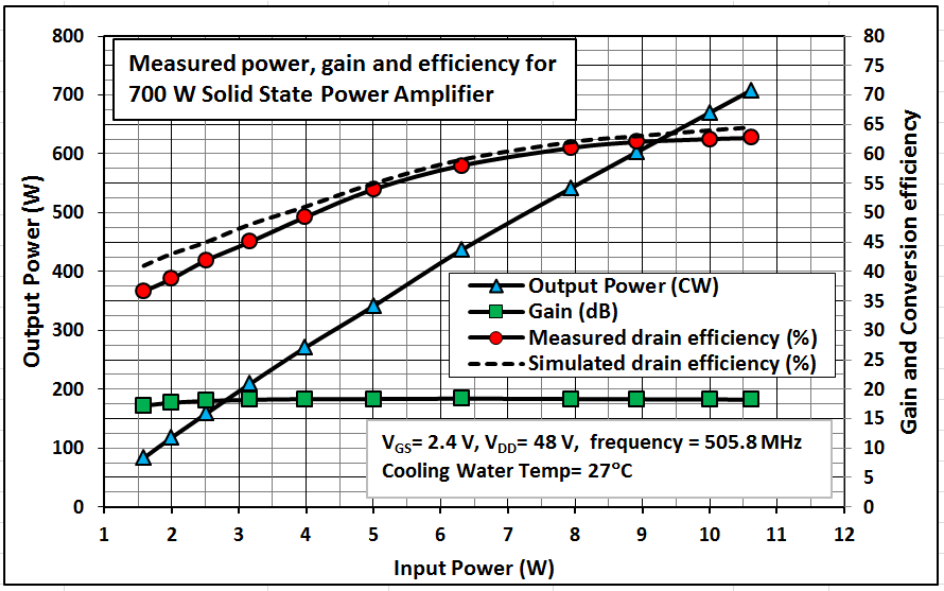


Fig. 3.33: Measured power, gain and efficiency for Class J3

3.6.3 Extended Continuous Class F Mode Amplifier

In this series of experimental demonstration, another high power design was carried out at 650 MHz, order to examine the analysis presented in the section 3.5.2.2. The CF and XCF modes studied, to date, are focussed on the low power PA design. The design parameters for the present PA include a power gain of 19 dB, a bandwidth of 5 MHz and its spurious response below 30 dB from the fundamental signal. Based on the circuit simulation studies and these specifications, an RF transistor *viz.* MRFE6VP8600H was selected for this PA. It consists of two similar devices which can be used in the push-pull configuration. In such configuration it is capable of delivering nearly 600 W of RF power at 650 MHz using a 50 V of bias across the drain-source. Its maximum drain voltage is 130V. The target efficiency was set at 70% in view of practicalities ($V_k \approx 7\ V$) of the transistor. The DC IV characteristics for one of this transistor were obtained with the help of Microwave office™, as shown in Fig. 3.34. For this circuit simulation, its nonlinear MET model, provided by the vendor, was used.

The normal Class F operation [69] with Class B excitation of the drain current is a good point for starting such design. Hence, the input drive and gate bias were selected, corresponding to the maximum swing of the drain voltage for Class B operation. Now design was manipulated towards Class F mode, by bringing Z_2 near to the short circuit and Z_3 near to very high resistive value, with the help of tuning capacitors. Fig. 3.35 shows the load network selected to fulfil these impedance conditions.

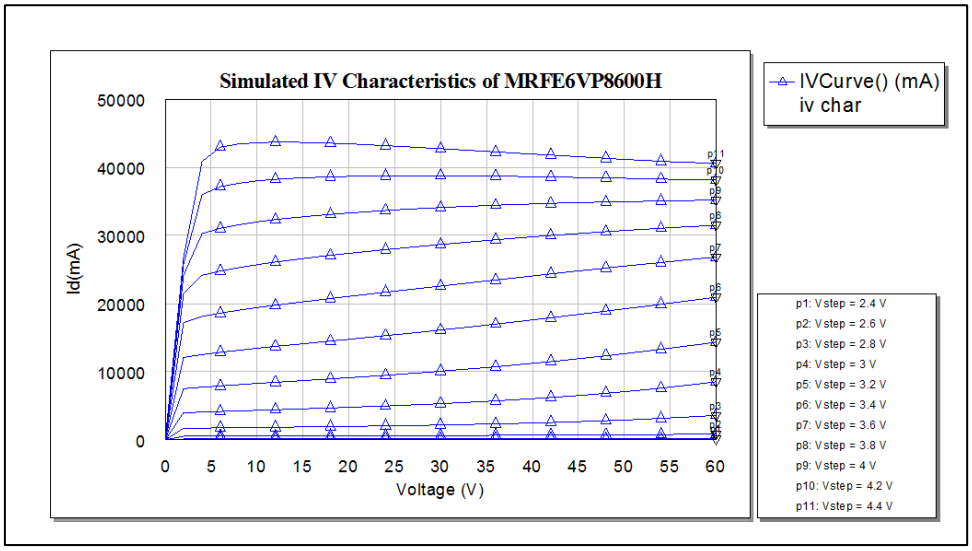


Fig. 3.34: IV characteristics of MRF8600 LDMOS

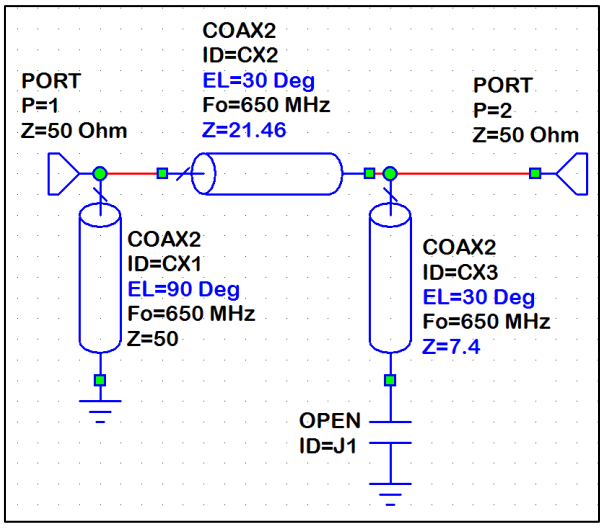


Fig. 3.35: Ideal output matching for Class F mode for 550 W amplifier design

Here, the series coaxial line CX2 and open-circuit stub CX3, both having an electrical length of 30º at the fundamental frequency, provide an open-circuit at the third harmonic.

Now Z_1 is scaled by a factor of $2/\sqrt{3}$ in accordance with (3.26) . This process establish Class F mode with Class B drain current excitation. The simulated efficiency of this configuration comes equal to 74.5%, with $V_k = 7\,V$ and ideal impedance matching components. Now, this design is manipulated toward extended continuous Class F mode where device parasitics may be easily absorbed in matching networks. For high power PA design, main problem is to accommodate peak design value of drain voltage. This voltage can be kept within limit by a proper manipulation of three design parameters *viz*. α, β, and γ. In present design α and γ were changed so as to tune ψ_1 and ψ_2, thus changing the imaginary part of Z_1 and Z_2. While changing the drive power, the parameter γ was adjusted to keep the drain current constant. Using graphical analysis, a family of wave shaped drain voltages were generated for different values of γ and α (Fig. 3.16). From this analysis design set was finalised with $\alpha = 0.95$, $\beta = \alpha/2$ and $\gamma = -0.5$. The selected value of α keeps the peak drain-source voltage less than 130V. The negative value of γ gives an inductive value of Z_4, which is easier to absorb in the matching circuit. The terminal impedances for OMN, calculated using (3.59) to (3.62) for increasing output power are shown in Fig. 3.36.

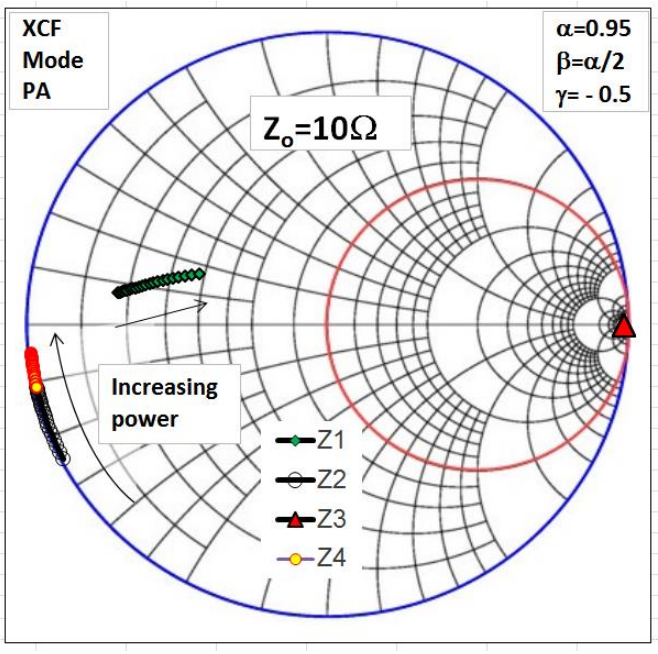


Fig. 3.36: Terminal impedances for extended continuous Class F PA

During the circuit simulation, it was observed that the nonlinear drain capacitor C_{out} reduces the performance sensitivity to Z_4. It gives a negative resistance at the harmonics, due to frequency generating property of nonlinear C_{out}. This nonlinear capacitor ensures a prominent I_3 that shapes the current toward the square wave, thus reducing its overlap with the voltage and improving the efficiency. The designed circuit was optimized with the help of Microwave office™, with proper augmentation of package parasitics and nonlinear drain capacitor.

The complete PA (Fig. 3.37) was fabricated on an RF substrate TC-350 ($\varepsilon_r = 3.5, h = 0.786mm$) it was mounted on a water cooled heat-sink. A 600 W circulator was used to protect the transistor from the reflected power. Compared to the previous amplifiers, this PA has compact dimensions of its PCB and therefore its enclosure. A water-cooled copper cold plate forms the base of this amplifier board. The simulated voltage and current corresponding to 500 W of output power, at the drain node of the transistor, for this PA are shown in Fig. 3.38. Effect of nonlinear output capacitor is seen clearly in these waveforms. The square-shaped drain voltage and current waveforms helps improving efficiency. However, overlapping between these waveforms is less than expected from the base line design. A photograph of the fabricated PA is shown in Fig. 3.39.

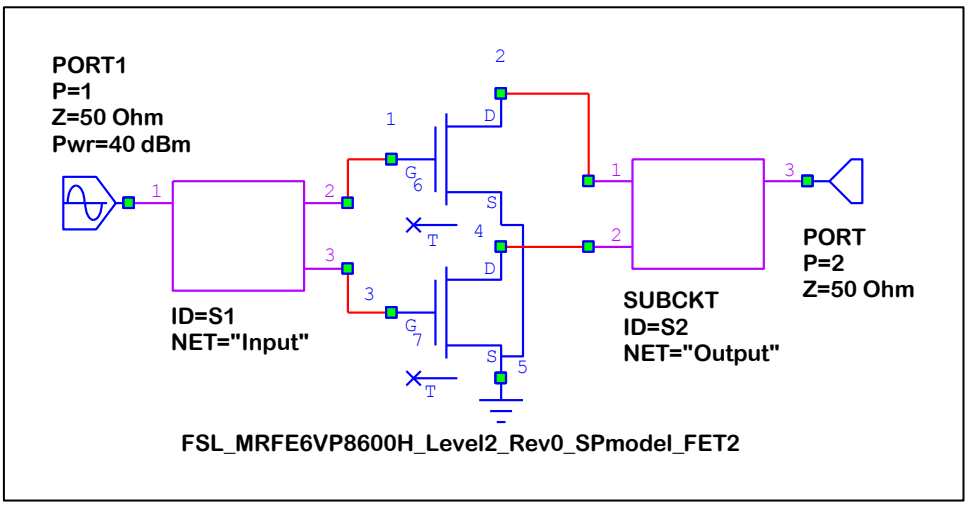


Fig. 3.37: Circuit scheme of extended continuous Class F mode amplifier

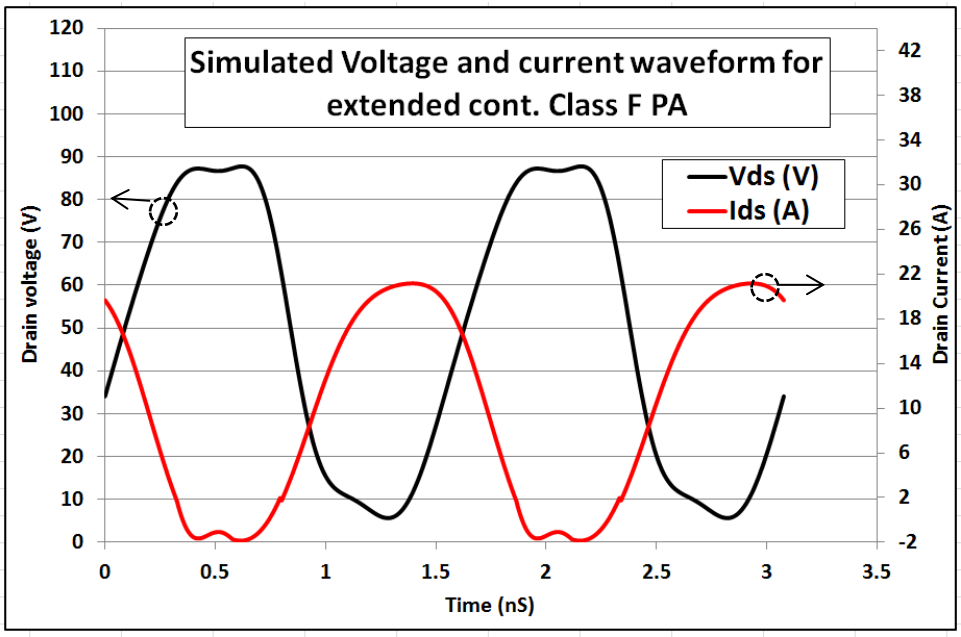
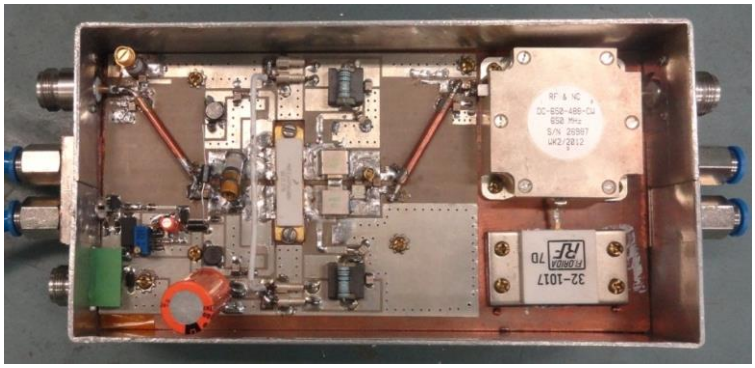


Fig. 3.38: Simulated voltage and current for extended continuous Class F PA



Brief Details

Length, Width: 16 cm, 10 cm

Height: 4 cm

Substrate: TC350™

Input/ Output Connector: N type

DC Bias: 50 V

Fig. 3.39: Designed and fabricated extended continuous Class F amplifier

The measurement for the output power, efficiency and power gain, performed for this PA using the RF test bench, are shown in Fig. 3.40 and Fig. 3.41. In former one, the measured efficiency at the saturate power of 600 W is near 68%, (with output circulator) with a power gain of 17.8 dB. Without circulator this efficiency goes up to nearly 70%. This is slightly higher than the simulated result. This must be due to the beneficial effect of the current at the fourth harmonic across the balun, which flattens the current waveform and allows the fundamental current component to be increased [158]. This effect of Balun was not taken during circuit simulation.

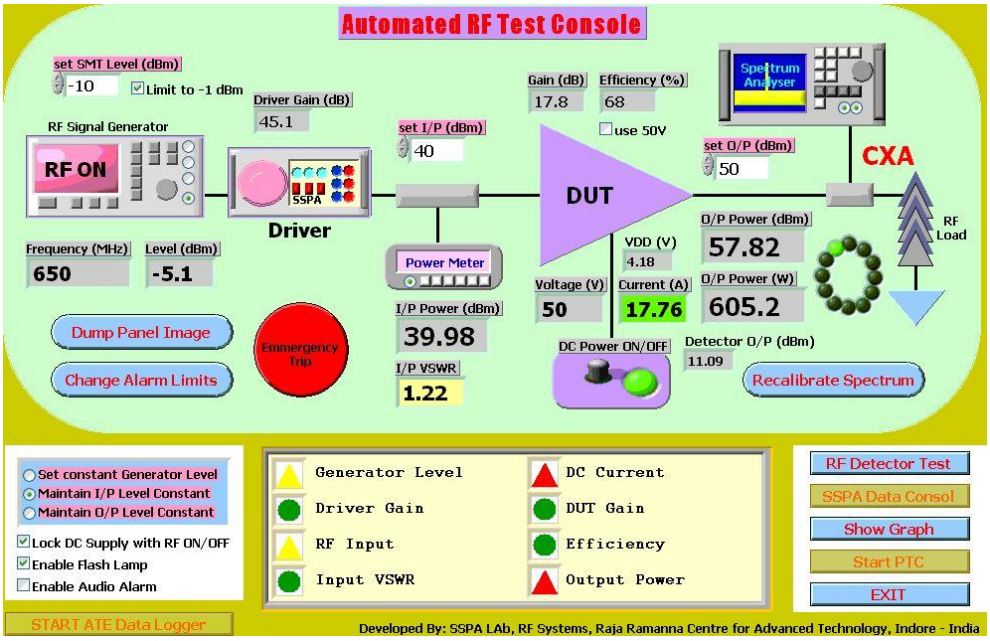


Fig. 3.40: Single frequency measurement for extended continuous Class F PA

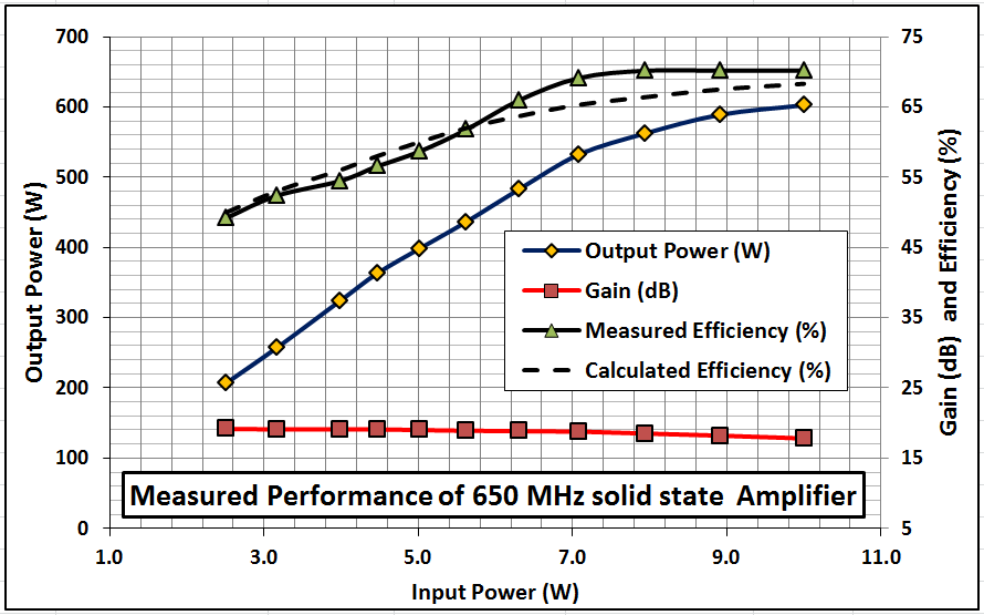


Fig. 3.41: Measured Gain and efficiency of extended continuous Class F PA

In Fig. 3.41, throughout the linear region, the power gain is more than 18.5 dB. The measured return loss (Fig. 3.42) is also satisfactory. It improves with increasing input power. This is a desired feature for high power amplifiers. Apart from this, the spectral response of this PA for harmonics and spurious components, as measured at high power, was -32 dBc.

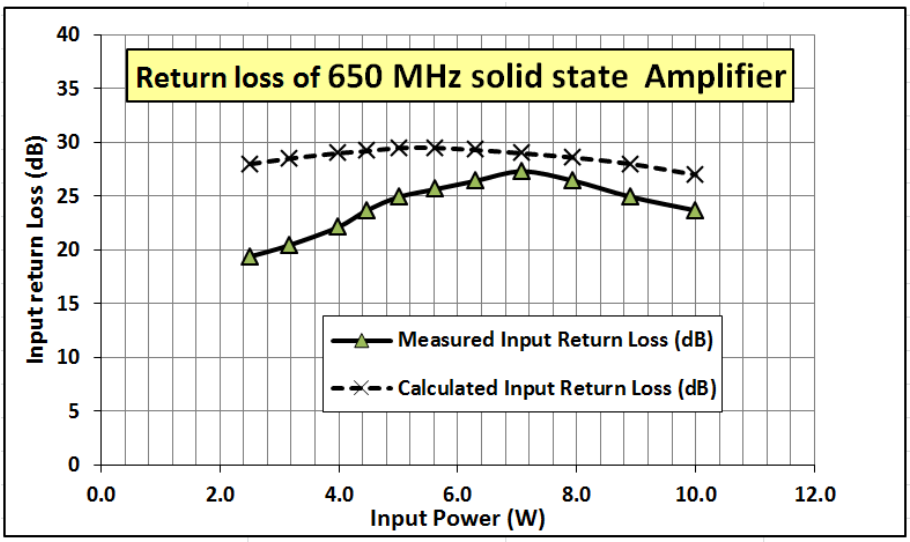


Fig. 3.42: Measured and calculated return loss for extended continuous Class F PA

In this chapter, an investigation was carried out with the experimental study for harmonic tuned solid state amplifiers. Unlike the conventional modes with shorted harmonics at the output, in these modes the output voltage waveform of the PA is engineered and optimized by selecting a set of harmonic terminations, for the given bias and input drive conditions. This provides some flexibility in impedance matching design in view of transistor's parasitics. The newer continuous design spaces were investigated for high power solid state amplifier design. In particular, two variants of the Class J mode amplifier in 500-700 W power regime, both at 505.8 MHz and an extended continuous Class F mode amplifier, capable of delivering 600 W at 650 MHz with 70% of DC to RF conversion efficiency were physically demonstrated. Different theoretical analysis suitably supported by the experimental investigation, presented in this chapter, seems promising techniques for high power amplifier design. Apart from such power amplifiers, the power divider and combiner play a pivotal role in a high power SSPA system using divide and combine strategy. These are discussed in the next chapter.

Chapter 4. RF Power Divider and Combiner

Due to a modest power of the solid state transistors, the RF power divider and combiner are essential for making a high power solid state amplifier, based upon the multi-way *divide and combine* architecture [53]. In such architecture the power combiner needs to handle high power as it sums output signals from multiple amplifier modules. Its insertion loss and any imbalance [75] in forward transmission coefficient directly affect the transmitter efficiency [76]. It governs [77] the graceful degradation [78] performance and thus available output power of the transmitter [79]. The overall growing interest in high power solid state RF source for particle accelerators has motivated for considerable research activities to develop high power, efficient and scalable power divider/combiner (PDC) structures. Generally, a passive power combiner can work as a power divider without any modification due to the reciprocity. Hence, concepts developed for the power combiner equally applies to a divider. In fact, these two components are collectively referred as PDC here, unless a specific case is discussed.

In present chapter, starting with useful features and an overview of RF power combining techniques, a design methodology is explored, for a novel N-way radial PDC, operating at kW level. These are realizable in slab like radial transmission line structures without incorporation of any isolation resistor and external tuning element. The rigorous and lengthy calculation for the radial line impedance is replaced by a simpler segmentation method. The outlined design configurations were simulated [174], using a full wave 3D simulator, *viz.* High Frequency Structure Simulator (HFSS™) [175], built and tested. This exercise yielded three 8-way radial PDC, operating at 352, 505.8 and 704 MHz, respectively. Each one of these is capable of handling RF power up to 4 kW. Followed by this successful development,

another design of two 16-way PDCs, operating at 352 and 505.8 MHz respectively is demonstrated with an enhanced power handling capability up to 16 kW. The choice of the frequency and RF power was based on project requirements of the institute. Along with these multi-way PDCs, binary dividers and combiners are also needed for obtaining a high power. Hence, a design of binary PDCs was also carried out at different power levels. A design proposal and discussion, based on full wave simulation studies is presented for the performance enhancement of low power 2-way PDC, by loading its T junction, separately, with a capacitive stub and a dielectric resonator. The necessary vector and high power scalar measurements of these designed PDCs were carried out for validating the design procedure and for demonstrating their suitability for high power SSPA system.

4.1 Important Features of Power Divider/Combiner

The power dividers, in a typical SSPA system architecture, are generally required at low power, whereas, the combiners need to handle high power. This difference makes their structures unlike in terms of the transmission media, port designs and a choice of dielectric. Nevertheless, from analysis point of view, a passive combiner structure can behave as a divider. Hence, any discussion, made henceforth, equally applies to both. Important features of an N-way equi-phase PDC, drawing attention for present work, are listed below. Being an (N+1) port network, the branch ports are numbered from 1 to N whereas feed port or summing port is assigned zeroth index.

- Insertion loss: It is the difference of power delivered to load without and with PDC. In radio and microwave frequency passive circuits, this term is frequently used. However, its mathematical definition is different from the reciprocal of the transducer gain, unless source and load impedance are real and equal to each other [176]. At a high power, the low insertion loss helps improving overall efficiency as well reduces the combiner‘s cooling requirement.

- Isolation: It is a quantitative estimate of the cross talk for a PDC network. This cross talk can result in spurious oscillations among the PA modules, connected at input ports of the combiner or output ports of the divider. The poor isolation results in increased heating due to reflected power leading to degradation in combined power, if some PA modules underperform or fail during operation. For a low power PDC, the isolation is achieved by using resistive elements. For PDC operating in kW level of RF and microwave power, these elements are not preferred as their placement inside the structure is difficult and their frequent maintenance is troublesome. In a multi-way PDC, for symmetric and loss-less case, this parameter gets improved with increasing number of branch ports. Or

$$\text{Isolation} \equiv \left| s_{cij} \right|^2 = -20 \log_{10} N \quad i, j = 1, 2, \ldots N \quad i \neq j \tag{4.1}$$

- Transmission coefficient: For a combiner each branch contributes to final output at feed/summing port (assigned port zero) according to its coupling or transmission coefficient. It is defined as the ratio of forward power wave from any one of the N branch ports to the forward power wave at feed port, when all other branch ports are matched terminated. For a symmetric and equi-phase PDC its magnitude in dB is equal for each branch port and it is given by

$$\text{Transmission coefficient} \equiv |\, s_{coi}|^2 = 10 \log_{10} \left(\frac{1}{N}\right) \quad i = 1,2, \ldots N \tag{4.2}$$

This is an intrinsic property of the passive structure of the PDC.

- Amplitude and phase imbalance: The variation or peak-to-peak deviation in the transmission coefficient from branch to branch will cause a power loss in the PDC. It increases reflection or power consumed in the isolation resistor, if incorporated. This imbalance/variation may be due to the practical limitation during its fabrication in translating electrical design of the PDC into a perfect symmetrical structure. Thus symmetry and topology of the PDC is important in deciding the degree of imbalance.

- Bandwidth: The frequency range over which rated performance is achieved is useful bandwidth of the PDC. In particle accelerators, narrowband PDCs are required. But for wideband applications, this parameter becomes a main criterion for designing the PDC.
- Return loss: The return loss or VSWR at the combined or feed port is an important parameter for determining impedance mismatch with other RF components in the system. For feed port (assigned an index of zero) the return loss is expressed as s_{coo} assuming that all other ports are properly matched terminated.
- Dividing/Combining efficiency: This is a ratio of the net power delivered to the load at the output to the sum of available input powers [177]. When these input signals are equal and in-phase, this efficiency is limited by only the insertion loss of the PDC. For a power combiner, excited in even mode and matched terminations at its branch ports as well as the output port, it is given as

$$\eta_c = \sum_{i=1}^{N} | s_{coi}|^2 \tag{4.3}$$

  This expression is true without any assumptions concerning the properties of the linear power combiner, such as losslessness, reciprocity, matching, or isolation. These properties do, however, influence the value of η_c. This issue is discussed in detail in chapter 6.
- Physical size and performance repeatability: The overall dimensions and physical structure of the PDC will be dictated by its power handling capacity and the selected dividing/combining technique. They can be realized in a number of different transmission media such as microstrip, coaxial line, or waveguide. The choice of the transmission medium heavily impacts the resulting size and circuit losses. For example, a radial PDC using a microstrip/slab line will be compact compared to a waveguide based design. The compact size of a PDC is important for obtaining a high RF power for per unit volume of the SSPA space. Also, the PDC structure should be fabrication-friendly. Due to their re-

quirement in multiple, in a typical SSPA operating in tens of kW, their design and performance repeatability is a desired feature for getting a high yield during their fabrication and operation.

4.2 Overview of N-way Power Dividing/Combining Techniques

Due to their crucial role in high power applications, different solutions were studied to address the power dividing/combining issue. These techniques broadly include spatial approach [178] and circuit-level approach. The choice of a particular approach depends upon the specific application, RF power and frequency. In the spatial-level combiners, the power combining process is performed in an unbounded [179] or partially bounded [180] region, and it is accomplished through transmit/receive radiating elements [181]. It is feasible near millimetre-wave frequencies. This approach is not discussed here as majority of the particle accelerator employ RF and microwave systems operating somewhere within VHF to S band. For this frequency regime, circuit level approach is quite suitable. In such circuit-level PDCs, the power is supposed to be confined within a finite region, so that any radiation into free space is considered as an undesired and lossy occurrence. Such PDCs can be further divided into the two families of resonant and non-resonant types. In the former type of combiner, the sum of output powers from a number of devices is obtained by coupling their outputs to a single resonator [87] . Because of their resonant nature, they are narrowband PDCs. The transmission medium of the cavity can be a coaxial or a waveguide, but in both of them N input ports excite a single cavity. Non-resonant techniques [81] usually use transmission lines in their dividing/combining path. Because of their non-resonant structure, they offer the wide-band operation. They are split into two categories: N-way PDCs and corporate PDCs. The former type of combiners adopts a star/radial structure where N input ports are properly combined into an output port in a single step. In this class the popular Wilkinson PDC [89] (two-way or N-way), hybrid structures (branch-line, rat-race, Lange coupler, etc.), multi-ports

radial, bus bar, and others can be recognized. The principal problem with the Wilkinson approach at high power is that for N >2 it is generally not possible to connect sufficiently powerful isolation resistors in planar circuits. Accordingly, a number of modifications of the concept [90] [91] [92] have been suggested over the years. Conversely, corporate PDCs use a tree structure and travelling waves or serial topologies [81]. For N-way PDC, three popular circuit level schemes and their comparison is discussed next with their role as a combiner.

4.2.1 Travelling Waves or Serial Combiner

In a serial combiner (Fig. 4.1), for an N-stage combiner each successive stage or coupler adds $(1/N)^{th}$ part of the output power. The number of the stage determines the required coupling coefficient for that stage. Neglecting losses, the necessary coupling coefficient for the N^{th} stage is $10\log_{10}(N)$ in decibels [81]. One advantage of this configuration is that another stage can be added by simply connecting the new PA to the line after the N^{th} stage through a coupler with $10\log_{10}(N+1)$ coupling coefficient.

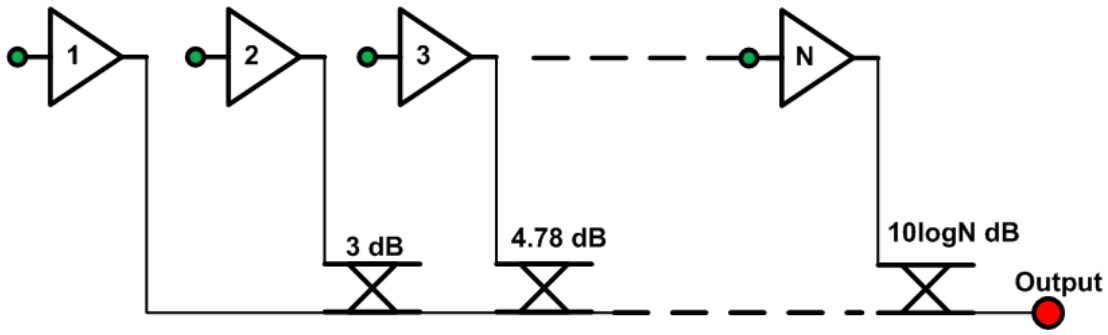


Fig. 4.1: A serial combining scheme

This approach is non-binary, and, in principal, any number of PA can be combined. Although, it is difficult to build the couplers with the low loss and high coupling coefficients, necessary when larger numbers of devices are to be combined. The RF power losses in the couplers reduce the combining efficiency and bandwidth attainable. Based on the power loss incurred to each input signal in forward direction, the combining efficiency [81] in terms of L (insertion loss of couplers in dB) and *N* (number of stages) is

$$\eta_c = \frac{1}{N}\left[10^{(N-1)L/10} + \sum_{i=1}^{N-1} 10^{iL/10}\right] \tag{4.4}$$

It is obvious that the combining efficiency decreases as number of devices increases.

4.2.2 Tree Combiners

The tree combiners use a multi-tier structure of *K*-way combiners (typically *K* = 2 or 3) in *S* stages to create a topology (Fig. 4.2) with input ports or individual PAs (=*N*) equals K^S.

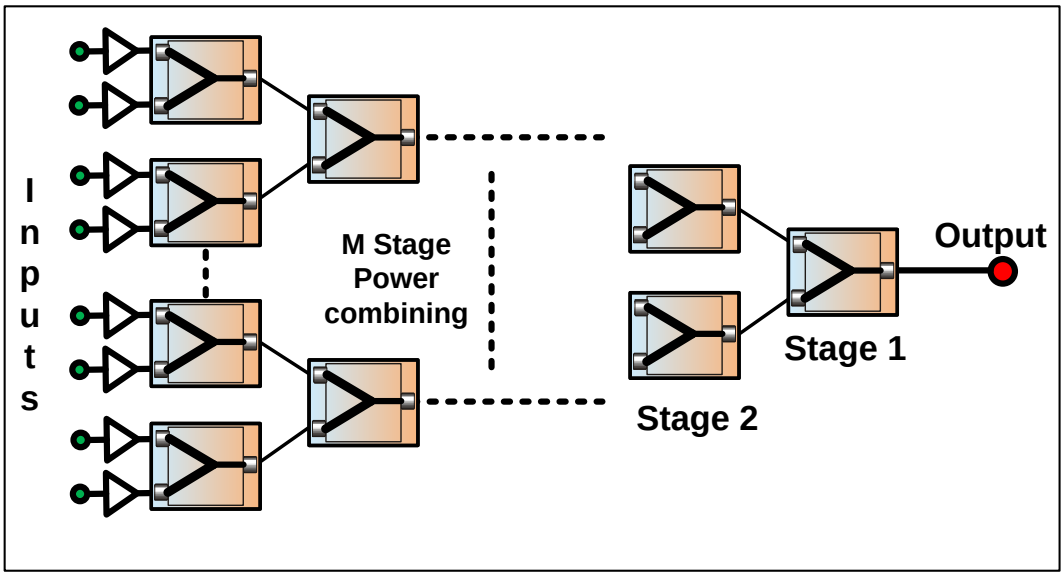


Fig. 4.2: A corporate combining scheme with binary tree

The combining efficiency in terms of L (insertion loss in dB of each combining stage) is

$$\eta_c = 10^{LS/10} \tag{4.5}$$

For obtaining high output power, the tree-structures, with large S, have the disadvantage of utilizing a multitude of 2-way or 3-way combiners. Accordingly losses in connecting transmission line segments increases.

4.2.3 Multi-way Radial Combiner

Both of the serial and tree combiners show inferior performance with increasing number of PAs in the SSPA system. For such case, multi-way combiner with large N (>>2) using radial symmetric topology (Fig. 4.3) is useful. The radial symmetry is obtained by placing

peripheral ports, distributed along a circular disk or along pill box type waveguide. Thus, it comprises of an axially oriented mode transducer or impedance converter (summing port) coupled to a radial base. This base combines/divides a plurality of peripheral/branch ports (coaxial or waveguide) into a single summing port. From circuit point of view it is an (N+1) port junction endowed with complete rotational symmetry with respect to the first N ports.

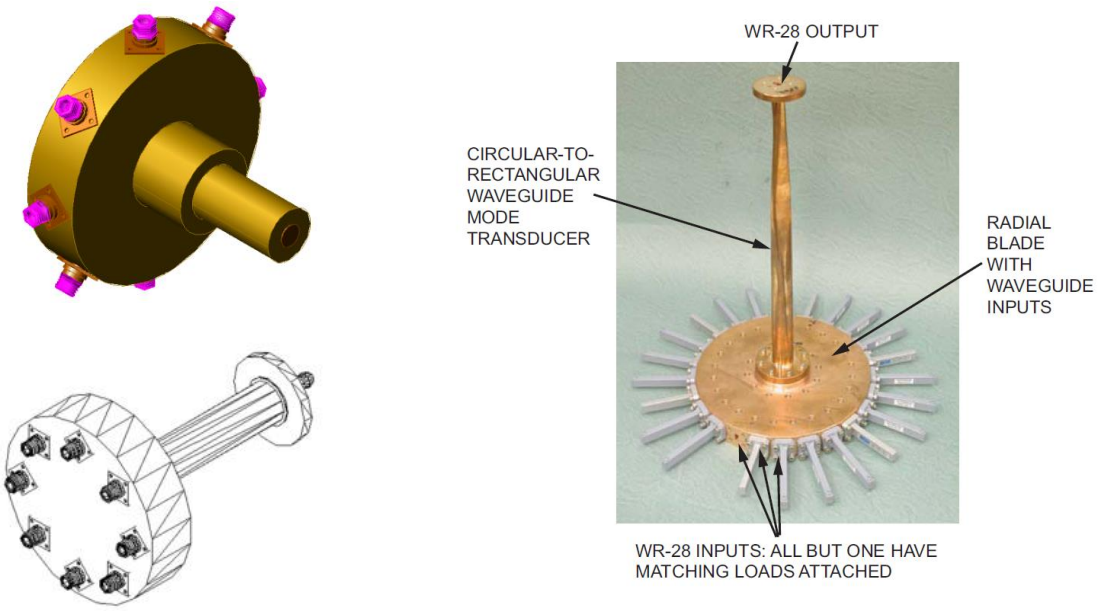


Fig. 4.3: Radial combiner in coaxial (left) and waveguide (right) [182] configuration

For N-way dividing/combining, generally, radial structures are preferred, due to their simple design and easily achievable amplitude and phase balancing between their branch ports. Unlike tree and serial structures, the radial PDC can lead to a higher combining efficiency because it divides/sums the power of the N PAs directly in one step, without having to proceed through several stages. This fact is evident from the comparison of the combining efficiency for these three topologies, shown in Fig. 4.4. To cater typical requirement of majority of particle accelerators much higher power radial PDC, as a part of modern RF source operating in kW regime, at comparatively lower frequency band (VHF to S band) is required. Apart from high power handling capability, it should be efficient, compact, reliable and repeatable.

As the outcome of this research, perhaps radial N-way PDCs have proved to be most promising candidate for high efficiency and high power applications. For power requirement, going beyond the capability of such multi-way PDC, a combination of binary tree and such radial structure can be adopted.

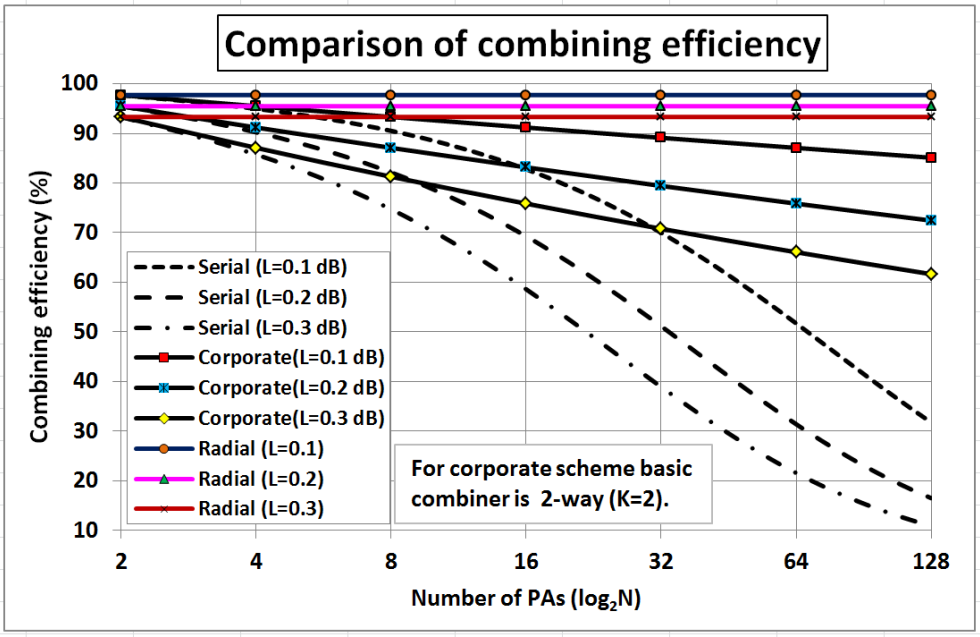


Fig. 4.4: Comparison of combining efficiency for different schemes

4.3 Proposed Radial Power Divider/Combiner

In order to accomplish power dividing/combining task for a high power SSPA, the investigation was made for different radial PDC structures. Based on this research studies, a novel kW level radial PDC design, realizable in stripline like structure (slab-line) without isolation resistor and external tuning element, is proposed as shown in Fig. 4.5. This structure consists of three parts: the feed line, dividing/combining path and N-way branch ports. Being a passive component, it can equally work as a power divider. The feed line is a cascaded structure of the coaxial line sections. These sections are needed for converting the input impedance at the main port (50 Ω) to somewhat lower impedance, as seen by the radial line at the junction point of the feed line and the dividing/combining path. The feed line, transferring power to/from the dividing/combining path, is perpendicular to the radial line. The divid-

ing/combining path is a circular radial transmission line, realised with low loss parallel plate slab-line type disk structure. The feed line is connected at its centre whereas branch ports are located near its circumference. These ports can be placed either in the radial direction or parallel to the axis of the main port (as shown in Fig. 4.5). They are usually designed for a characteristic impedance of 50 Ω.

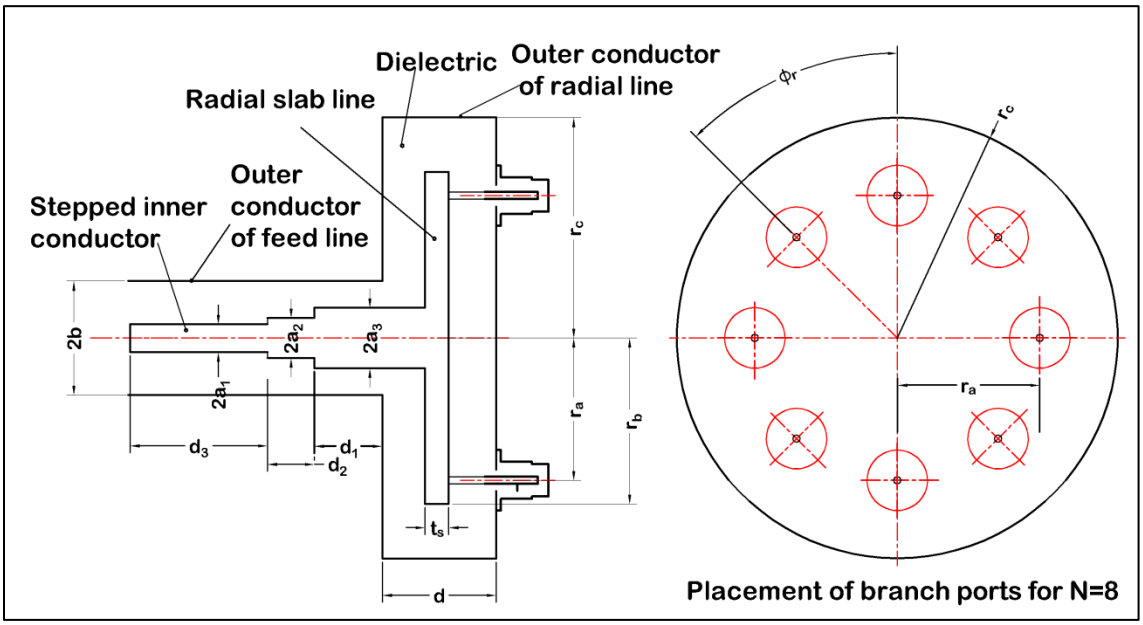


Fig. 4.5: Proposed N-way radial PDC using radial slab type line

The radial line accomplishes the task of impedance matching, at high power, without incorporating quarter wave transformer. Along with providing a mechanical rigidity, its symmetry minimise insertion loss and phase imbalance. The dielectric inserted here, helps operation at higher power and support to the inner structure of the combiner. The absence of isolation resistor adds toward reliability, which otherwise may suffer due to heat dissipation, ageing and mechanical difficulty in placing resistor inside structure. Reduced isolation, due to absence of resistor, can be regained by using circulator at the output of solid state amplifier modules.

Although a detailed full-wave analysis for the scattering characteristics, based on a mixed potential integral-equation formulation [183], has been developed for N-way radial

PDC, it is numerically too intensive to deal with the present structure. Being rotationally symmetric structure, it was analysed [184] by a partial spectral decomposition of its scattering matrix. This approach produces N/2 one-port boundary value problems, as well as a single two-port problem, which can be solved by means of standard full-wave simulators by applying Floquet boundary conditions [185]. For analysis purpose, a circuit model of the proposed PDC was developed in in Microwave office™ simulator, as shown in Fig. 4.6.

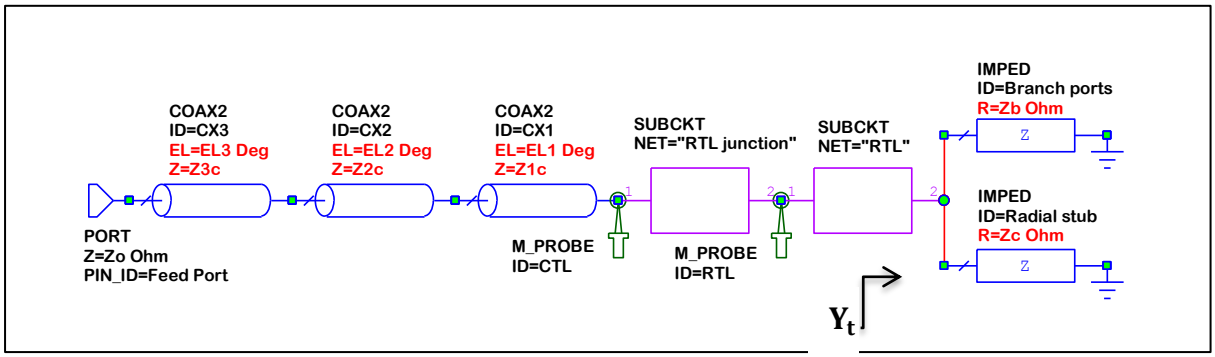


Fig. 4.6: Circuit model of proposed N-way PDC with radial line

In this model, three coaxial line sections represent stepped transmission lines for the impedance matching between the main port and the circular radial line. These sections have different characteristic impedances and electrical lengths. The sub-circuit *RTL junction* is radial to coaxial line junction, to be discussed later. It describes the radial line, having varying input impedance with respect to its radius as seen from the centre. At the radius of r_a, terminating admittance (Y_t) is a sum of parallel resultant of branch ports' admittance $(1/Z_b)$ and input admittance $(1/Z_c)$ of open circuited radial stub with annular ring with a width of $(r_b - r_a)$. The design of radial PDC depends upon the ability to model a radial transmission line. The analysis approach for this purpose is discussed next.

4.3.1 Design of Circular Radial Transmission Line

A circular radial transmission line, useful for the present PDC, consists of a plate sandwiched between two parallel ground-planes (Fig. 4.7) and a dielectric material. When excited at the centre, it will generate electromagnetic waves, guided radially outwards from the

source. Both the electric and magnetic fields, in dominant mode, vary only in the direction of propagation, r, and are constant in the z and angular directions. Also, both are transverse to r. For PDC design, one needs to calculate the input impedance of this radial line at the centre or excitation point. This calculation characterise the sub-circuit model *RTL*, shown in Fig. 4.6. For this calculation, a classical approach is discussed in present section, followed by a piecewise approximated segmentation approach, which was adopted for the final design.

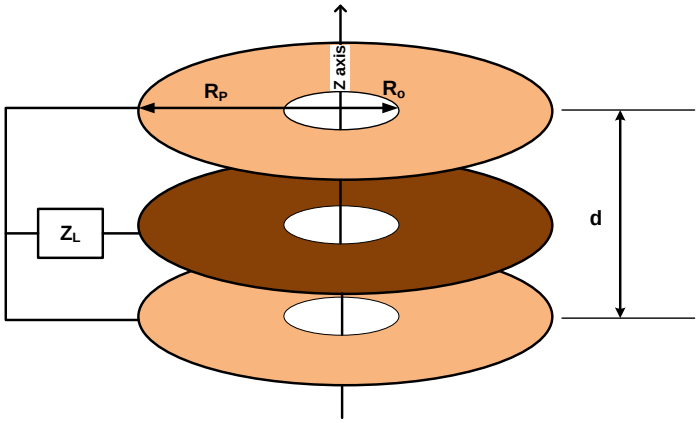


Fig. 4.7: A circular radial transmission line

The solution of the wave equation for the radial line, in terms of Bessel and modified Bessel (Neumann) functions, was presented by Marcuvitz [118] and Ramo [119]. Due to a symmetric or even mode excitation, the electromagnetic interaction in radial PDC is predominantly due to radial waves in the dominant mode, axially symmetric with respect to the feed line. The field configuration in this mode resembles the TEM mode in strip-line type transmission line, having planar inner conductor in the middle and ground planes on its top as well as bottom, duly separated by a dielectric material. This description is valid as PDC is used normally in electrically symmetric configuration with an equal potential (even mode excitation) on all branch ports. In practice, the propagation of higher order modes is easily prevented by a careful design and good mechanical symmetry. In this dominant mode, the electric and magnetic fields contain only $E_z(r)$ and $H_\varphi(r)$ components (where φ is the

rotation about the z axis). These EM fields give rise to a radially dependent characteristic impedance, defined as

$$Z_0\,(r) = Z_{TEM} \cdot \frac{G_{0h}(kr)}{G_{1h}(kr)} \tag{4.6}$$

Here $G_{0h}(kr)$ and $G_{1h}(kr)$ are magnitude part of Hankel functions, defined in [119]. Also Z_{TEM} is given for strip line [186] as

$$Z_{TEM} = \frac{120\pi}{\sqrt{\epsilon_r}} \tag{4.7}$$

The symbol k is the wave number, equal to $2\pi/\lambda$. Also λ is the wavelength of the signal suitably augmented by the relative permittivity (ϵ_r) of the dielectric material. Such a wave has no variations in the z direction or circumferentially. As described in [118], the normalized impedance with respect to $Z_0\,(r)$, for this radial line operating in the dominant mode, can be expressed as

$$z'(r) = \frac{Z\,(r)}{Z_0\,(r)} = \frac{z'(r_0)F_1 + jF_2}{jz'(r_0) + F_2F_3} \tag{4.8}$$

Here $z'(r_0)$ is the relative input impedance, normalised to the characteristic impedance, at another radius r_0 with $r_0 > r$. Also F_1, F_2 and F_3 are given as

$$F_1 = \frac{J_1(kr)N_0(kr_0) - N_1(kr)J_0(kr_0)}{J_1(kr)N_1(kr_0) - N_1(kr)J_1(kr_0)} \tag{4.9}$$

$$F_2 = \frac{J_0(kr)N_0(kr_0) - N_0(kr)J_0(kr_0)}{J_1(kr)N_1(kr_0) - N_1(kr)J_1(kr_0)} \tag{4.10}$$

$$F_3 = \frac{J_1(kr)N_0(kr_0) - N_1(kr)J_0(kr_0)}{J_0(kr)N_0(kr_0) - N_0(kr)J_0(kr_0)} \tag{4.11}$$

J_n are Bessel functions and N_n are Neumann functions.

Thus, the input impedance of the radial line at its centre can be calculated by using (4.8) and (4.6). As evident, $z'(r)$ is not real but complex, because the input impedance of an infinite radial line is not equal to its characteristic impedance. For this calculation, approxi-

mate expressions for $z'(r)$, provided by Marcuvitz [118], are useful. According to this formulation, $z'(r)$ can be approximated for two conditions of kr as follows

$$\frac{1}{z'(r)} \cong -j \tan\left(kr - \frac{\pi}{4}\right) \quad \text{for } kr \gg 1 \tag{4.12}$$

$$\frac{1}{z'(r)} \cong -j \frac{kr}{2} \quad \text{for } kr \ll 1 \tag{4.13}$$

This calculation is significantly complicated due to the existence of a complex characteristic impedance with spatial dependence, as well Bessel function arguments, associated with radial line parameters. Therefore a different approach that leads to a simpler formulation using available CAD programs [187] is adopted here.

4.3.2 Segmentation Approach for Radial Line

In this approach, with reference to Fig. 4.8, a radial line having outer radius of R_p and inner radius of R_o is segmented into q numbers of narrow concentric, annular and adjacent strips. Each of these strips is a radial transmission line with small width, for which, constant characteristic impedance can be assumed.

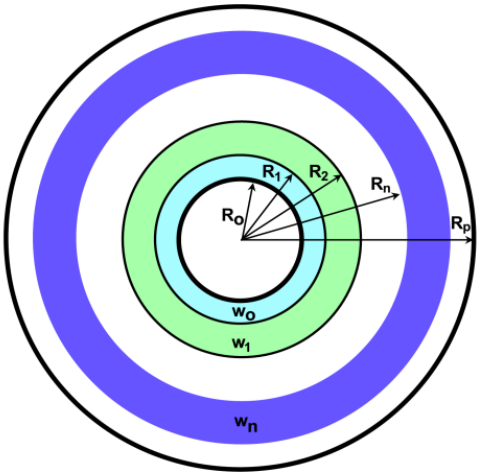


Fig. 4.8: Circular radial transmission line segmented in strips

The calculation of this characteristic impedance can be carried out using the popular strip line theory. For a normal stripline having strip width of w_s and ground plane distance of d,

the expression for the characteristic impedance, derived by estimating the static capacitance, can be approximated [186], for ($w_s/d \ < 0.35$), as

$$Z_{0,strip}(r) = Z_{TEM} \cdot \frac{d}{4w_s} \tag{4.14}$$

As stated earlier, the dominant mode in the radial transmission line resembles the popular TEM mode in strip-line. Hence, the characteristic impedance (neglecting imaginary part) of the radial line, at any radius r, can be approximated by replacing w_s by $2\pi r$. Or

$$Z_0(r) = Z_{TEM} \cdot \frac{d}{8\pi r} \tag{4.15}$$

Though, this formula was derived by neglecting the presence of fringing capacitance, it gives a starting value. The radial line in the proposed PDC is a slab line, having a significant thickness of strip or inner conductor. Hence, the calculation of the static capacitance needs to be modified, for taking into account the finite thickness t_s (Fig. 4.5) of this slab. The modified expression, derived for this purpose, is given as

$$Z_0\,(r) = Z_{TEM} \cdot \frac{(d - t_s)}{8\pi r} \tag{4.16}$$

Again referring to Fig. 4.8, each of the annular strips, being a transmission line in the radial direction, can be thought to have the characteristic impedance, which does not show spatial variation. Thus, when all the strips are cascaded, they approximate the original radial line. Thus input impedance of the radial line can be calculated by finding average radius of the strip and its width. Thus sub-circuit *RTL* in the circuit model (Fig. 4.6) is characterised by q number of cascaded transmission lines, all operating in nearly TEM mode. Since, the curvature of the strip limits the accuracy of this approach, the segmentation is performed in such a way that the ratio of strip width to its radius is always equals to a constant. Or

$$\frac{w_0}{R_0} = \frac{w_1}{R_1} = \cdots\cdots = \frac{w_n}{R_n} = C_r \tag{4.17}$$

Here, w_n and R_n are the width and the radius of the n^{th} strip while C_r is a curvature constant. Using this condition it can be easily shown that

$$R_n = R_0(1 + C_r)^n \tag{4.18}$$

$$w_n = w_0(1 + C_r)^n \tag{4.19}$$

The average radius of the first strip and n^{th} strip are

$$R_{1,ave} = R_0\left(1 + \frac{C_r}{2}\right) \tag{4.20}$$

$$R_{n,ave} = R_{1,ave}(1 + C_r)^n \tag{4.21}$$

Also total number of strips can be determined from

$$\frac{R_p}{R_0} = (1 + C_r)^q \tag{4.22}$$

Here q is the total number of strips. Thus, the required width and average radius of a strip can be calculated by (4.19) and (4.20). This width of the strip can be taken as the length of the transmission line. This completes the calculation for the relative input impedance of the radial line for PDC design.

Using this analysis, the value of input impedance Z_c (Fig. 4.6) at radius r_a, contributed by annular ring of length ($r_b - r_a$), can also be computed, by treating an open circuit at one end. The calculation of r_c depends more on electric field, which can be sustained in the annular region having width of ($r_c - r_b$) and also on the footprint of N connectors to be placed along the periphery of the radial line. This placement must provide some space for the cable movement, while making a connection. Hence, a few iterations may be required before the final selection. Thus, values of radii r_a, r_b and r_c can be calculated. Having analysed the radial line, the next step in this procedure is the design of the feed line.

4.3.3 Designing Feed Line

The feed line consists of air-dielectric coaxial transmission line sections, with stepped impedance, to match the radial line to a 50 Ω EIA coaxial port. The impedance transfor-

mation is achieved by stepping the radius of the inner conductor, and keeping the radius of the outer conductor constant as shown in Fig. 4.5. The radius of the outer conductor is determined by the connector (1-5/8" EIA or 3-1/8" EIA port) to be used as the summing port. The length and inner conductor radius of each section of line are used as parameters in the circuit model optimization. The effect of a step in the coaxial line is modelled by small static capacitances at the junction [188]. This capacitance $C_j(r)$ is given by

$$C_j(r) = \frac{\varepsilon_0}{100\pi}\left[\frac{\tau_1^2+1}{\tau_1}\ln\left(\frac{1+\tau_1}{1-\tau_1}\right) - 2\ln\left(\frac{4\tau_1}{1-\tau_1^2}\right)\right] + \frac{1.11}{1000}(1-\tau_1)(\tau_2-1) \text{ pF/cm} \quad (4.23)$$

Where

$$\tau_1 = \frac{r_3 - r_2}{r_3 - r_1}, \text{ and } \tau_2 = \frac{r_3}{r_1} \quad (4.24)$$

Here r_3 is the radius of the outer conductor of a coaxial line having step discontinuity. Also r_2 and r_1 are the radius of the larger and smaller inner conductor, respectively. The capacitance is obtained by multiplying (4.23) by the circumference ($2\pi r_3$) of the outer conductor. For present design there are two coaxial steps in the feed line. Hence calculation needs to be performed twice by substituting the set of (r_1, r_2, r_3) in (2.32) with (a_1, a_1, b) and (a_2, a_3, b), with reference to Fig. 4.6. It completes the first order design of the feed line.

In order to account for the effect of the discontinuity at the coaxial/radial line junction (modelled by sub-circuit *RTL junction* in Fig. 4.6) additional reactive components, contributing to the input impedance of the coaxial and radial lines, need to be estimated. Williamson [189], modelled this junction in terms of reactive components *viz.* B_1, B_2 and B_3, as shown in Fig. 4.9. This junction model contributes two capacitances to the feed line and one capacitance to the radial line. The junction model is accounted for using the following expressions [101]

$$B_1 = -\frac{2\pi}{Z_{TEM}\ln(b/a_1)} \quad (4.25)$$

$$B_2 = \frac{4\pi}{kdZ_{TEM}\ln^2(b/a_1)}\sum_{m=1}^{\infty}\frac{1}{q_m^2}\frac{K_0(q_m kb)}{K_0(q_m ka_1)}[I_0(q_m ka_1)K_0(q_m kb) - I_0(q_m kb)K_0(q_m ka_1)] \quad (4.26)$$

$$B_3 = \frac{2\pi ka_1}{kdZ_{TEM}}\cdot\frac{J_1(ka_1)Y_0(kb) - J_0(kb)Y_1(ka_1)}{J_0(ka_1)Y_0(kb) - J_0(kb)Y_0(ka_1)} \quad (4.27)$$

$$T = \frac{(2/\pi)\ln(b/a_1)}{J_0(ka_1)Y_0(kb) - J_0(kb)Y_0(ka_1)} \quad (4.28)$$

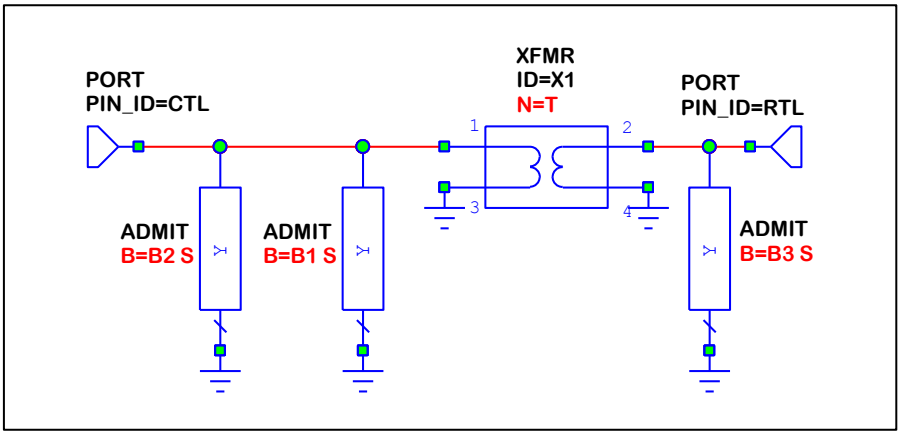


Fig. 4.9: Radial-line/coaxial-line junction with equivalent circuit

Where

$$q_m = \sqrt{(m\pi/kd)^2 - 1}$$

Using these values the impedance at the coaxial port of the junction can be derived as

$$Z_{CTL} = \frac{1}{\frac{1}{T^2 Z_{RTL}} + j\left(B_1 + B_2 + \frac{B_3}{T^2}\right)} \quad (4.29)$$

Where Z_{CTL} is the impedance at the coaxial port, Z_{RTL} is the impedance of the radial line. The normalized imaginary part (with respect to real part) of Z_{CTL} increases with the frequency. At UHF its value is negligible; hence, it may be omitted in the present modelling.

4.3.4 Full Wave Electromagnetic Structure Simulation

After the design of the constituting parts, it is necessary to simulate the whole PDC structure, for final optimisation with the help of a 3D solver like HFSS™. In this simulation,

different geometrical parameters of the feed line, radial line and location of branch port connectors need to be fine-tuned to achieve desired goal. This goal often involves an optimization of important parameters like return loss at the main port, insertion loss of the PDC and isolation among branch ports. Finally, any possibility of the electric field breakdown needs to be studied by providing sufficient spacing between the inner and outer conductors of the different transmission lines and by removing any sharp corners within the structure.

While performing such electromagnetic simulation, it is often impractical to measure the desired parameters of the RF structure, directly at its ports/terminals. Instead the structure is typically *embedded* at a reference plane, some distance away from it. De-embedding [190] is the mathematical process of removing the embedding networks and determining the true parameters of the device under test. It is needed to remove the discontinuities at numerical ports and to remove lengths of line from our numerical fixture.

4.4 Design and Measurement of 8-way Radial Divider/Combiner

In order to demonstrate theoretical calculation described in last section, three types of novel 8-way PDCs, operating at 352, 505.8 and 704 MHz respectively, were designed. Their design specifications were selected so as to fulfil project requirements of the institute. These include combining efficiency better than 90%, 1-dB bandwidth of 10 MHz (minimum) and minimum return loss of 20 dB, all at respective centre frequency of 352, 505.8 and 704 MHz. In addition to this the overall insertion loss (other than coupling) should be less than 0.5 dB and combined RF power up to 4 kW (average) should be achievable for all these PDCs. As this output power is within 7 kW, a standard rigid coaxial line with EIA 1-5/8" flange, was selected for its main port. Similarly, at branch ports expecting the maximum power below 1 kW, N type connectors were selected. The N type connectors, in 8-way PDC, were placed in parallel but opposite direction to feed line. The radius of circular disk (r_b) and radius of outer conductor (r_c) were 8 cm and 9 cm respectively for all of the PDCs. Impedance matching

from the radial line to the 50 Ω impedance was carried out by different coaxial sections having same outer conductor diameter ($2b$) of 38.6 mm but varying diameter of inner conductor. The length of the feed line ($d_1 + d_2 + d_3$) is 95 mm in 8-way PDC at 352 MHz and it decreases with increasing frequency. No additional external tuning screw or isolation resistors were used in this design. After initial design calculations, their EM model (Fig. 4.10) was developed for a full wave simulation using HFSS™. Being a passive and reciprocal circuit, it can equally perform as a power divider or combiner. The simulated E and H field patterns are shown in Fig. 4.11 for the 352 MHz PDC. During this EM simulation, care was taken to remove high electric field spots in the constricted coaxial regions of PDC, where possibility may exist for the dielectric failure at full power.

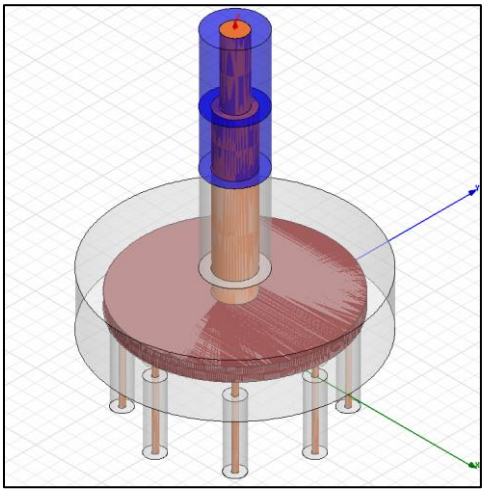


Fig. 4.10: EM model of the PDC for 3D structure simulator

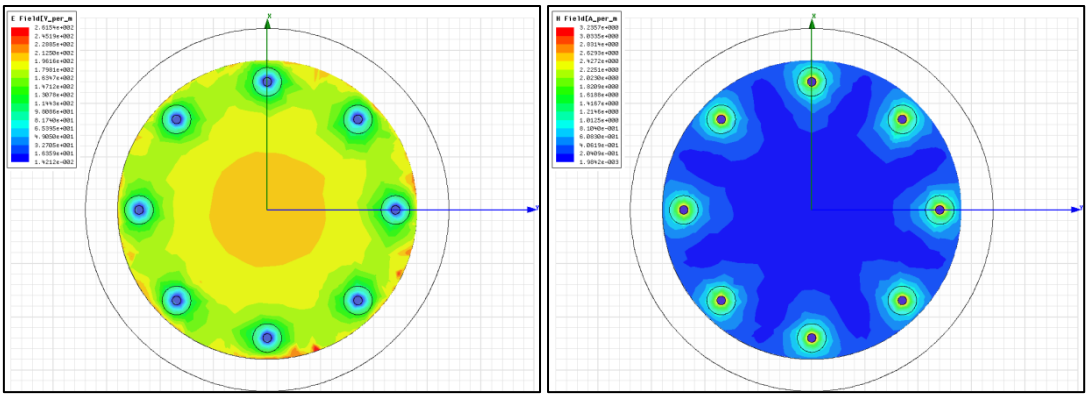


Fig. 4.11: Simulated E and H field patterns for 8-way PDC (352 MHz)

Finally, as an outcome of these design efforts, three PDCs, operating at the centre frequency of 352 MHz, 506 MHz and 704 MHz respectively, were fabricated (Fig. 4.12).

Fig. 4.12: Three 8-way fabricated and assembled power combiners

The major difference in these PDCs is in respect of the length of the respective feed line, decreasing with frequency. The input as well as output ports are similar for all three structures. The selection of a suitable material for these PDCs depends upon various factors [191]. Generally, in an RF rigid component, the electrical requirement for metals is focused on the conductivity, at the given frequency. This, in turn, often includes the skin effect. Copper, aluminium, brass, gold, and silver are considered good, whereas various steel alloys are traditionally accepted only in heavy duty applications. Among these material, brass is a soft and very easily machined material. Unlike many copper alloyed materials it does not produce long chips during machining and therefore the surface quality is much better. Just like beryllium copper, it conducts heat and electricity well. Furthermore, its resistance against atmospheres and various oils is good. Hence, it was selected for PDC fabrication.

4.4.1 Measured Performance of 8-way Dividers/Combiners

For designed PDCs, the necessary low power and high power continuous wave (CW) RF measurements were carried out for validating the design procedure and for demonstrating their suitability for high power operation. At low power the vector measurement, in terms of scattering parameters, was carried out using network analyser E5071B (Fig. 4.13).

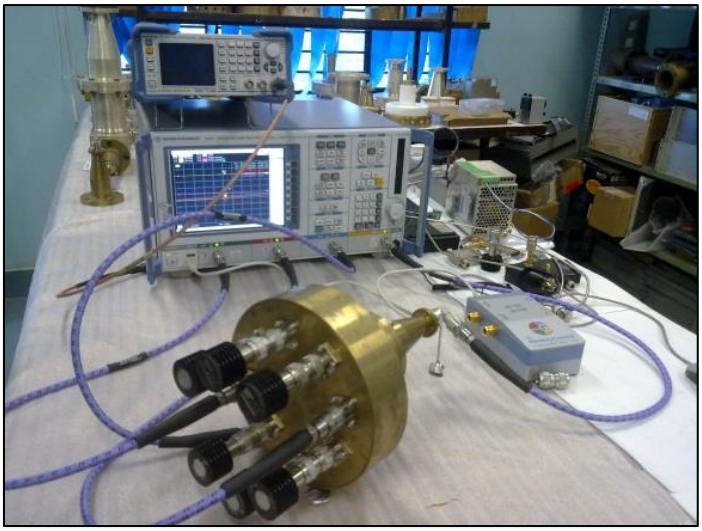


Fig. 4.13: Low power test setup for 8-way power combiners

A 1-5/8” coaxial line to N transition/adaptor, developed in-house, was used for the connection of PDC’s main port to vector analyser’s N type test cable. At high power, the scalar measurement was performed using Rohde & Schwarz NRT power meter, FSP7 spectrum analyser along with in-house developed PA modules (detailed in chapter 2) and directional coupler (to be described in chapter 5). The measured return loss (Fig. 4.14) for all of the PDCs, was better than 20 dB at their respective frequencies.

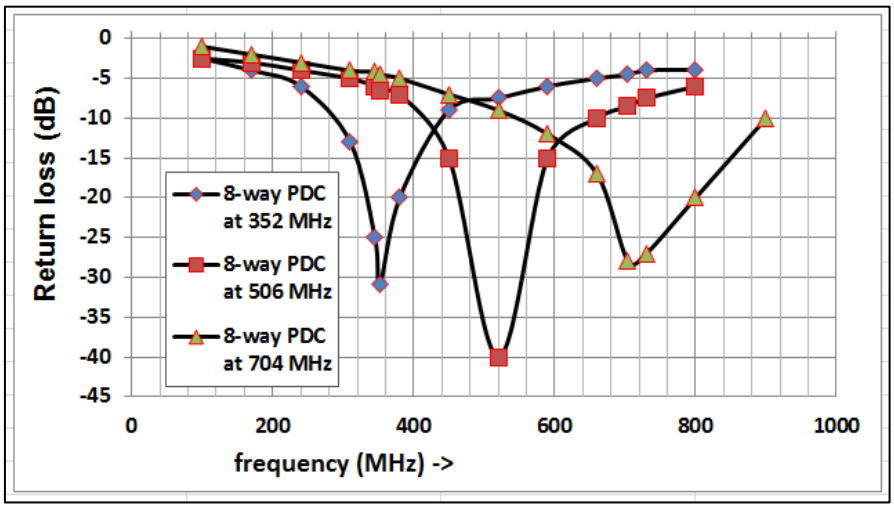


Fig. 4.14: Measured return loss of 8-way power combiners

For design qualification, the calculated and measured value of return loss, transmission coefficient and isolation are compared in Table 4.1. In an ideal PDC, any power fed from the

main port should get distributed equally among branch ports with equal phase difference with respect to input signal. This property for PDC is characterised by s_{coi} ($i = 1,2, \ldots N$). The ideal value of s_{coi} is 9 dB for an 8-way PDC. However, in practice, some amplitude and phase imbalance is observed due to the tolerances in mechanical dimensions of the structure. This imbalance for designed PDCs, as deduced from the measured value of s_{coi} is negligible. The phase deviation of all transmission coefficients is less than 0.7 degree.

Table 4.1: Measured scattering parameters for three 8-way power combiners

Frequency >	**352 MHz**		**505.8 MHz**		**704 MHz**	
Parameter	*Magnitude (dB)*	*Phase (degree)*	*Magnitude (dB)*	*Phase (degree)*	*Magnitude (dB)*	*Phase (degree)*
Return Loss (s_{c00}) The port number zero is summing port.						
calculated	*-35.00*	*-130*	*-33.00*	*149*	*-30.00*	150
Measured	-31.8	-104.51	-36.1	159.50	-28.2	152.25
Transmission coefficient (s_{coi} $i = 1, 2, \ldots .8$)						
calculated	*-9.1*	*150*	*-9.1*	*90*	*-9.1*	*15*
Measured						
s_{co1}	-9.17	154.42	-9.12	95.17	-9.21	16.40
s_{co2}	-9.20	154.43	-9.12	95.07	-9.25	16.02
s_{co3}	-9.10	154.52	-9.12	94.81	-9.20	16.17
s_{co4}	-9.14	154.31	-9.10	95.04	-9.25	16.13
s_{co5}	-9.11	154.30	-9.11	94.92	-9.13	16.67
s_{co6}	-9.07	154.61	-9.09	94.93	-9.25	16.51
s_{co7}	-9.07	154.72	-9.12	95.17	-9.20	16.17
s_{co8}	-9.20	154.43	-9.10	95.04	-9.25	16.13
Measured Isolation (s_{ci1} $i = 2, 3, \ldots .8$) with respect to port 1						
s_{c21}	-14.11	-28.81	-12.00	-49.95	-9.44	-84.33
s_{c31}	-17.79	-82.82	-17.26	-113.77	-17.50	-153.43
s_{c41}	-14.13	-28.92	-11.98	-49.96	-9.43	-84.37
s_{c51}	-17.72	-82.81	-17.26	-113.77	-17.49	-153.09
s_{c61}	-14.15	-28.80	-11.97	-50.03	-9.41	-84.53
s_{c71}	-17.78	-83.21	-17.36	-113.60	-17.47	-154.88
s_{c81}	-14.11	-28.62	-12.00	-50.08	-9.41	-84.53

A symmetric behaviour can be observed from the measured values of the isolation parameter, due to the circular nature of the structure. This behaviour is due to the existence of higher order modes in the radial line when it is driven unsymmetrically. For the ideal case, TEM operation was assumed in all the transmission lines, and as can be seen in the simulated

E-field pattern plotted in Fig. 4.15, this is clearly not the case here. Here, the branch port 1 is driven and all other ports are terminated. It can be deduced that the strongest coupling from port 1 would be to its nearby ports. The minimum isolation decreases from 352 MHz PDC to 704 MHz PDC, perhaps due to same dimensions of circular combining path in all three structures. It is to be noted from (4.1) that for ideal lossless Wilkinson type 8-way combiner without isolation resistor, isolation is 18 dB.

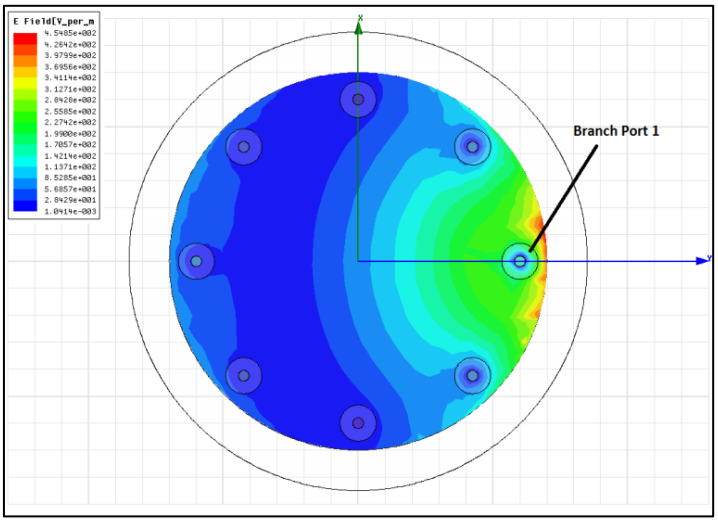


Fig. 4.15: Simulated E-field pattern with port 1 as a driven port

For in-situ insertion loss measurement and graceful degradation testing, two similar 8-way PDCs at 505.8 MHz were connected back to back (Fig. 4.16). Thus one structure performs dividing action, while second one combines divided power. The branch port connections were randomly changed several times. The total (twice of single PDC) worst case insertion loss for this divider-combiner pair was 0.33 dB. Thus, the insertion loss for each 8-way PDC is 0.165 dB, which is very low. The corresponding combining efficiency comes out better than 96%. This value reconfirm negligible phase imbalance measured at the low power. This loss due to mismatch, directly reflects the control over the uniform phase distribution in a radial topology, a feature making this PDC attractive for high power amplifier in particle accelerators, putting less strain over associated control electronics. These PDCs showed the 1-dB bandwidth of 50 MHz .

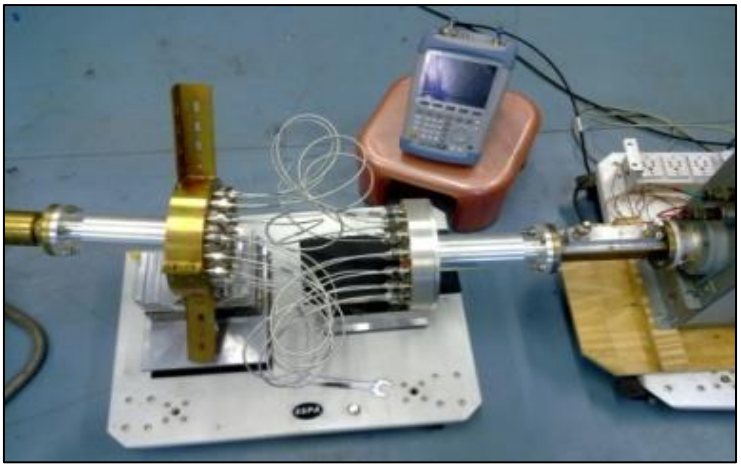


Fig. 4.16: Test setup for insertion loss measurement of RF power combiner/divider

At 352 MHz, 8-way PDC was tested for more than 110 hours, with each test segment stretching nearly 4 hours in time. During this life time testing, no any problem like excess heating or the local hot-spot formation, was observed. For safety purpose, its radiation level was also measured. It was less than 1mW/cm^2, which is much below than the safe limit prescribed [192] in frequency range of 300-800MHz.

4.5 Design and Measurement of 16-way Radial Dividers/Combiners

Having qualified 8-way PDC, it was felt that rather compact and optimized PDC structure capable of combining more number of PAs, is useful. The initial design of the PA using harmonic shorted operating modes, at 300-400 W of RF power, was performed along with the design of 8-way PDC. Afterwards as the power levels of the harmonic tuned PA increased it became important to increase the number of branch ports in power combiner for not only an RF design aimed at reducing power loss but also from the viewpoint of optimizing the design and space requirement. Accordingly, keeping a trade-off between the mechanical size and the output power from a single PA, N was increased from 8 to 16. For this newer topology, a 16-way PDC, operating at the centre frequency of 505.8 MHz and having a topology similar to the 8-way PDC, was designed using the methodology described in section 4.3. The fabricated 16-way PDC is shown in Fig. 4.17 along with its electromagnetic model.

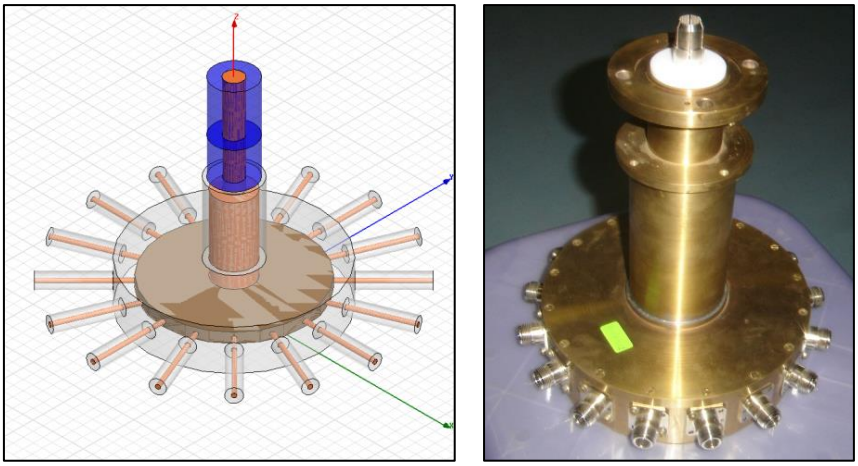
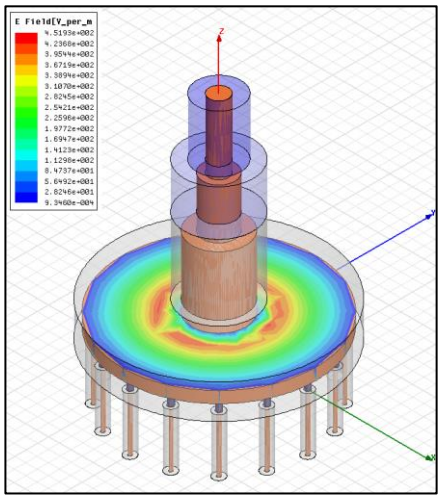


Fig. 4.17: First design of 16-way combiner with radially placed branch ports

In this structure, 16 number of N connector were placed in the radial direction along cylindrical surface of the radial line's curved (outer) conductor. Due to 1-5/8" EIA feed line, this PDC can handle 7 kW of CW RF power in the lower UHF band. However, during RF testing of this PDC, it was noticed that its measured performance was not quite satisfactory due to increased losses (transmission coefficient of -12.6 dB and insertion loss of 0.3 dB).

The careful diagnosis revealed that the imperfect RF contact, between the flat flange of branch port's N type connector and the curved surface of the radial line, was the main reason for its poor measured performance. Further the thickness of the inner conductor of the radial line was only 10 mm, hence a perfect RF contact is difficult to make on the cylindrical surface of this conductor also. This imperfect RF mating developed a parasitic capacitance and consequently the peripheral branch ports are no longer ohmic as assumed in the electromagnetic design and simulation. In order to sort out this problem, the necessary simulation study was carried out by re-orientating branch port connectors, in parallel to the feed line. With this augmentation, two versions of 16-way PDC were designed at 505.8 MHz. The first design is similar to one at 352 MHz, having 1-5/8" EIA main port. In the second design, this port was changed to 3-1/8" EIA to have an increased power handling capacity up to 16 kW at the desired frequency of operation. This can facilitate obtaining more RF power per unit volume in view of the increasing power of LDMOS devices. The EM model of these PDCs

and their design specifications are shown in Fig. 4.18. The fabricated and assembled units are shown in Fig. 4.19.



Design specifications for two 16-way PDCs

Centre frequency: 505.8 MHz

Output port: 1-5/8” EIA flange and 3-1/8”

Input ports number and type: 16, standard N

Maximum output power: 4 kW and 16 kW CW

Combining Efficiency: > 95%

Bandwidth: 10 MHz around centre frequency

Cooling: Self air cooled

Fig. 4.18: EM model and technical specifications of 16-way high power combiners

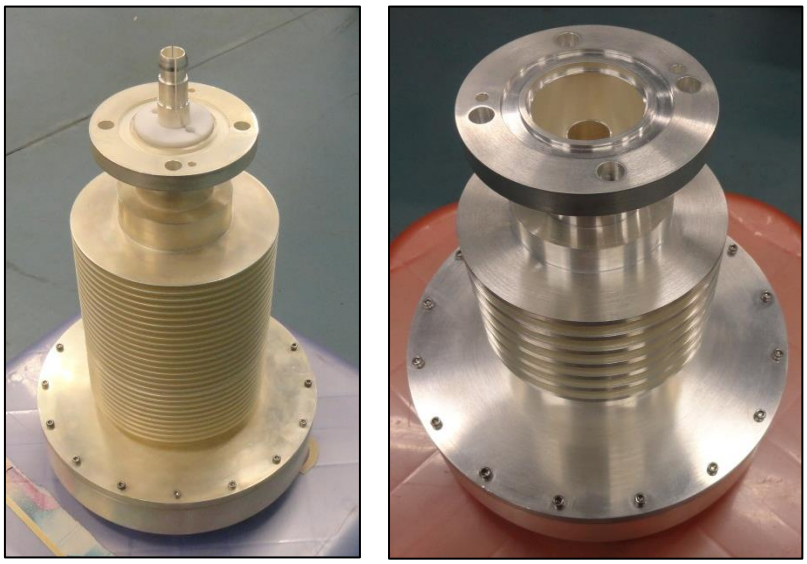


Fig. 4.19: The fabricated PDCs with 1-5/8” (left) and 3-1/8” (right) EIA port

These designs have increased diameter (20 cm) of the radial line’s outer conductor so as to accommodate all 16 N type connectors on its bottom flat surface, similar to the 8-way PDC. These PDCs are useful for characterising high power SSPA, as described in chapter 6. For robust design, it is necessary to dissipate the heat developed due to RF power loss incurred inside the PDC structure and due to the heat conduction from connecting coaxial cables at branch ports. Hence, in this improved design of PDCs, cooling fins were provided

on the outer conductor of the feed line. The inner structure for both of these combiners is quite similar to one used in 8-way combiners.

4.5.1 Measured Performance of 16- way Dividers/Combiners

Similar to earlier measurements made for 8-way PDCs, rigorous RF measurement at low as well as high power were performed using test setup shown in Fig. 4.20, for the designed 16- way PDCs. For the insertion loss measurement, two similar 16-way PDCs were connected back to back (right most part of Fig. 4.20). High power RF source (2 kW SSPA described in chapter 6), used for their testing, was materialised using the 8-way PDCs and harmonic shorted PA modules, qualified earlier.

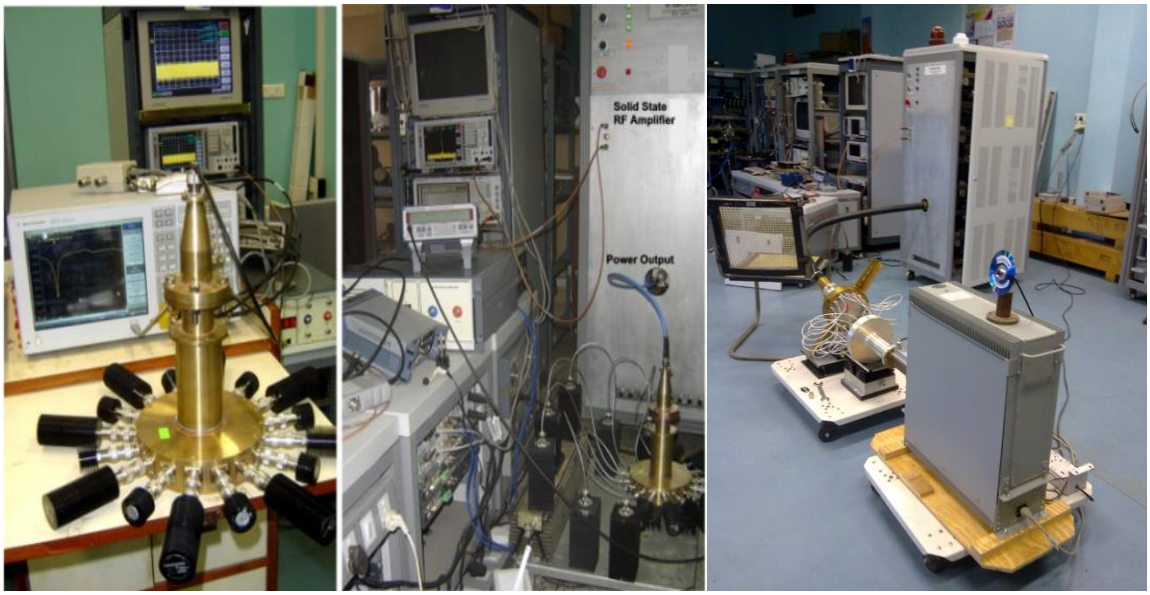


Fig. 4.20: Low power, high power and insertion loss test setup for 16-way combiner

The measured performance of all these PDCs was satisfactory in terms of return loss, bandwidth, insertion loss, transmission coefficient and isolation. In the present report, for brevity, the measurement results are summarised for only the second 16 kW design, having 3-1/8” output port. The calculated and measured values of the return loss for this 16 kW design, as shown in Fig. 4.21, are acceptable and satisfy 20 dB criteria from 492 to 510 MHz. The minima of measured return loss is shifted by 5 MHz from the centre frequency, still it is

below 20 dB. The amplitude and phase of transmission coefficient (s_{coi}) measured using network analyser is shown in doughnut style in Fig. 4.22.

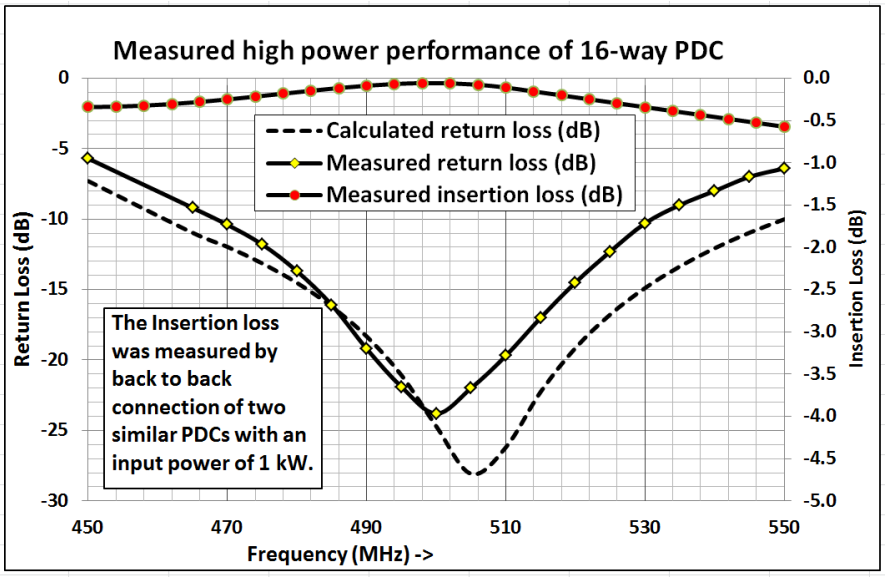


Fig. 4.21: Return loss and bandwidth of 16-way combiner with 1-5/8" output port

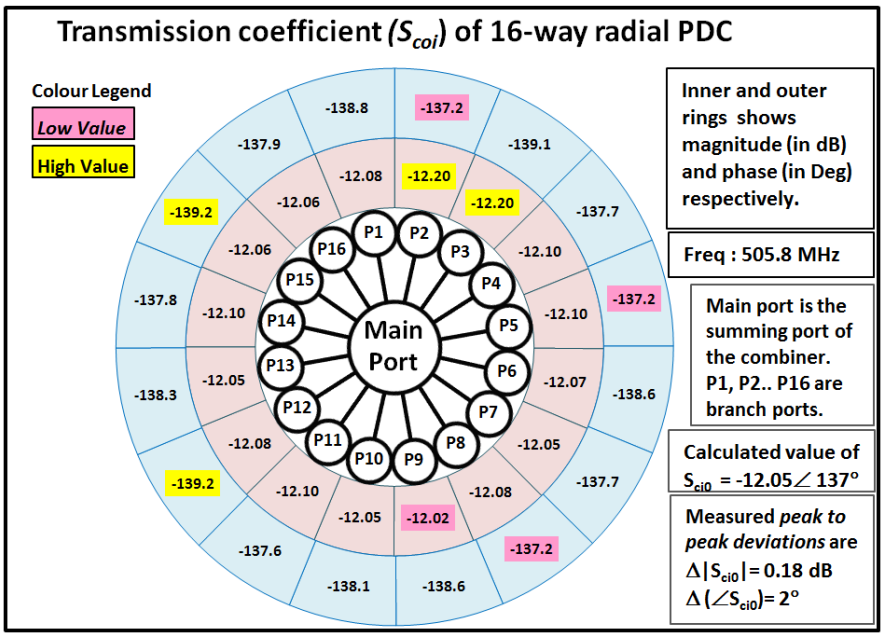


Fig. 4.22: Transmission coefficient of 16-way combiner with 1-5/8" output port

The worst case value of the transmission coefficient from summing port to branch port is -12.2 dB. Thus imbalance is only 0.2 dB in amplitude and nearly 2° in phase. This measured data justifies the use of radial and electrical symmetric combining topology for kW level SSPA. This negligible variation in power coupling allows repeatable design and minimum

loss in the SSPA system incurred due to mismatch/reflection at various junctions of the system. The comparison of measured and HFSS™ result for isolation parameter among branch ports of the PDC is given in Fig. 4.23. Due to PDC's circular structure, this measurement shows a cyclic nature for the isolation pattern. Only few ports attain the value predicted by (4.1). The minimum value of the isolation (about 10 dB) is exhibited among adjacent branch ports (2 and 16), whereas diametrically opposite ports (8, 9 and 10) are moderately isolated (Fig. 4.24).

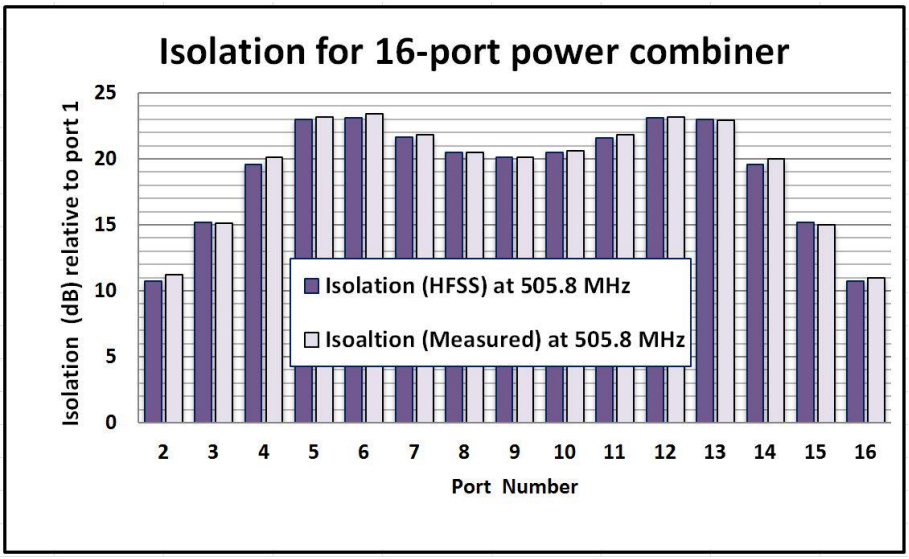


Fig. 4.23: Computed and measured isolation of 16-port combiner at 505.8 MHz

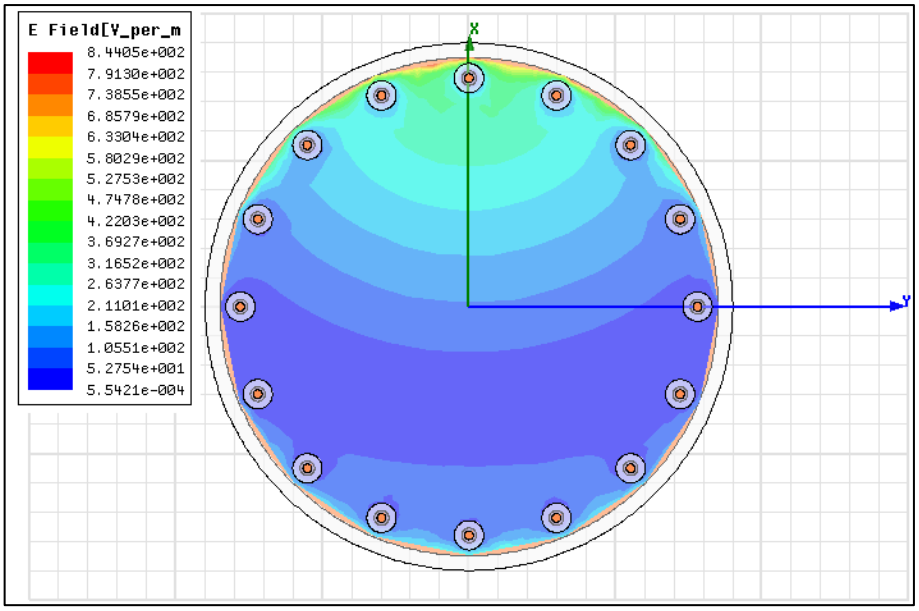


Fig. 4.24: Simulated E-field with port-1 (coinciding with x axis) as driven port

This behaviour is same as described in context with the measured isolation for the 8-way power PDC (Fig. 4.15). The measured insertion loss of the 16-way PDC was nearly 0.1 dB, corresponding to a combining efficiency of 98.9%.Finally, for prolonged time testing this PDC was also tested as a part of the kW level SSPA, as detailed in chapter 6, without any degradation in its performance.

These successful test results verify the suitability of proposed design method at different frequencies and different structures.

4.6 Design and Measurement of 2-way Dividers and Combiners

Apart from N-way PDCs, the binary or 2-way in-phase dividers and combiners are also required at different stages of an SSPA. For the 2-way dividers, required to operate at the low power (< 200 W), two separate modified versions of the Wilkinson topology [89], were implemented. The first version, realised with the semi-rigid coaxial, makes use of a recently reported stub loading [193], for reducing the length of the quarter wave section in a normal Wilkinson divider. The second one incorporates a novel way for loading the T junction of a microstrip Wilkinson divider, using a dielectric resonator. These modifications result in the compact and better designs, respectively. On the other hand, the 2-way combiners are needed for combining very high output power obtained from the multi-way PDCs. Hence, the rigid coaxial line based T junction design was selected, to materialise them. The design description of these low power dividers and high power combiners is detailed next.

4.6.1 Low Power 2-way Dividers

Two modified designs of Wilkinson binary dividers were investigated using the semi-rigid coaxial line and microstrip line, respectively. The starting point, for both of these designs, is an equivalent circuit model [194] of the 2-way Wilkinson divider (Fig. 4.25) and its even-odd mode analysis [195]. This model can be used to find the characteristic imped-

ances and electrical lengths of quarter wave transformers by imposing the matching condition at the input or output ports. In this analysis, it is assumed that the cross-sectional dimensions of the microstrip/strip lines are relatively small with respect to wavelength, so that the effect of the discontinuities caused by corners and junctions on the performance of the designs is neglected [195]. The necessary design equations are

$$Z_{01} = Z_{02} = \sqrt{2} \cdot Z_0 \tag{4.30}$$

$$R_{iso} = 2 \cdot Z_0 \tag{4.31}$$

$$\theta_q = 90° \tag{4.32}$$

The modified versions of this basic topology, for realising two power dividers using semi rigid coaxial line and microstrip line respectively, are presented next.

4.6.1.1 2-way Divider using Semi-Rigid Coaxial Line

The first design of the 2-way divider was performed at 505.8 MHz using the semi-rigid coaxial lines as the quarter wave transformers. Since the centre frequency of the operation for this design is quite low, the length of the transformer was reduced by the stub loaded approach, [193] for Wilkinson dividers. The left part of Fig. 4.25 shows the schematic of the modified equal power division divider, loaded with a capacitive susceptance (C_m) in the middle of the quarter wave transformer. Due to this loading, the characteristic impedance and electrical length of the transformers get reduced, depending upon the selection of the impedance transformation ratio z_r.

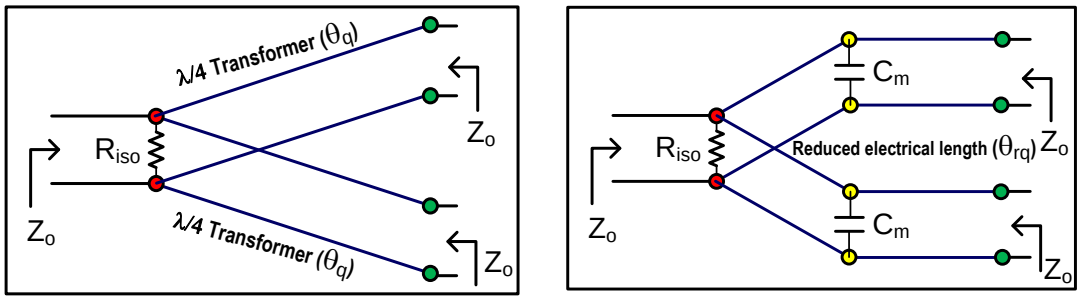


Fig. 4.25: Schematic of a normal 2-way Wilkinson divider (left) and its modified version with stub loading at the middle point of quarter wave transformers (right)

The necessary design equations [193], with reference to Fig. 4.25, are

$$Z_{01m} = Z_{02m} = z_r \cdot Z_{01} \quad (Z_{01} = Z_{02} = Z_0) \tag{4.33}$$

$$B_m = 2\pi f_1 C_m = \frac{1}{Z_{01}} \cdot \left(\frac{z_r^2 - 1}{z_r^2}\right) \sin\theta_q \tag{4.34}$$

$$\tan\left(\frac{\theta_{rq}}{2}\right) = \frac{1}{z_r} \cdot \tan\left(\frac{\theta_q}{2}\right) \tag{4.35}$$

For the present design at (f_1 =) 505.8 MHz, z_r was selected equal to $\sqrt{2}$, in order to use easily available semi-rigid coaxial line, with a characteristic impedance of 50 Ω. With this value of z_r, the electrical length of the transformer get reduced to 70.6°. Also Z_{01m} and C_m comes out equal to 100 Ω and 2.2 pF, respectively. This impedance was achieved by making a series connection of two 50 Ω lines. This design was physically tested by implementing it with UT-141-A line from Micro-coax. The fabricated stub loaded Wilkinson divider is shown in Fig. 4.26. Its outer dimensions are 11.5 X 5 cm^2. The air variable capacitors (0.8-8 pF) from Gigatrim were used as the stub capacitance C_m.

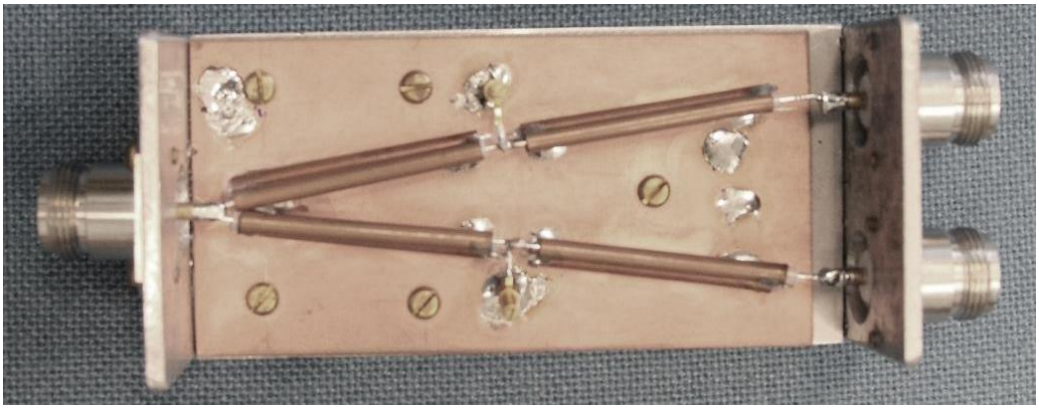


Fig. 4.26: Fabricated stub loaded 2-way Wilkinson divider

The measured values of the return loss and transmission coefficient at the centre frequency of 505.8 MHz, for this fabricated 2-way divider, were -37.2 dB and -3.17 dB, respectively (Fig. 4.27). For comparison simulated results are also plotted here. Measured return loss is lower than calculated one; still it is acceptable for common applications. This divider was tested up to 200 W of RF power at the design frequency satisfactorily.

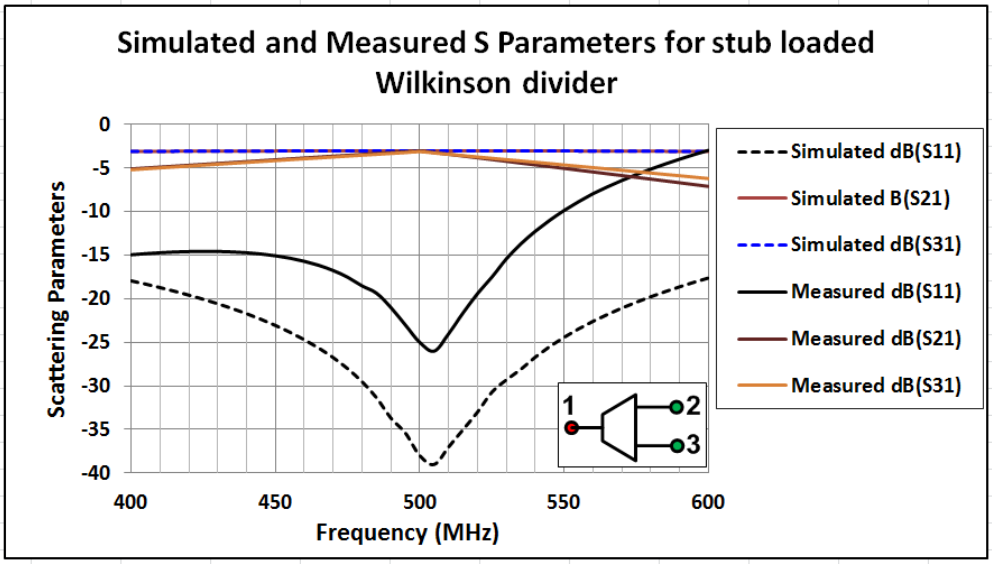


Fig. 4.27: Simulated and measured S parameters for modified Wilkinson divider

4.6.1.2 Dielectric Resonator Loaded 2-way Divider

The second design of the 2-way divider was carried out using a dielectric resonator (DR) loaded microstrip Wilkinson divider. A normal 2-way Wilkinson divider, realized using quarter wave transmission lines, performs satisfactorily at single design frequency. This resonator loading enhance the operational performance of such conventional Wilkinson topology, depending upon the resonator's dimensions and relative permittivity and its physical placement on the divider. Due to its high Q factor, high radiation efficiency and ease of electromagnetic coupling, it can alter properties of a normal power divider so as to make it more versatile for the system. For integration of the DR with a microwave circuit, its coupling with the transmission lines or other DRs needs to be calculated.

A full wave electromagnetic simulation was performed, using HFSS™, to show that an acceptable return loss with equal power division can be achieved at additional multiple frequencies. By changing the magnetic coupling of the resonator with microstrip line, the divider can be made to perform an unequal power division. Also its operating frequencies can be tuned by changing the dielectric constant of the resonator. The measured results show a good agreement with the results of parametric study, developed using full wave analysis.

Before discussing this design, it is necessary to introduce technical advantages of the dielectric resonator, in brief.

4.6.1.2.1 About Dielectric Resonators

In recent years, dielectric resonators [196] have brought immense research interest due to their inherent attractive features like high permittivity, compact size, low conducting losses, ease of excitation and relatively low cost. Due to a breakthrough in the ceramic technology [197] and the flexibility in fabricating the DR in a desired shape, its circuit integration and signal excitation [198] is easier with commonly used transmission lines. Its resonant frequency depends on its dimensions and dielectric constant. It is used in the design of microwave filters [199], antenna [200] and stabilized oscillators. Recently its application was extended for the power divider [201] in whispering gallery modes, useful for many optical and millimetre wave circuits.

It supports resonant modes similar to those in a metallic cavity, but with the electromagnetic field extending beyond the boundaries into the surrounding air region. It also acts as a frequency tuning element because of the internal reflection of electromagnetic waves at its material/air boundary. The most practical configuration of a DR is usually a cylindrical disk. For such shape, with its height less than its diameter, the dominant resonant mode is $TE_{01\Delta}$. The subscript Δ specifies variation less than half cycle, in the axial or z direction. The electric field of a dielectric resonator is contained substantially within the resonator structure in the desired mode of operation. The magnetic fields yielded by dielectric resonators do extend beyond the confines of the resonator structures and into a cavity of a filter in which the resonators are contained. When its height is more than its diameter, the dominant mode is $TM_{01\Delta}$. Its resonant frequency depends upon its dimensions and its dielectric constant. Since, these parameters change with the temperature, it is necessary to use materials that have low coefficients of expansion and relatively temperature-independent dielectric constants. For a

cylindrical DR, operating in $TE_{01\Delta}$ mode, the resonant frequency (f_{dr} in GHz), is given (accurate to 4%) by the following empirical relation [202]

$$f_{dr}(GHz) = \frac{36}{a_{dr}\sqrt{\epsilon_r}}\left(\frac{a_{dr}}{h_{dr}} + 3.75\right) \tag{4.36}$$

Where 'a_{dr}' is the cylinder radius in mm and h_{dr} is the height of the cylinder in mm.

4.6.1.2.2 Dielectric Resonator Loaded 2-way Power Divider

The schematic of a planar Wilkinson two-way power divider, designed to operate at 770 MHz, is shown in Fig. 4.28. Its T junction is loaded with a cylindrical DR. The DR is placed on the substrate, near port 1, so as to magnetically couple microstrip lines, which are meant for equally dividing power among the port 2 and 3. Its placement is controlled by the distance a and the angle θ.

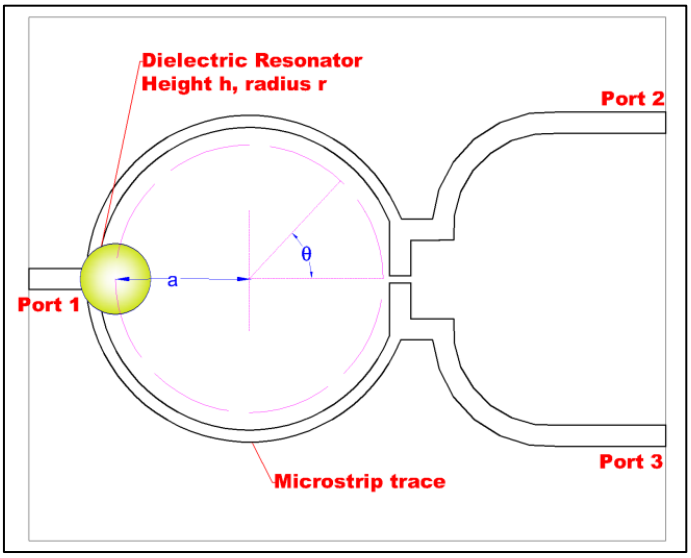


Fig. 4.28: Schematic of dielectric resonator loaded two-way power divider

Initial simulation of this divider was performed without the DR, for calculating its scattering (S) parameters (S_{11}, S_{21}, S_{31}); all in dB. In this designed structure, the microstrip trace widths were calculated as 3 mm and 1.58 mm for the line impedances of 50 Ω and 100 Ω, respectively, for equal power division. These were calculated using the following formula

$$\frac{w}{h} = \frac{2}{\pi}\left[\frac{377}{2Z_o\sqrt{\varepsilon_r}} - 1 - \ln\left(\frac{377}{Z_o\sqrt{\varepsilon_r}} - 1\right) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left\{\ln\left(\frac{377}{2Z_o\sqrt{\varepsilon_r}} - 1\right) + 0.39 - \frac{0.61}{\varepsilon_r}\right\}\right] \quad (4.37)$$

Here ε_r, w and h are the relative permittivity, width of copper trace and the height of the substrate, respectively. The RF substrate TMM4™ having relative permittivity of 4.5 and height (h) of 1.6 mm was chosen for this divider.

Based on the popular criteria of minimum 20 dB return loss, this divider performs satisfactorily ($s_{11} = -41.2\ dB,\ s_{21} = -3.04\ dB, s_{31} = -3.06\ dB$) at a frequency of 770 MHz. Next to this the incorporation of the resonator was carried out. A suitable EM model, prepared using HFSS™ for the simulation, is shown in Fig. 4.29.

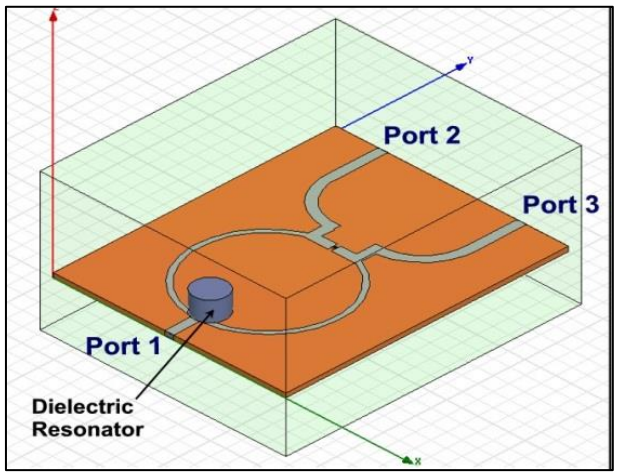


Fig. 4.29: EM model of two-way power divider with dielectric resonator

A full wave analysis of this model was performed in four parts. In the first part, S parameters were deduced for optimum values of a and θ (with reference to) equal to 19 mm and 180°, respectively. This value of a was selected based on the parametric study and the coupling factor calculation [203] for the optimum performance of this divider. The simulated response along with marker table is shown in Fig. 4.30. The power divider is able to operate at three frequencies (f_1, f_2 and f_3), corresponding to three consecutive minimum values of s_{11}, *viz.* 0.69, 1.95 and 3.2 GHz. The return loss, given by s_{11}, is below 20 dB at all these

frequencies. Also the lowest frequency (f_1) is lower, from 0.77 GHz, due to influence of the resonator. The other two parameters s_{21} and s_{31} are nearly overlapped, showing nearly equal power division at these frequencies.

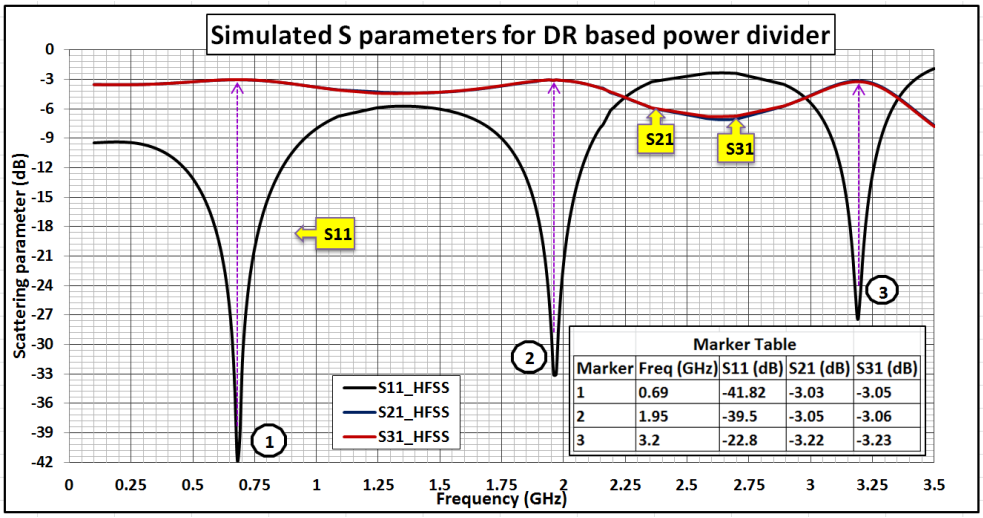


Fig. 4.30: Simulated response of two-way power divider with dielectric resonator

Thus incorporation of the DR with a normal power divider results in its operation at three different frequencies, compared to the earlier case (without DR). These new frequencies can be manipulated by changing dielectric constant (ε_r) of the DR. This manipulation was performed in the second part of the simulation, with values of a and θ equal to 19 mm and 180°, respectively. The simulated S parameters of interest, at three frequencies (f_1, f_2 and f_3), are tabulated in Table 4.2.

Table 4.2: S parameters for different dielectric constant of dielectric resonator

ε_r	f_1 (GHz)	s_{11} (dB)	f_2 (GHz)	s_{11} (dB)	f_3 (GHz)	s_{11} (dB)
27	0.692	-44.2	2.0	-29.1	3.2	-17.6
37	0.690	-41.8	1.95	-39.5	3.2	-22.8
50	0.658	-39.1	1.94	-27.3	3.2	-28.3
78	0.644	-35.7	1.92	-23.1	3.1	-32.4

The tabulated values of ε_r, used in this simulation, were based on the popular DR material available in the market. As observed here, an increase in the value of ε_r, shift the operating frequencies by a few MHz. Except the first case corresponding to ε_r equal to 27, in all other cases, the divider performance is acceptable at these frequencies.

In the third part of this analysis, an effect of the magnetic coupling of DR with two quarter wave microstrip lines was studies by changing distance a at fixed angle (θ) equal to 180°. It can be deduced from the tabulated results (Table 4.3) that the change in the coupling, do not affect divider's primary frequency of operation.

Table 4.3: S parameters for different values of coupling distance (a) in 2-way divider

a (mm)	f_1 (GHz)	s_{11} (dB)	f_2 (GHz)	s_{11} (dB)	f_3 (GHz)	s_{11} (dB)
16	0.77	-36.2	2.1	-14.0	3.3	-8.5
18	0.69	-34.8	1.95	-28.4	3.2	-20.6
19	0.69	-41.8	1.95	-39.5	3.2	-22.8
20	0.69	-33.6	1.95	-33.1	3.2	-12.1

However, the input VSWR and the power division ratio get affected. In this table the first row, corresponding to a value of a equal to 16 mm, refers to very loose coupling. Accordingly, results are nearly same as the one obtained for the divider without a resonator.

In the fourth part of this analysis, change in s_{21} and s_{31} were calculated as θ (azimuthal direction) varies from 0° to 180°, thus changing its placement only in the upper half portion of the symmetric divider geometry. The Simulated data at the lowest frequency (f_1), obtained for different angles for a fixed value of a equal to 19 mm, are given in the Table 4.4.

Table 4.4: S parameters for azimuthal variation of the DR

Angle θ	f_1 (GHz)	s_{11} (dB)	s_{21} (dB)	s_{31} (dB)
160°	0.68	-31.43	-2.90	-3.17
140°	0.68	-26.80	-2.77	-3.34
120°	0.72	-22.70	-2.62	-3.56
90°	0.77	-24.70	-2.60	-3.63
45°	0.8	-35.70	-2.90	-3.20
0°	0.77	-22.20	-3.04	-3.07

The case corresponding to 180° is already discussed with reference to Fig. 4.28. The last row in this table ($\theta = 0°$) results in the placement of the DR near the equi-potential lines (near isolation resistor). For such even mode coupling, the simulation data do not reflect the presence of the DR. For all other cases, an unequal power division takes place, with higher power flowing through the microstrip line tightly coupled with the DR. Apart from this

change, there is a small shift in the frequency f_1. In general, the coupling distance a equal to 19 mm and θ equal to 180° gives optimum performance for equal power division.

Finally, for experimental verification this divider was fabricated and measured to validate the simulated data. A resonator ($h = 7$ mm, $r = 5$ mm, $\varepsilon_r = 37$), prepared by Centre for materials for electronics technology (C-MET) [204], was used with the power divider (Fig. 4.31). This structure measures 9 X 6 cm^2.

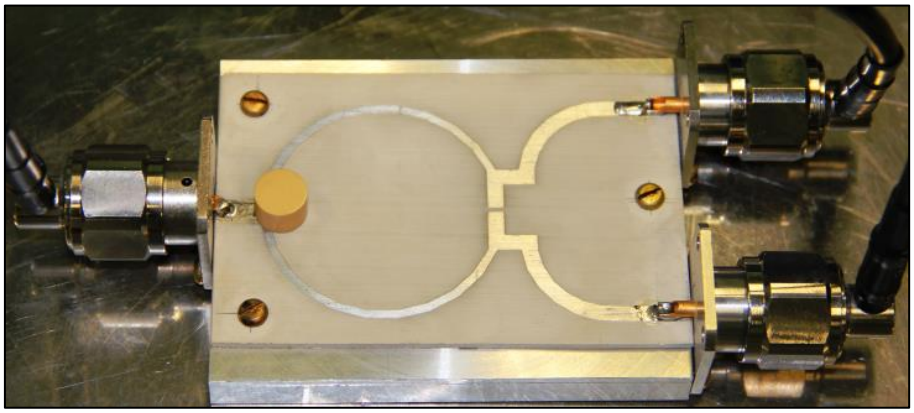


Fig. 4.31: Fabricated two-way power divider with dielectric resonator loading

For equal power division the microstrip trace widths were calculated as 3 mm and 1.58 mm for 50 Ω and 100 Ω, respectively. The substrate TMM4™, having a dielectric constant of 4.5 and height of 1.6 mm, was chosen for this circuit.

The measured results for this power divider, with and without the dielectric resonator (positioned at $a = 19$ mm and $\theta = 180°$), are shown in Fig. 4.32. The parameter s_{11} for the divider, without DR, has the value of -12.7 and -7.25 dB at 2.1 GHz and 3.34 GHz (marker 2 and 3), respectively. However, it fails to qualify 20 dB criteria at these frequencies. Thus divider without DR is operational at the single frequency of 0.76 GHz (marker 1). This measured value is slightly lower from the simulated value (0.77 GHz). The divider, with DR, shows three operational frequencies at 0.688, 1.98 and 3.152 GHz respectively. The power division as well as return loss is quite satisfactory at these frequencies. This modified divider

may explore the possibility for dual/tri band operation, often encountered in particle accelerator RF systems like 325 MHz and 650 MHz in RF system of SNS project.

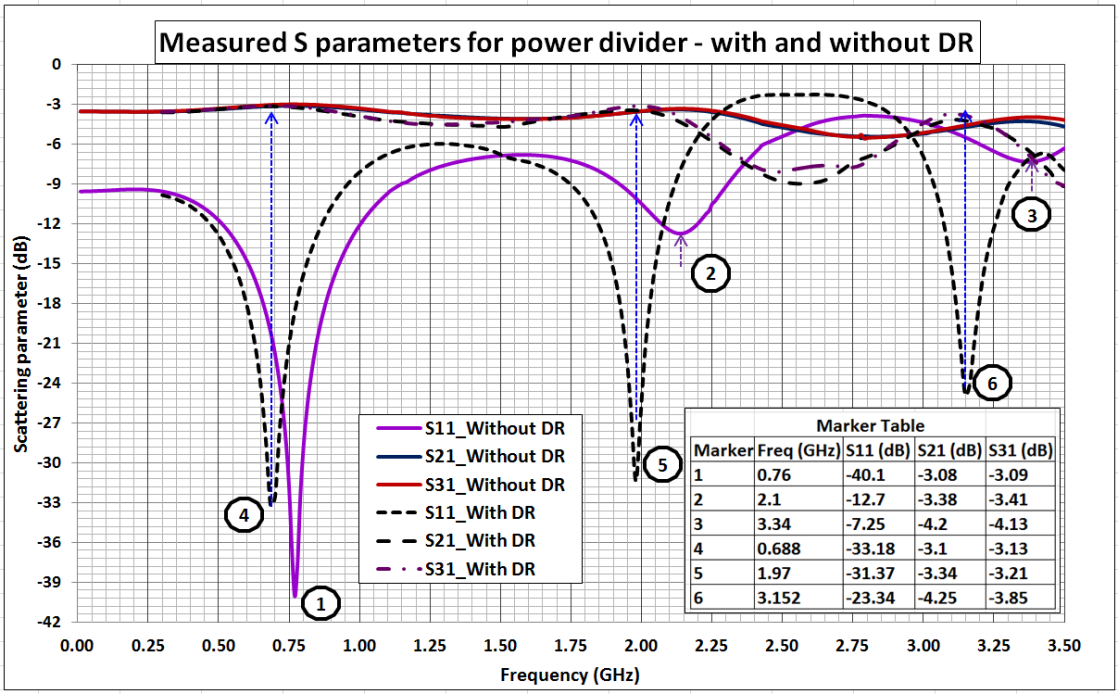


Fig. 4.32: Measured response of power divider with and without dielectric resonator

4.6.2 High Power 2-way Combiners

The 2-way high power combiners were designed as a T-junction of rigid coaxial lines suitably matched at the combined port. This approach keeps the overall structure compact and easy to fabricate due to the impedance matching required only at the combined port. The T-junction, basically, combines the incoming signals according to the inverted ratio of the impedances at the output ports. If the transmission lines used for the realization are assumed to be lossless, the T-junction too becomes a lossless three-port structure. As a consequence such junctions cannot be simultaneously matched at all the ports while simultaneously ensuring isolation between them. In the present design, an approximate equivalent model (Fig. 4.33) of the combiner was developed. It consists of a junction of three transmission lines with a parallel-connected lumped susceptance B. Such a reactance accounts for the fringing fields and the higher order modes arising from the discontinuity effects at the junction. The

impedance Z_{b1} and Z_{b2} (Fig. 4.33) are equal to the system impedance Z_o in order to provide equal power division. The resulting impedance Z_{TJ} needs to be matched to the system impedance Z_o with the help of impedance matching section. For the present narrowband application, this matching was accomplished with the help of cascaded coaxial line sections, instead of Wilkinson type quarter wave sections, resulting in overall compact structure. This combiner does not provide any isolation between its branch ports. However, this isolation problem is alleviated in an integrated SSPA system, due to the presence of the PA circulators.

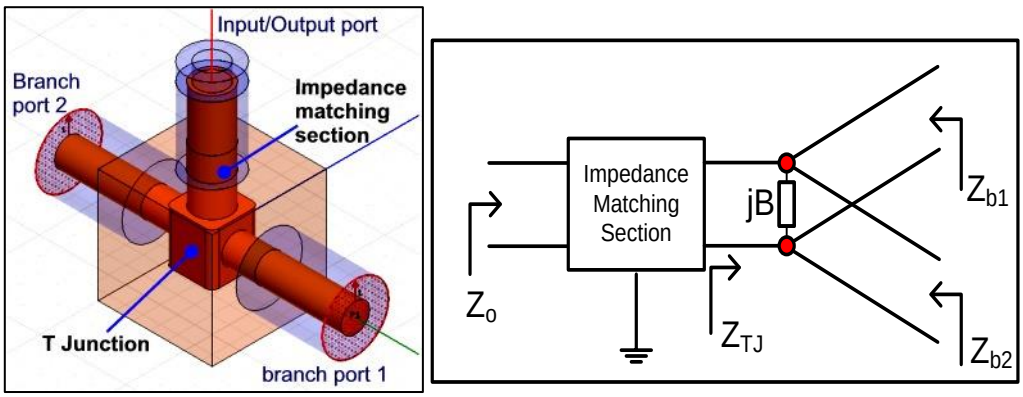


Fig. 4.33: T junction schematic for 2-way combiners

Using this design principle, three types of 2-way combiners were designed at the centre frequency of 505.8 MHz, as shown in Fig. 4.34.

Fig. 4.34: Three 2-way combiners designed at 505.8 MHz

Each one has a similar topology but different dimension and coaxial ports, for different power handling capability. The rightmost combiner (marked F2C) is meant for handling output power up to 20 kW. It has 3-1/8" EIA port at its inputs as well as at output. Rest of the two combiners (G and H) are with 40 kW and 65 kW of power capability, respectively. Both of these combiners have a 6-1/8" EIA output port. Their role becomes more evident in chapter 6. Their measured return loss and power combining ratio are shown in Fig. 4.35.

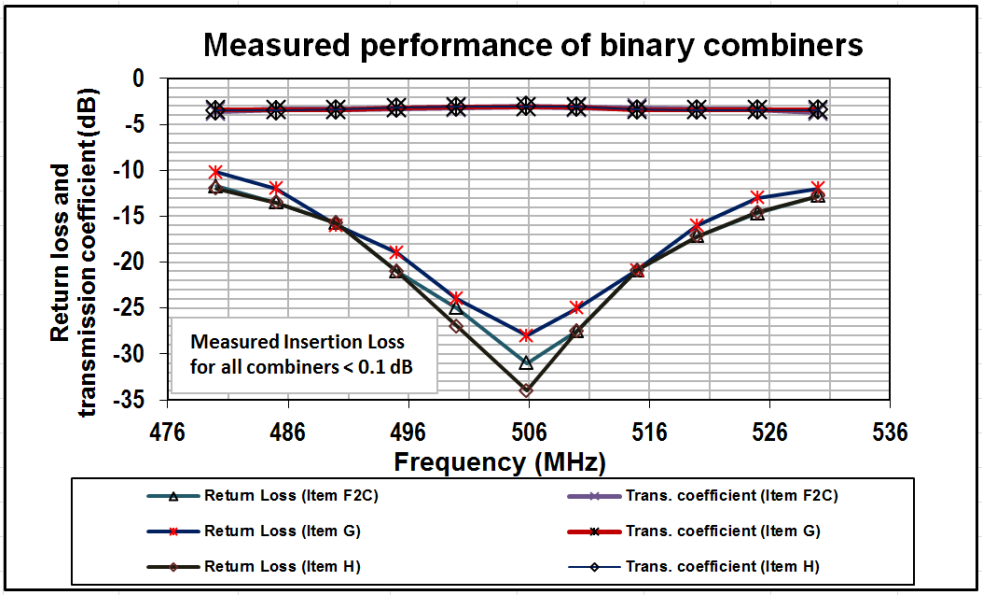


Fig. 4.35: Measured return loss and coupling for all 2-way combiners

Both of these parameters are quite satisfactory for the system integration purpose. The power combining ratio is overlapped due to the similar performance exhibited by these combiners around the centre frequency of 505.8 MHz. They were tested at high power of 2 kW without any degradation in the performance. Their insertion loss, measured by back-to-back connection was less than 0.1 dB at the centre frequency.

In this chapter, the theoretical design and experimental work on high power radial combiner, required for solid state power amplifiers, is presented. The design of multi way combiner makes use of rigid mechanical structure comprising of a parallel slab (stripline type) radial line and coaxial transmission line. A simplified calculation of radial line impedance using segmentation approach is performed, followed by high frequency electromagnetic

simulation. Absence of external tuning mechanism and isolation resistor make this design repeatable, economic, reliable and mechanically friendly without degrading performance. Successful development of 8-way, 16-way and binary combiners at different frequencies paves the way towards its implementation as a workhorse for divide and combiner strategy adopted in RF power source, based on cutting edge technology of solid state devices. All these features are desired for using PDC with SSPA, for powering superconducting accelerating structures, operating in the frequency regime intended for particle accelerator.

Chapter 5. High Power Directional Coupler

Directional couplers are often used in the RF systems as a plug-in component for the measurement of high power RF and microwave signal. It couples a specific proportion of the power travelling from one port in the main transmission line out through another port. Along with the signal coupling, it should present least perturbation in the main transmission path with the minimum insertion loss and a good VSWR. It is a three-port or a four-port structure with the directional coupling of the power. It finds many applications in RF design ranging from the through-line power sensors to the transmitter's automatic levels controls. A variety of designs for the coupler are available in the literature, including strip-line/microstrip couplers, waveguide couplers and coaxial configurations. The first one, using the planar topology [205], has attractive characteristics, useful for a variety of applications. But it is affected by significant losses and has low power-handling capabilities. Due to the harmonic/spurious response measurement, high power amplifier requires a coupler with broad-band and high-power characteristics. The waveguide Bethe-hole couplers [206] have been used in high-power applications but they suffer from their limited bandwidth. The coaxial structures seem a better choice owing to their low losses. Their TEM (or quasi-TEM) field configurations ensure a zero cut-off frequency and high power-handling capabilities, with respect to planar circuit based couplers. In order to obtain a coaxial structure having bandwidths competitive with the strip-line and microstrip coupler, it is necessary to properly control the variation of the coupling factor along the propagation direction. The scope of this work was to identify a directional coupler structure with high power handling, without using any planar part, for achieving a coupling coefficient in the range 40 to 50 dB, and having a repeatable performance. In this chapter, the design theory and physical implementation of different

coaxial directional couplers, required for the RF signal sampling at different junctions of the multi-stage SSPA system, is described. These couplers were designed to cover a frequency range from 300 to 700 MHz with varying power handling capability.

5.1 Important Parameters of Directional Coupler

The basic block diagram of a directional coupler is shown in Fig. 5.1. It is described by a normal 4X4 scattering parameter matrix. The power (P_1) fed at the input port, is coupled through the port 3 by a factor of $|s_{31}|^2$. The remaining power $(1 - |s_{31}|^2)P_1$ comes out of the output port 2. The transmission path formed by port 1 and port 2 is the main path whereas, the coupled and isolated ports (port 4) are part of the auxiliary line. In an ideal case no power should come out of the isolated port. It is generally connected to a matching load.

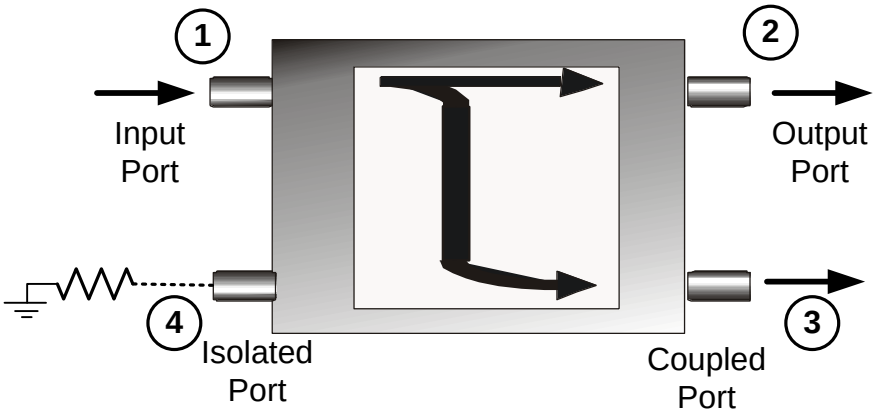


Fig. 5.1: Basic block diagram of a four port directional coupler

Few useful parameters, for characterizing the directional coupler, are defined below.

- Power Coupling (C): The coupling value is a ratio of the coupled output power to the input power, in dB (with all other ports being matched terminated). Or

$$\mathrm{C(dB)} = -10\log_{10}\left[\frac{P_3}{P_1}\right] = -20\ \log_{10}[|s_{31}|] \tag{5.1}$$

It is a primary specification of the directional coupler. Higher the value of the coupling in dB, weakest is the coupled output power from the coupled port.

- Isolation (I): It is a ratio of the power at the isolation port to the input power, in dB (with all other ports being matched terminated). This value indicates how well *isolated* the isolation port is. The higher the isolation, the better it is. Mathematically:

$$\mathrm{I(dB)} = -10\log_{10}\left[\frac{P_4}{P_1}\right] = -20\log_{10}[|s_{41}|] \tag{5.2}$$

- Directivity (D): It is a ratio of the power at the coupling port to the power at the isolation port, in dB (with excitation at port 1 and all other ports being matched terminated). This value indicates how effective the device is *directional* in coupling energy into the correct port. It is optimized by balancing the contributions from the electric and magnetic field components of the RF signal. Higher the directivity the better it is.

$$\mathrm{D(dB)} = 10\log_{10}\left[\frac{P_3}{P_4}\right] = 20\log_{10}\left[\frac{|s_{31}|}{|s_{41}|}\right] \tag{5.3}$$

The directivity, coupling and isolation (all in dB) are related as:

$$\mathrm{D} = \mathrm{I} - \mathrm{C} \tag{5.4}$$

- Insertion loss (IL): It is a ratio of the input power to the power at the through port, in dB. It indicates how much power the signal loses as it travels from the input to the output port.

$$\mathrm{IL\ (dB)} = 10\log_{10}\left[\frac{P_1}{P_2}\right] = -20\log_{10}[|s_{21}|] \tag{5.5}$$

- Coupling loss (CL): The coupling loss indicates the portion of the mainline loss that is due to the coupling of a fraction of the input power into the coupling port. In dB it is given as

$$\mathrm{CL\ (dB)} = 10\log_{10}[1 - |s_{31}|^2] \tag{5.6}$$

- Average Power: It is the maximum CW power level which may be applied to the coupler without altering its characteristics or causing any potential damage to it. This

power ratings, is usually specified for both CW power and peak pulse power, in both the forward and reverse directions.

5.1.1 Importance of Directivity

The directivity of a coupler is critical to the accuracy of various power measurements. When high measurement accuracy is required, the degree to which the auxiliary line is isolated from the load is of particular importance. In power measuring application, where the absolute magnitude of the coupled sample has a significant value, the reverse coupling into the auxiliary line will alter the magnitude of this sample, resulting in measurement error. This error, from the reflected power can be severe when the directivity is not adequate. Thus, the poor directivity causes an inaccurate power monitoring at the coupled and isolated ports by leaking the forward and reflected signals into one another's path. It is better to have the directivity in the range of 25 to 40 dB or better. For high power couplers, directivity achieved is not more than 20-30 dB while for the low power coupler directivity up to 30-40 dB can be achieved easily. A coupler's directivity cannot be better than the return loss of the terminations connected at the coupled and isolated ports. Further, with the finite directivity any impedance mismatch at the port 2 also affects the accuracy of the measurement. Hence, care needs to be taken to provide a good impedance match at all four ports of the coupler for the forward power measurement. For reflected power measurement, since there will be mismatch at the through port 2, use of an additional auxiliary line is preferred. Such arrangement can be materialised by a dual directional coupler. The error in the forward and reflected power measurement, due to the finite directivity of the directional coupler and mismatch at its port 2, can be estimated assuming its bi-directional nature. For a reasonably matched coupler with a loose coupling ($|s_{31}| << 1$ so $\sqrt{1-|s_{31}|^2} \approx 1$), the circuit can be represented by the signal flow graph, as shown in Fig. 2.4. The condition $|s_{31}| << 1$ is easily fulfilled for high power

(kW level) coupler with the value of coupling 40 dB onwards. The directional coupler provides a sample, V_i, of the incident wave and a sample, V_r, of the reflected wave. The realistic directional couplers, however, have finite directivity, which means that both the incident and reflected powers will contribute to both V_i and V_r, leading to an error. Combining the main reflected power with the directivity reflected power cannot be done by a simple addition, but rather the powers must be converted to voltages that are combined vectorially.

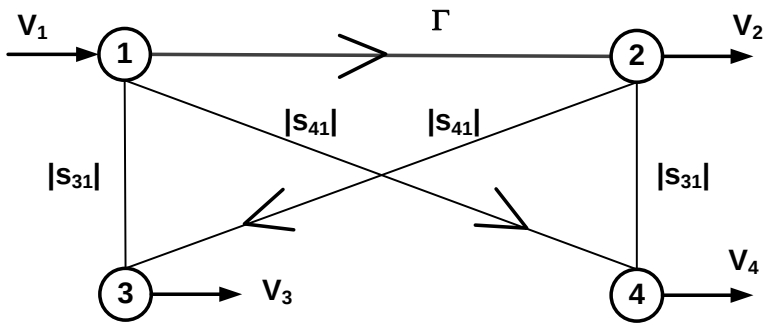


Fig. 5.2: Signal flow graph for bi-directional coupler

If a unit incident wave is assumed from the source, inspection of the signal flow graph leads to the following expressions for V_3 and V_4.

$$V_3 = |s_{31}| + |s_{41}|\,\Gamma e^{j\theta_1}$$

$$V_4 = |s_{41}| + |s_{31}|\,\Gamma e^{j\theta_2}$$

Where Γ is the reflection coefficient as seen outside at port 2, and θ_1 and θ_2 are unknown phase differences through the circuit. Because the phases of the voltage vectors are unknown, the extreme cases of combining in or out of phase must be assumed. Therefore,

$$V_3|_{max} = |s_{31}| + |s_{41}|\,|\Gamma| \tag{5.7}$$

$$V_3|_{min} = |s_{31}| - |s_{41}|\,|\Gamma| \tag{5.8}$$

$$V_4|_{max} = |s_{41}| + |s_{31}|\,|\Gamma| \tag{5.9}$$

$$V_4|_{min} = |s_{41}| - |s_{31}|\,|\Gamma| \tag{5.10}$$

The maximum and minimum values of the magnitude of $\left|\frac{V_4}{V_3}\right|$ can be written as

$$\left|\frac{V_4}{V_3}\right|_{\substack{max \\ min}} = \frac{|\Gamma| \pm \frac{|s_{41}|}{|s_{31}|}}{1 \mp |\Gamma| \frac{|s_{41}|}{|s_{31}|}} \tag{5.11}$$

The maximum value of $\left|\frac{V_4}{V_3}\right|$ results, when the positive sign is used in the numerator and the negative sign is used in the denominator. For a coupler with infinite directivity this reduces to an ideal result of $|\Gamma|$. Otherwise, a measurement uncertainty of approximately $\pm(1 + |\Gamma|)\frac{|s_{41}|}{|s_{31}|}$ is introduced. Good accuracy thus requires a coupler with a high directivity, preferably greater than 40 dB. However, to retain such accuracy, the impedance offered at the coupled and isolated ports should provide a return loss better than 40 dB.

An alternate solution to the poor return loss of the connecting instrument is a dual directional coupler (Fig. 5.3). It consists of two auxiliary lines coupled to one main (through) line, or two single-ended couplers connected back-to-back. In each auxiliary line, power at the isolated port is dumped in a dummy matched load, having very good VSWR.

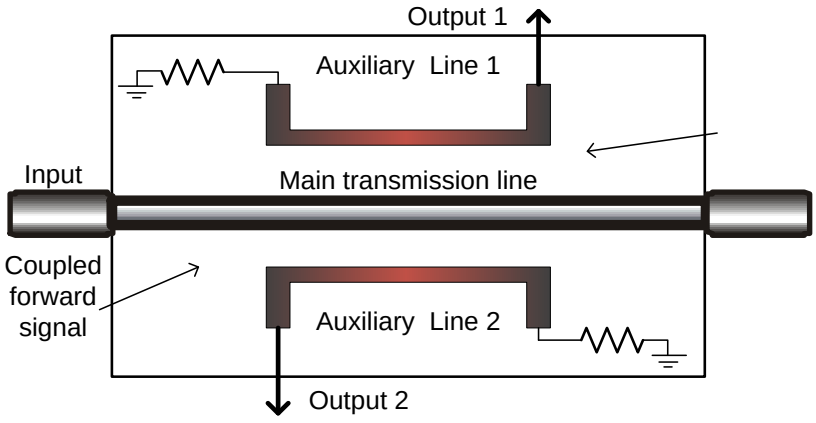


Fig. 5.3: A dual directional coupler

In practice, most of the directional power meter measures power with an accuracy of 5%. For a reasonable value of $|\Gamma|$ of 20 dB, the error for 35 dB directivity is 2%. This is good enough if one wants to keep the accuracy better than the uncertainty of the power meter. As a

thumb rule, less than 1 dB error in the return loss, to be measured, will result when the directivity is 20 dB greater than this return loss.

5.2 Theory of Designed Couplers

For directional sampling and measurement of very high power in the UHF range, a weakly coupled coaxial type of directional coupler, is a reliable and cost-effective solution. Due to the TEM coupling mode, such couplers show an excellent performance in terms of the directivity, insertion loss, bandwidth and EMI shielding. For high power SSPA system, such features are desired for its efficient operation. It is well known that a pair of parallel coupled lines (for main as well as auxiliary lines) achieves the maximum coupling in a TEM system, when they are a quarter wavelength long (λ/4) [207]. Additionally, broad-banding may be achieved by cascading such several λ/4 sections, coupled together. However, it is difficult to realize such coupler due to its excessive physical dimensions at UHF. Hence, this design, using coaxial lines, needs to be modified. The present solution, proposed for high power and weakly coupled design, is a rigid structure using rectangular and non-symmetrical coaxial transmission lines. The coupling mechanism is similar to one suggested by Tepatti [208], where, a thin metal diaphragm with a properly shaped aperture was inserted between the two cylindrical rods forming inner conductors of longitudinal main and auxiliary coaxial lines (Fig. 5.4) respectively. The RF signal is loosely coupled with the help of this aperture, throughout the working frequency range. This design helps reducing the length of the coupler in order to make it realizable in the desired frequency range of 300-700 MHz. The non-symmetrical cross sections of these coaxial lines result in their unequal characteristic impedances. The use of non-standard cross section of coaxial cable, having a rectangular outer conductor and a circular inner conductor, is effective to overcome mechanical constraints posed by the standard dimensions of the lines and connectors. The coupling can be adjusted

by the width of the mechanical diaphragm, sandwiched between the flat surfaces of these rectangular outer conductors. Thus, the overall design, being very compact and repeatable in performance, results in a tight control over the coupling and directivity. Also, it provides an ease of fabrication and does not need any additional mechanical shielding/housing.

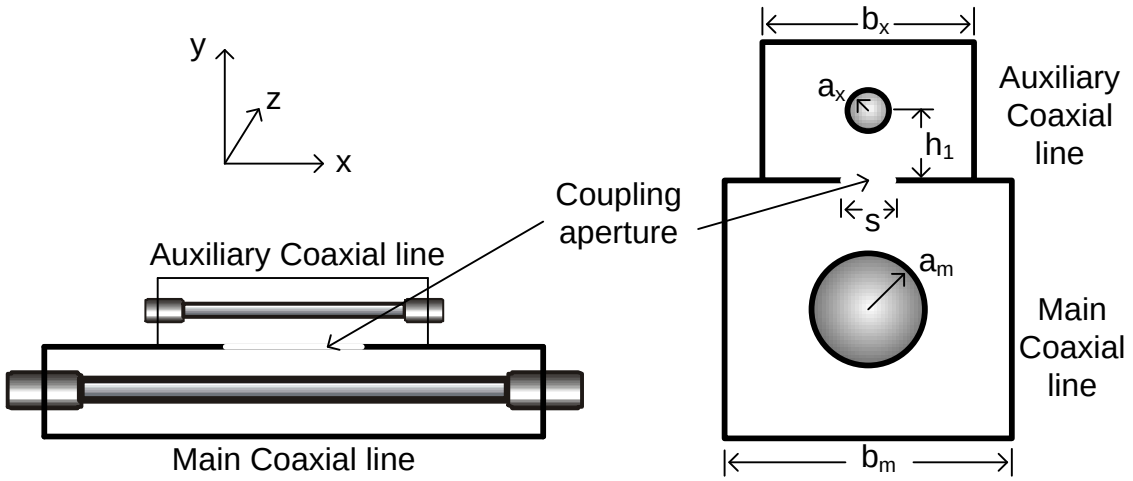


Fig. 5.4: Aperture coupled coaxial directional coupler with its enlarged cross section

The design calculation of the proposed coupler is based on the quasi static assumption that decouples the transversal and longitudinal problems. The necessary analysis [209], provides the coupling factor and the characteristic impedances as a function of the structure dimensions. The characteristic impedance of a coaxial cable with the square outer conductor is given [210] by

$$Z_{0,sq} = 138 \log_{10}\left(\frac{1}{\cos(\pi/8)} \cdot \frac{b_m}{a_m}\right) \tag{5.12}$$

where b_m is the side of the square, and a_m is the diameter of the inner conductor. The cross section of main line and auxiliary line is shown in Fig. 5.4. Both of these lines can be realised with rigid metallic structure. The absence of any printed circuit structure allows the design of these couplers with excellent repeatability.

For uniformly coupled symmetric lines, the mid band voltage coupling factor k_c can be expressed [211] in terms of even and odd mode impedances (Z_{oe} and Z_{oo}), as

$$k_c = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \tag{5.13}$$

However, due to a lack of the symmetry between the conductors in the present design, this description must be replaced by a capacitance matrix, as

$$C_{DC} = \begin{bmatrix} C_A + C_{AB} & -C_{AB} \\ -C_{AB} & C_B + C_{AB} \end{bmatrix} \tag{5.14}$$

Here C_A and C_B are the per-unit length capacitance associated to the inner conductors and C_{AB} is their per unit length mutual capacitance. Various numerical techniques can be used to determine the accurate primary parameters of the couplers. In this work, the full wave EM analysis has been used for the design of the couplers. The coupling coefficient may be derived from the classic formulation by Cristal [211].

In the present design, as the main and auxiliary coaxial lines are non-uniformly coupled, an additional calculation is required as a part of the longitudinal design procedure. Such non-uniform coupling arises due to the tapered or diamond shaped profile of the aperture. The aperture shape corresponds to the desired longitudinal profile of the coupling factor. The aim of this procedure is to build an approximation of target coupling factor by varying along a geometrical parameter (e.g., the diaphragm aperture or the distance between the inner conductors). This longitudinal design procedure is based on the following equations [212] .

$$|s_{31}| = j2\pi \frac{l}{\lambda} \int_0^l k_c(z).\, e^{-4\pi \frac{l}{\lambda} z}\, dz \tag{5.15}$$

Here, l is the length of the coupler in z direction and λ is the guide wavelength. The coupling factor in longitudinal direction can be assumed to be a polynomial with some unknown coefficients. Based on the parametric study, these coefficients can be determined for a given value of coupling along the z direction.

5.3 Experimental Investigation

For the present requirement of measurements at different power levels, three high power directional couplers were designed and experimentally verified. They shares the similar type of rigid rectangular structure, but differ in their power handling capability and aperture profiles, corresponding to different coupling coefficients in the frequency band of 300-700 MHz. Due to the sampling of RF power level in 1 kW to 20 kW (CW) range, minimum coupling factor was set to be 40 dB. The input and output connectors for the main transmission line were selected in accordance with the power handling capability of this line. For coupled and isolated ports in the auxiliary line, the standard SMA and N type of connectors were used. All of these couplers should have very low insertion loss (<0.1 dB) due to their high power handling. It must be possible due to short length of coaxial lines used therein. The technical specifications of these directional couplers are given in Table 5.1.

Table 5.1: Technical specifications of three designed directional couplers

Directional coupler type	**Maximum forward power**	**Coupling factor (mid band)**	**Main line connectors**	**Minimum directivity**	**Minimum return loss (mid band)**
A- Low power design	1 kW CW	40 dB	N type	30 dB	25 dB
B- Medium power design	5 kW CW	50 dB	1-5/8” EIA	28 dB	25 dB
C- High power dual coupling design	20 kW CW	50 dB	3-1/8” EIA	28 dB	25 dB

The structure for the type A and B is essentially similar, except 1-5/8” EIA flange connection, instead of N connectors, at the output as well as the input ports. However, the type C (20 kW coupler) is a dual directional coupler, with 3-1/8” EIA flange at input and output ports. Using these specifications computation of various dimensions for couplers’ structures was carried out. The final design optimization with various discontinuities was carried out using full wave Electromagnetic (EM) analysis software HFSS™. The Electro-Magnetic

model, prepared for the 1 kW coupler, is shown in Fig. 5.5. As described in the design theory, its main line is formed by a coaxial line having a square outer conductor and a cylindrical inner conductor.

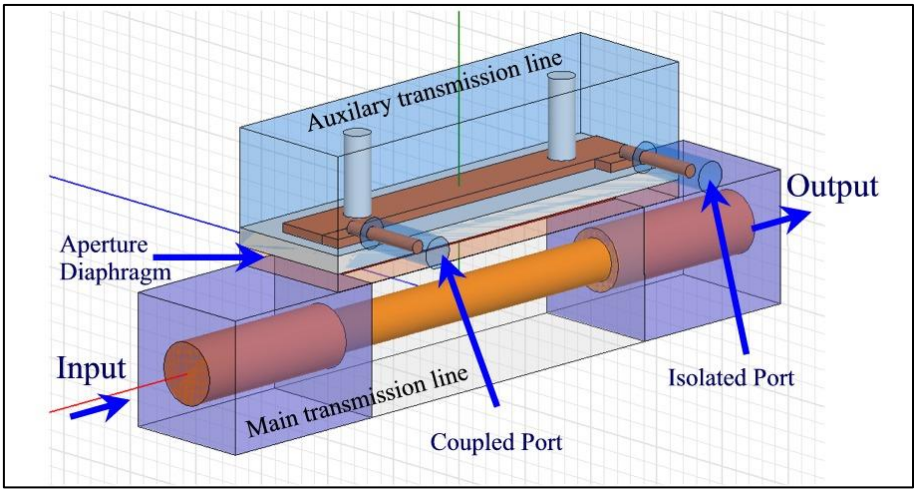


Fig. 5.5: EM model of 1 kW directional coupler

The auxiliary line was realised using a suspended slab/strip line with dielectric posts. The coupling aperture, realised as a metallic diaphragm, was inserted between the broad sides of the outer conductors of these two lines. The final length of the optimised structure was 60 mm. Two SMA connectors were used for providing interface at the coupled port as well as the isolated port. The input and output ports of the main line were interfaced using the standard N type connector. Necessary impedance matching was provided at both ends of the main transmission line with the help of coaxial sections.

For this coupler, the simulated results like return loss, insertion loss, coupling and isolation are shown in Fig. 5.6. The return loss is at minimum (-66 dB) at 500 MHz. It maintains a value of -35 DB throughout the frequency band of 200-800 MHz. Its simulated insertion loss is very low. For all of these couplers, silver material was taken for the simulation purpose.

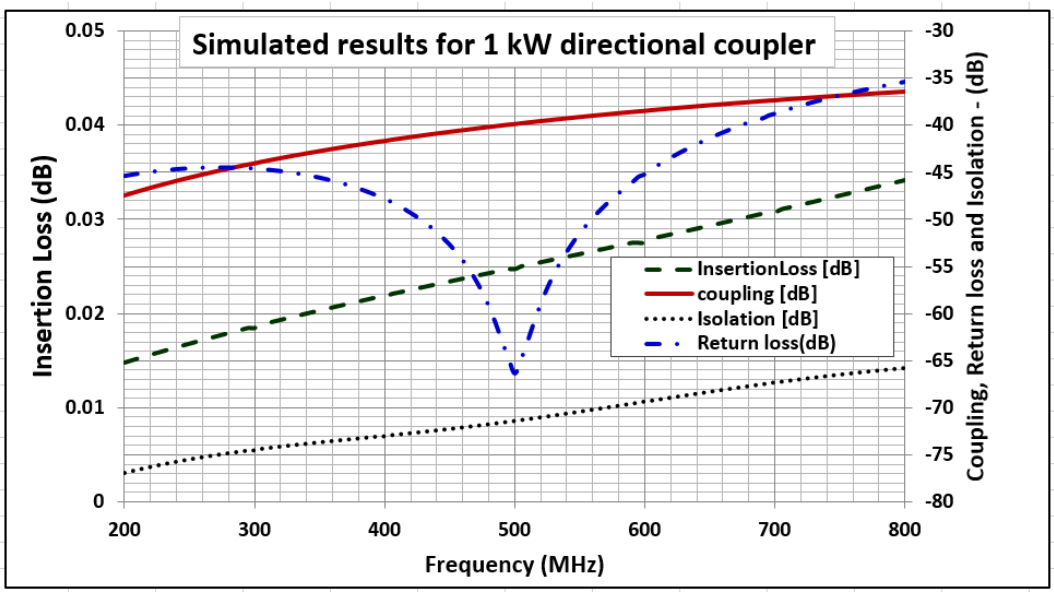


Fig. 5.6: Simulated results for 1 kW directional coupler

The structure for the type B or 5 kW coupler is essentially similar to the 1 kW coupler, except the 1-5/8" EIA flange connection, instead of N connectors, at the output as well as the input ports. However, the 20 kW coupler is a dual directional coupler with 3-1/8" EIA flange at its input and output ports. Its EM model is shown in Fig. 5.7. This coupler has a pair of auxiliary lines and associated coupled and isolated ports. In fact, it is a combination of two 3-port couplers having their main lines cascaded, and their internally terminated ports facing each other at the interface between the couplers. Such combination provides bi-directional coupler action, but with the independent use of the coupled ports. It has the advantage that a mismatched load applied to either of them will not affect the other. At high power this arrangement is necessary in order to accurately characterize the various performance factors of the SSPA system. The separate auxiliary lines are provided for the separate sampling of forward and reflected power, without getting affected by the return loss of the terminating impedance at the respective isolated port. All these directional couplers, discussed above, were fabricated (Fig. 5.8) using brass material, and afterwards they were suitably silver plated on their inner surface. The length of the 1 kW coupler was 60 mm while for 5 kW and 20 kW

couplers it was 120 mm and 220 mm respectively. For the 1 kW coupler, standard SMA connectors were used for providing access to auxiliary line. In other two couplers standard N type connectors were used for this purpose.

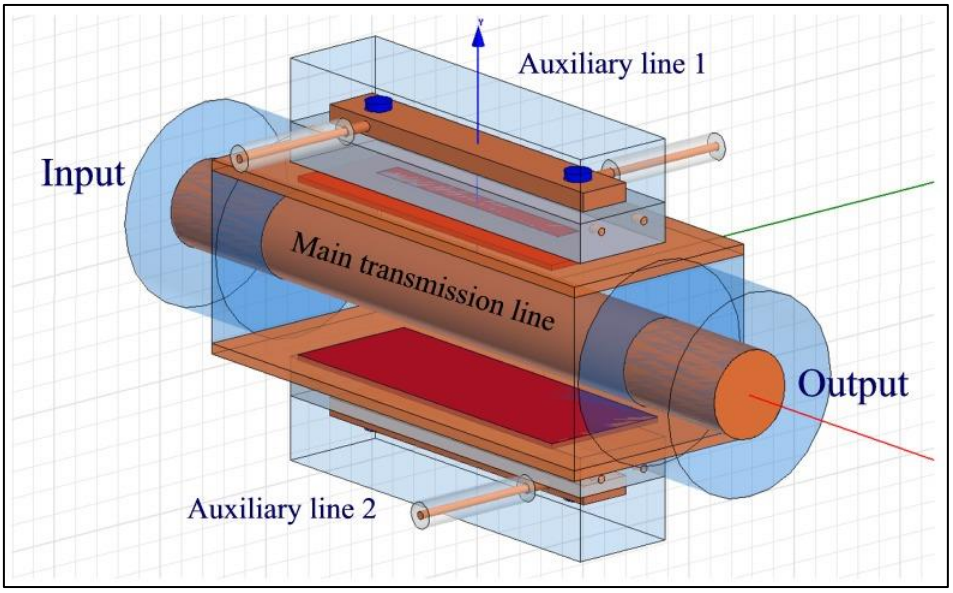


Fig. 5.7: EM model of 20 kW bi-directional (dual) coupler

Fig. 5.8: Three fabricated couplers (for 1 kW, 5 kW and 20 kW respectively)

All these couplers were characterized at different frequencies for measuring various figures of merit. Their scattering parameters were measured by using a vector network analyser.

The measurement results show a good agreement with the design specifications and simulated data, as compared in Table 5.2 at 352 MHz. The swept frequency measurement for each coupler is presented separately. The measured insertion loss, throughout the operational frequency band, for these couplers was less than 0.05 dB. This is one of the advantages of the rigid and compact structure used for these couplers.

Table 5.2: Comparison of calculated and measured parameters at 352 MHz

Directional Coupler type	**Calculated (HFSS) coupling**	**Measured Coupling**	**Calculated (HFSS) directivity**	**Measured Directivity**
A- 1 kW	42.7 dB	41 dB	30.9 dB	28.1 dB
B- 5 kW	50.2 dB	55.4 dB	28.8 dB	29.6 dB
C- 20 kW	50.3 dB	50.4 dB	28.1 dB	19.6 dB

The coupler type A, designed for 1 kW, was tested to measure its return loss, insertion loss, coupling and isolation as a function of the frequency. This swept frequency measurement, for different scattering parameters, is shown in Fig. 5.9.

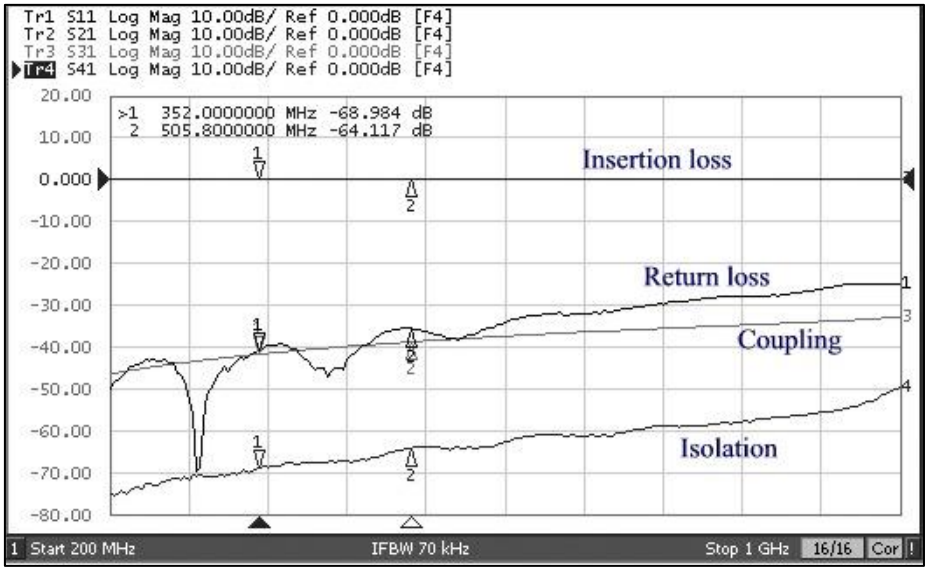


Fig. 5.9: Measured swept frequency parameters for 1 kW directional coupler

As seen here, the coupling and return loss degrade with the frequency but maintain an acceptable value throughout the frequency band. The data markers, shown on different traces,

are at 352 MHz and 505.8 MHz respectively. At 505.8 MHz input VSWR is 1.027 while coupling is 39.4 dB. The calculated directivity from the measured value of the coupling and isolation is 28.4 dB. The insertion loss, as stated earlier, is very low throughout the frequency range.

Similarly, the measured swept frequency response, for the 5 kW coupler, is shown in Fig. 5.10. From this graph it is clear that the return loss (Trc1) is better than -27 dB throughout the operating frequency range of 300 to 700 MHz. The traces 5 and 6 represent the insertion loss and the coupling respectively. The traces 7 and 8 are duplicate ones and each one of them represents the isolation. The coupler directivity is still better than 26 dB throughout the frequency range.

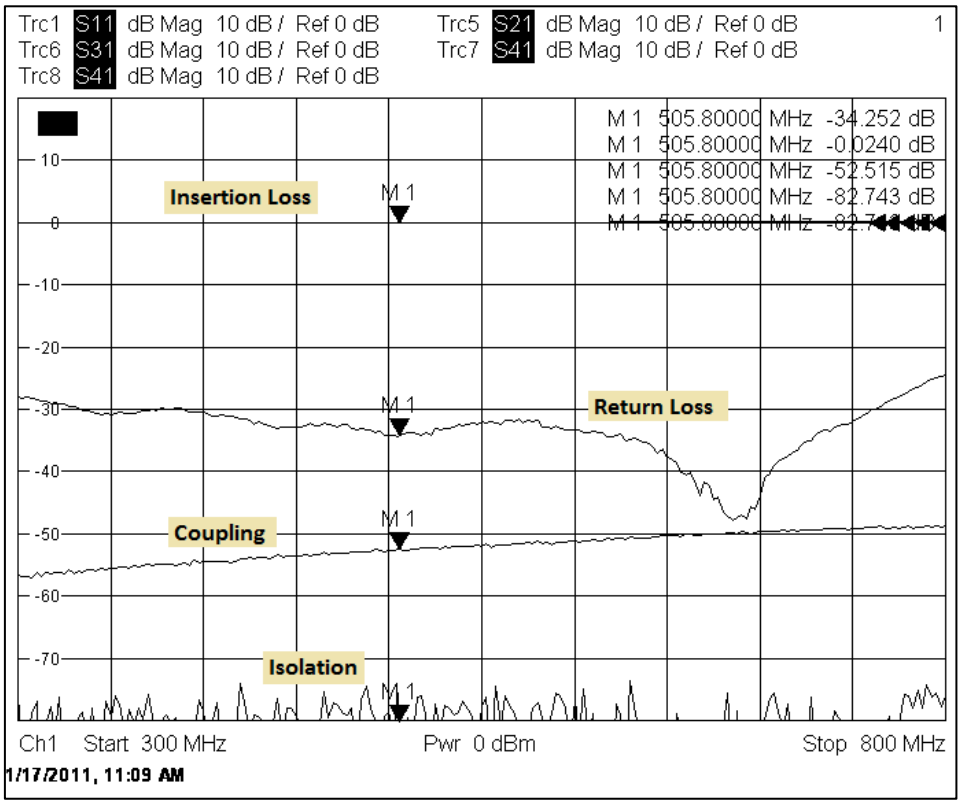


Fig. 5.10: Measured swept frequency parameters for 5 kW directional coupler

Finally, the Table 5.3 shows the measurement data, taken at four different frequencies of interest, for the dual directional coupler. The insertion loss is quite low while the return loss

is slightly poor as compared to values obtained for the previous two couplers (type B and C). The coupling is acceptable in the lower frequency range but deviates by 3.2 dB at 650 MHz. It can be seen that the directivity is lower compared to the previous two designed couplers. Hence, dual auxiliary lines are essential at high power, in order to alleviate the effect of the poor directivity in the measurement.

Table 5.3: Measured data for 20 kW dual directional coupler

Frequency of measurement / **Measured parameter**	**325 MHz**	**352 MHz**	**505.8 MHz**	**650 MHz**
Return loss (dB)	22.01	20.9	22.9	27.1
Insertion loss (dB)	0.12	0.12	0.12	0.13
Isolation-1 (dB)	70.3	70	70	74
Coupling-1 (dB)	50.8	50.4	48.2	46.8
Directivity-1(dB)	19.5	19.6	21.8	27.2
Coupling-2 (dB)	51.3	50.9	49	47.6
Isolation-2 (dB)	70	68.4	70.4	74
Coupling-2	51.3	50.9	49	47.6
Directivity-2	18.7	17.5	21.4	26.4

In making a high power SSPA system, the directional couplers are required in multiple in order to sample and measure the RF signal. The presented designs with a rigid structure for the main line as well as the auxiliary line, achieve a coupling coefficient in the range 40 to 50 dB. The designed directional couplers represent a significant improvement for the high-power measurement systems since they are broad-band and have a good directivity. They may be fabricated at low cost with an excellent repeatability due to the rectangular cross section and its rigid structure. The measured results show very good agreement with the predicted per-formance of the designed couplers.

Chapter 6. High Power Solid State Amplifier System

This chapter examines the system level design and operational issues for high power solid state amplifier, which encompasses multiple PAs, dividers, combiners and directional couplers. Such system was termed as an SSPA in previous chapters. Typical RF power, required in the particle accelerators and communication systems, is much higher than the capability of an individual RF transistor. Hence, multiple stages of a modular and scalable architecture are adopted to enhance the RF power in an SSPA. This architecture makes use of the *divide amplify and combine* strategy with the help of multiple PAs, dividers and combiners. For such architecture, issues pertaining to the graceful degradation and amplitude as well as phase imbalance are important. In this chapter, starting from a discussion on the architecture selection, these issues were studied by developing a suitable scattering parameter based model in tune with the design guidelines available from the literature [213]. This study helped designing high power SSPA systems. In this series, the first design of 2 kW SSPAs, was a fruitful starting point. It served as a test stand for the performance evaluation of various passive components, at high power, designed thereafter. Encouraged by its successful characterisation and performance, design efforts were extended for the physical implementation of two more systems at 20 kW and 50 kW, respectively. Their performance estimations, design detail, system level simulation and measurement results are discussed in this chapter.

6.1 Selection of System Architecture for High Power

For obtaining a high power, the direct connection of several PAs is generally impractical as they interact, allowing changes in their output from one to cause the load impedance, seen by the other, to vary. Therefore, in selecting the architecture for the SSPA system, an RF

combiner plays a pivotal role. Different types of architecture have evolved from power combining schemes, discussed in chapter 4. Its selection involves the system level study and its impact on the overall RF performance. Such an exercise leads to the system budget calculation for the output power, gain and efficiency.

For making use of N PA modules in an SSPA system, the corporate architecture is preferred compared to the travelling wave or serial topology. The increasing losses in transmission line segments, used in the latter one, makes such topologies inefficient for large number of PAs. The corporate architecture is designed using an M-tier tree structure of N-way combiners. For low power output, the binary tree with N equal to 2 is very popular in communication amplifiers. For realising kW level SSPA, N is optimally selected depending upon the combiner (N-way) topology, frequency of operation and output power from the individual PA module. For large numbers of PAs with equal gain, the N-way radial combiner outperforms, in terms of its insertion loss, compact structure and uniform power distribution.

Whether to use a number of smaller power PAs or a few larger power PAs is one of the basic decisions in the selection of the SSPA architecture. Even when larger power PAs are available, smaller power PAs often offer a higher gain, better phase linearity, and lower cost. The heat dissipation is more readily managed with a number of smaller power PAs. Advantage of using a large N for the power combiner is that the phase noise contributed by the PA-ensemble is reduced by a factor of 1/N. This is because the input signal, being amplified, adds coherently at the output, whereas the uncorrelated noise fluctuations add in-coherently. Hence, the peak amplitude of the signal increases more rapidly than the noise skirts. On the other hand, the increase in components count, assembly time, connecting cables and physical size are significant disadvantages to the use of multiple smaller PAs. In general, the N-way *divide and combine* architecture is very popular for making a modular SSPA system. If required power of the system exceed beyond the capacity of such N-way architecture, it can

be used as a generic template for implementing a tree architecture using binary power dividers and combiners. Recently a new concept was proposed [214] in ESRF for obtaining very high power by directly coupling hundreds of PA modules to a pill-box type cavity combiner. Due to absence of connecting coaxial cables, this architecture is claimed to have a very high power and good system efficiency.

Apart from being efficient at high power, the architecture selection for the SSPA system is also affected by additional issues like RF grounding, volume, heat dissipation, reliability implications, ease of fabrication, technology readiness, and scalability to extend to higher power as well as higher frequencies. It should also be easy to maintain. In SSPA systems, the power dividers and combiners are generally very efficient. Hence, they do not require any forced cooling. However, for PA modules, forced air or liquid cooling is required.

For an RF and microwave circuit, the separation of the signal and ground conductors establishes the configuration of the electric and magnetic fields along with their *wave impedance*. If the high frequency grounding of SSPA system and its components is not proper, they may malfunction and interfere with each other in unexpected and undesirable ways. A proper RF grounding helps achieving EMC/EMI standards along with providing safety and the suppression of unwanted radiation from the system components. The basic RF grounding problems influencing the performance of SSPA include discontinuities, excessive inductive reactance, excessive resistance, excessive electrical length, incorrect ground-signal conductor geometric relationships and ground path induced coupling. The PA modules require careful grounding to suppress output-to-input feedback and to prevent oscillation. At individual PA level, this phenomenon is avoided by drilling Vias on the PCB with proper separation and length. In general at least 10 vias per wavelength are required [215]. Another satisfactory solution to this problem is to mount the modules on a low impedance metal plate.

Such plate also serves as the rigid base for the PA board, as well as a cooling plate. It has low inductance in addition to low resistance, so it makes a good DC, digital, and RF ground path.

6.2 System Level Performance Estimation

After selecting the architecture of a high power SSPA system, its gain/power budget and other performance factors need to be estimated. If constituent components of the SSPA, discussed in previous chapters, are lossless and perfectly matched at various interfaces, their integration according to the selected architecture, yields an ideal performance for the final output power and the system efficiency. However in a real time SSPA system, components, specifically PA modules, are not ideal ones and accordingly the integrated system shows performance-degradation, manifested as reduced output power and system efficiency. The PA modules, being active components, are most vulnerable to degrade in performance. Such degradation may occur with time due to full or partial failure of the PA modules. The popular N-way *divide and combine* architecture ensure a graceful degradation [78]. This term translates into a smooth variation in performance; if one or more among the PAs fail or underperform, whereas the remaining ones are not affected strongly by such a failure. The graceful degradation represents a significant aspect of the SSPA system as compared to the microwave tubes, for which a failure is usually a catastrophic occurrence.

Apart from the graceful degradation, the output power reduction can happen due to the amplitude and phase imbalance in the output response of different components of the SSPA system. In practice, the cluster of PAs, which feed to the N-way combiner, are rarely identical due to device/fabrication tolerances and the variation in the impedance tuning. There may be a deviation in the amplitude and phase of the output signal from one PA to another. In an integrated SSPA system, even with a symmetric and uniform combiner/divider, such deviation disturbs the impedance matching at various interfaces. This may result in the system

instability and degradation of the final output power and the overall system efficiency. This problem is further aggravated if divider and combiner response is non-uniform. Mathematically this problem can be illustrated by a simple formulation for N-way SSPA system, shown in Fig. 6.1. Let the time varying input signal to this system is given as

$$X(t) = A\cos(\omega t) \tag{6.1}$$

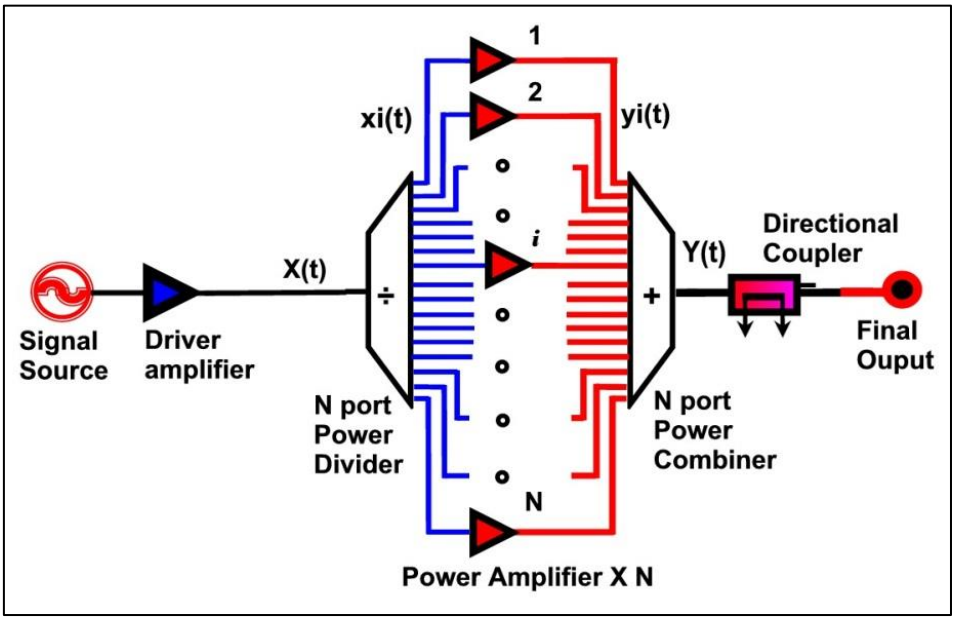


Fig. 6.1: A typical N-way solid state amplifier system architecture

Here ω is the angular frequency of the RF signal and A is its amplitude. This signal gets split up by an N-way divider. Let the variation in transmission coefficient in each branch of this divider is accounted by δA_i *and* $\delta\varphi_i$ for amplitude and phase respectively, for the i^{th} branch. Hence, the input and output signal for the i^{th} PA will be, respectively

$$x_i(t) = \frac{A(1+\delta A_i)\cos(\omega t + \delta\varphi_i)}{\sqrt{N}} \quad (i = 1..N) \tag{6.2}$$

$$y_i(t) = \frac{A(1+\delta A_i)G(1+\delta G_i)\cos(\omega t + \delta\varphi_i + \delta\theta_i)}{\sqrt{N}} \quad (i = 1..N) \tag{6.3}$$

Where G is the nominal voltage gain of the PA, δG_i and $\delta\theta_i$ are the gain/amplitude and phase imbalance for the i^{th} PA. Thus input signals to the combiner are having variation in the

amplitude as well as phase. Assuming the same RF characteristic for the combiner and divider, the sum of the N branch signals (output of the combiner) can be expressed as

$$Y(t) = \frac{AG}{N}\sum_{i=1}^{N}(1+\delta A_i)^2(1+\delta G_i)\cos\left(\omega t + 2\delta\varphi_i + \delta\theta_i\right) \tag{6.4}$$

Thus, the output response deviates around a mean value and it may deteriorate due to the deviation in amplitude and phase from their respective ideal values. A negative fractional value of δG_i, tending to 1 corresponds to a partial of full failure of the PA. Thus, analysis of the amplitude/phase imbalance and the graceful degradation is necessary for the performance prediction before the system implementation as well as during the real time operation. SSPA designers have tried different methods like phase delay line [54] and forced compression of drain characteristics [216] in order to synchronize amplitude and phase of PAs.

Depending upon the degree of system complexity, its analytical solution is possible for some specific cases. In general, for a high power SSPA system, a system level simulation is required for the accurate calculation of the output power, efficiency and electrical/RF power distribution among building blocks. The latter one helps estimating thermal load for the system and the lifetime of a particular RF component. For analytical solution as well as the computer aided system simulation, it is necessary to develop a scattering parameter [217] based behaviour model [79] for the N-way SSPA architecture, shown in Fig. 6.1.

6.2.1 Scattering Parameter Model of N-way SSPA Architecture

In accordance with the architecture shown in Fig. 6.1, this model consist of an N way divider, N way power combiner and N PA modules (Fig. 6.2). Initially it is shown without any interconnection. Such set represents a basic template. A high power (kW level) SSPA system may utilise multiple instances of such template. The branch ports of the combiner/divider are indexed from 1 to N while the zeroth port reserved for the input port in the divider and the

output (summing) port in the combiner. Different power waves, at various ports, represent the incident or forward (a_{xi}) and reflected waves (b_{xi}). In this notation, the letter x stands for d, c and s for the divider, combiner and PA respectively. Similarly scattering parameters are represented as s_{xij}. These are all vector quantities. Γ_{si} is the reflection coefficient at the output of i^{th} PA (source) and b_{si} corresponds to the available complex power wave that would be launched from the i^{th} PA on a transmission line, with reflection coefficient equal to Γ_{si}^{*}. Here, i and j are integers which represent the port numbers.

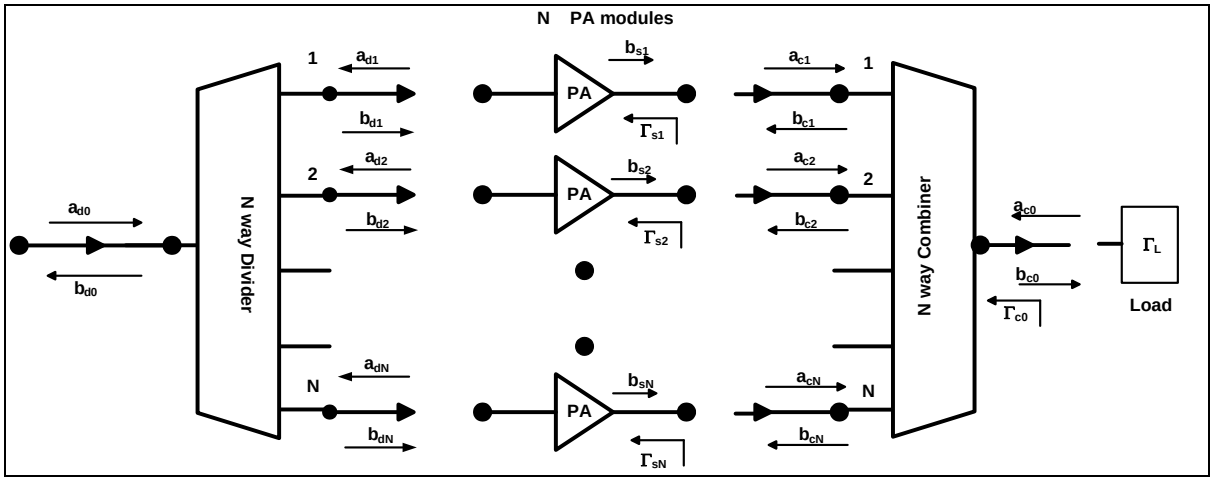


Fig. 6.2: S parameter model of the N-way SSPA system

All of the PA modules are assumed to be memory less, identical and linear. The divider and combiner are assumed to be radial, symmetric, passive and lossless (N+1) ports networks, having only intrinsic loss. The scattering matrix of the divider/combiner, having (N+1) row and columns, is given as

$$S_{PDC} = \begin{bmatrix} S_{c11} & S_{c12} & \cdots & S_{c1N} & S_{c10} \\ S_{c21} & S_{c22} & \cdots & S_{c2N} & S_{c20} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ S_{cN1} & S_{cN2} & \cdots & S_{cNN} & S_{cN0} \\ S_{c01} & S_{c02} & \cdots & S_{c0N} & S_{c00} \end{bmatrix} = \begin{bmatrix} S^{11} & S^{12} \\ S^{21} & S^{22} \end{bmatrix}$$

This matrix is partitioned in four blocks. S^{11} is the matrix related with the dividing/combining network. S^{22} is related with the reflection coefficient (s_{c00}) of the

dividing/summing port. S^{12} and S^{12} are the reverse and forward transmission coefficients of the divider/combiner. Further, for a uniform and symmetric PDC, all of the transmission coefficients are equal, or

$$s_{coi} = s_{coe} \quad i = 1,2,\ldots..N \tag{6.5}$$

In majority of cases, designing a symmetric combiner with negligible variation in s_{coi} from branch to branch is not difficult. This fact is also evident from the measured data, presented in chapter 4 for different 8-way and 16-way combiners. In these combiners worst case value of measured deviation was nearly 0.2 dB (~ 4.7%).

Once these components *viz*. divider, PAs and combiner are interconnected, power waves get modified to satisfy the boundary conditions at the interfaces. Galani [75] computed the transfer function of such system using scattering matrices to discuss the optimum performance for the small value of the imbalance in PA outputs (variation in b_{si}) and the PA failure. The analysis revealed that such transfer function shows a weak dependence on any mismatch at the output of the PA, provided these PAs are identical and have a high power gain, compared to their input as well as output reflection coefficients.

For analytical solution, the power combiner is the main attraction. Hence, to simplify the analysis, the power divider may be deleted from this model without any loss of generality. This is also justified because the power level at the divider ports is nearly ten to twenty times lower than the power at the combiner. Hence, the effect of the imbalance (of amplitude/phase) will be negligible at the divider's output. Such deletion makes input of all PAs matched to the system impedance. The remaining interconnected model is shown in Fig. 6.3. At the output port of the combiner, the power wave equation can be written as

$$b_{co} = s_{co1}a_{c1} + s_{co2}a_{c2} + \cdots + s_{coN}a_{cN} + s_{coo}a_{co} = s_{coe}\sum_{i=1}^{N} a_{ci} + s_{coo}a_{co} \tag{6.6}$$

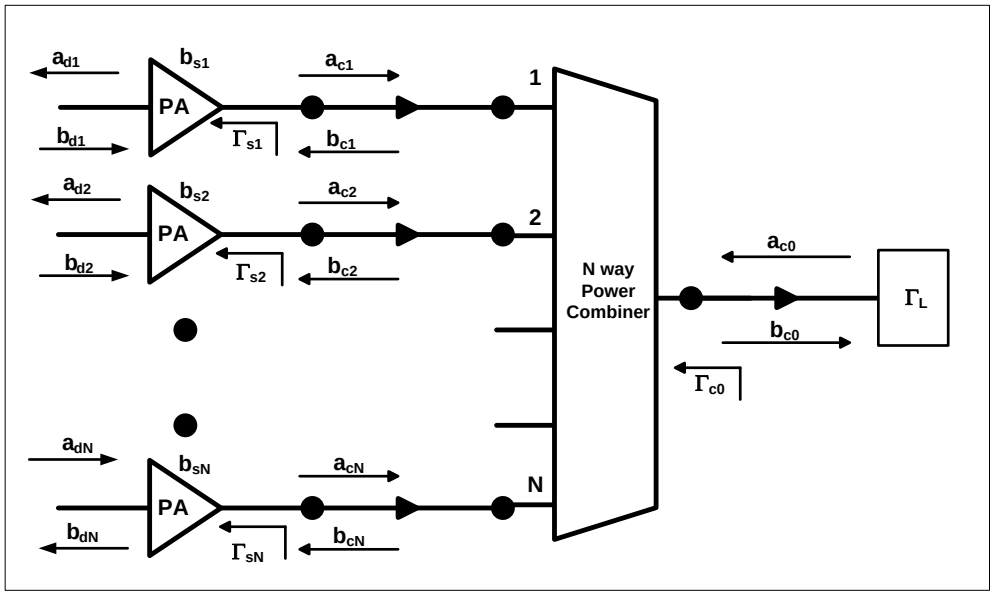


Fig. 6.3: Simplified behavioural model of N-way SSPA system

Again for simplification, it may be assumed that the power combiner is matched at its input as well as output ports with the interfaced PA and load, respectively. In a high power PA, Γ_{si} can be brought near to its ideal value, by deploying a circulator at the output of the PA. Such assumptions result in

$$\Gamma_{ci} = \Gamma_{si}^{*} \tag{6.7}$$

$$\Gamma_{L} = \Gamma_{co}^{*} \tag{6.8}$$

Here Γ_{ci} is the input reflection coefficient at the i^{th} port of the combiner. These conditions implies that

$$a_{ci} = b_{si} = \sqrt{P_{avi}}\, e^{j\theta_i} \tag{6.9}$$

$$a_{co} = 0 \tag{6.10}$$

P_{avi} is the available power from the i^{th} PA and θ_i is the phase angle of the i^{th} input signal (b_{si}) with respect to some arbitrary reference. Substituting these results in (6.6) we get

$$b_{co} = s_{coe} \sum_{i=1}^{N} b_{si} = s_{coe} \sum_{i=1}^{N} \left(\sqrt{P_{avi}}\, e^{j\theta_i}\right)$$

For such case, the output power P_{out} from the combiner is proportional to the square of the magnitude of the power wave b_{c0}. Hence, it can be expressed as

$$P_{out} = |b_{c0}|^2 = |s_{coe}|^2 \left[\left(\sum_{i=1}^{N} \sqrt{P_{avi}} \cos\theta_i \right)^2 + \left(\sum_{i=1}^{N} \sqrt{P_{avi}} \sin\theta_i \right)^2 \right] \tag{6.11}$$

Using this expression, the N-way PA-combiner system efficiency, defined as the ratio of output power to total input power fed to this combiner, can be derived as

$$\eta_{pc} = |s_{coe}|^2 \cdot \frac{\left[\left(\sum_{i=1}^{N} \sqrt{P_{avi}} \cos\theta_i \right)^2 + \left(\sum_{i=1}^{N} \sqrt{P_{avi}} \sin\theta_i \right)^2 \right]}{\sum_{i=1}^{N} P_{avi}} \tag{6.12}$$

For an equal signal excitation, it takes the maximum value of

$$\eta_{c,max} = N. |\, s_{coe}|^2 \tag{6.13}$$

Hence, (6.12) can be finally expressed as

$$\eta_{pc} = \frac{\eta_{c,max}}{N} \cdot \frac{\left[\left(\sum_{i=1}^{N} \sqrt{P_{avi}} \cos\theta_i \right)^2 + \left(\sum_{i=1}^{N} \sqrt{P_{avi}} \sin\theta_i \right)^2 \right]}{\sum_{i=1}^{N} P_{avi}} \tag{6.14}$$

For the efficiency calculation of the complete SSPA system, this value should be duly augmented by the power added efficiency (η_{pae}) of the PA and AC to DC efficiency of bias power supplies. As seen in (6.12), there are two loss mechanisms which may impart towards a power reduction. The first one is the insertion loss of the combiner, accounted by $\eta_{c,max}$ or its transmission coefficients s_{coe}. This is entirely an intrinsic property of the combiner. The second one is the power loss due to the imbalance in amplitude ($\sqrt{P_{avi}}$) and phase (θ_i) of the output signals (b_{si}). This imbalance disturb the even mode excitation of the combiner and manifest itself as multiple reflection between PA cluster and combiner.

For varying amplitude but equal phase (no phase imbalance) of the output signals (b_{si}), an analysis for quantifying the graceful degradation, was performed detailed in the next section, in two parts. The first part of this analysis assumes that the failed PAs maintains the

matched impedance at the PA-combiner interface, whereas the second part accounts for the mismatching offered by failed PAs. For the general case (amplitude and phase imbalance as well as non-uniform combiner), an approach for estimating worst case efficiency is discussed afterwards. Such analytical techniques help estimating the performance parameters of the SSPA system. However, during the physical design of the SSPA system, the effect of the divider as well as the nonlinear response of the PA, need to be accounted with the help of a system level computer-aided simulation. Hence, during the real time designs and their experimental verification, an amalgam of such analysis and the system level simulation was used to estimate the system efficiency.

6.2.2 Analysis for Graceful Degradation

As stated earlier, when multiple PAs are combined, the output power of the SSPA system (Fig. 6.3) will degrade gracefully in case one or more PA fail to operate. Ideally, when a PA fails, the output power would have been reduced only by the amount contributed by that PA. Thus in an N-way system, if M (M<N) PA fail, the resulting output power would be multiplied by a fraction (1-M/N). However, in actual condition, some power is diverted from the healthy PAs to failed PAs. Hence, the reduction in power is somewhat different [218]. Depending upon the situation, the PA may or may not remain impedance matched with the combiner input, after failure. Hence, two cases (matched and mismatched PAs) need to be considered. It is assumed that the failed PA maintains the same insertion phase, the one exhibited by it in healthy condition.

6.2.2.1 Case 1: Matched Impedance

This analysis is the simplest case of the graceful degradation. Let, N PAs are feeding to the power combiner with an equal signal in amplitude and phase. During the SSPA operation, let M amplifiers among the N ones fail in an identical manner. Under such situation, each of

these M modules gives reduced output power by a factor p (fractional reduction ratio) varying from 0 (total failure) to 1 (no failure). Still (N-M) PAs are providing the full available power to the combiner. Hence, P_{out} can be written from (6.14) as

$$P_{out} = \frac{\eta_{c,max}}{N}\left(\sum_{i=1}^{N-M}\sqrt{P_{avi}} + \sum_{i=1}^{M}\sqrt{p.P_{avi}}\right)^2 \tag{6.15}$$

For an equal power from PAs, substituting $P_{avi} = P_{ave}$ for all value of i in above equation, we get after simplifying

$$P_{out} = \frac{\eta_{c,max}}{N}\cdot(N - M + M\sqrt{p})^2 \cdot P_{ave} \tag{6.16}$$

While, the total combiner input power is given by

$$P_{cin,total} = (N - M + p\cdot M)\,P_{ave} \tag{6.17}$$

Thus, the N-way PA-combiner system efficiency becomes

$$\eta_{pc} = \frac{\eta_{c,max}}{N}\cdot\frac{(N - M + M\sqrt{p})^2}{(N - M + p\cdot M)} \tag{6.18}$$

A plot of the normalized output power is reported in Fig. 6.4.

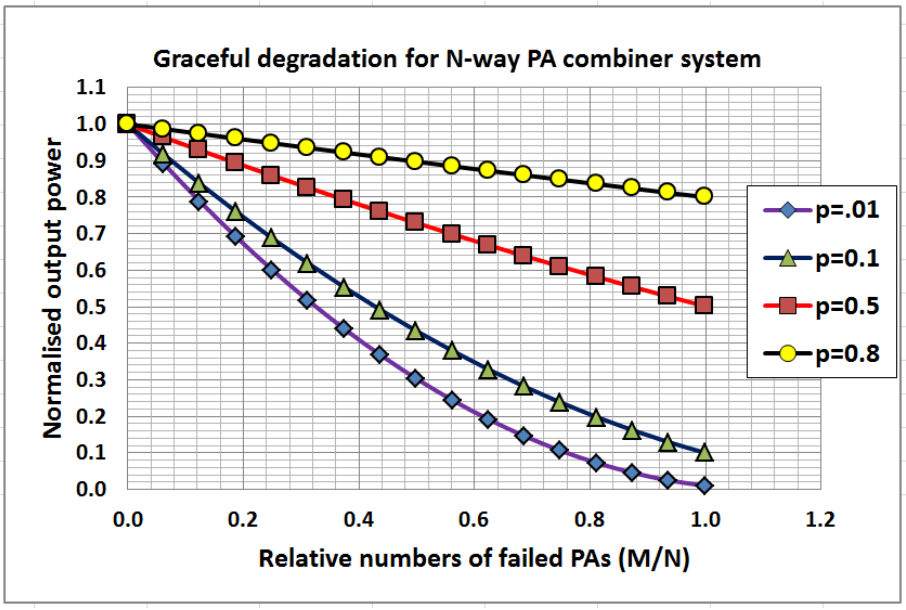


Fig. 6.4: Normalized output power for increasing failure of PAs

It is normalised with respect to the maximum output power ($= \eta_{c,max} \cdot N \cdot P_{ave}$) in the healthy condition, as a function of the relative number of failed PAs (M/N), for different values of p. The failure of some PA modules results in a slightly reduced output power, depending on the failures entity (p). Such a graceful degradation represents a significant aspect of the SSPA system, compared to the vacuum tube amplifiers. This is advantageous for particle accelerator like machines, where a sudden breakdown is highly undesirable.

6.2.2.2 Case 2: Mismatched Impedance

Unlike previous case, if the failed PA presents an impedance mismatch at its output port, the reflection may occur from the combiner input [219]. There may be multiple reflections between the output of failed PA and the combiner input. For calculating the output power degradation, in this case, it is assumed that M PAs fails in an identical manner so they have similar reflection ($\Gamma_{si} = \Gamma_s$) at the respective output port. Corresponding impedance mismatch, at the n^{th} input of the combiner, is denoted by Γ_c. It is also assumed that the remaining (N-M) PAs are non-interacting and continue to operate normally. Under such failure, the net power at the combiner's output gets reduced due to power waves flowing from healthy ports to failed ports. Hence, the degraded output wave, denoted by $b_{c0}^{'}$, can be written as

$$b_{c0}^{'} = \sum_{n=1}^{N-M} (s_{c0n} a_{cn}) + \sum_{m=1}^{M} (s_{c0m} a_{cm}) \tag{6.19}$$

In general subscript n refers to the healthy node and m refers to the failed node. For failed PAs, we have

$$a_{cm} = \Gamma_s \, b_{cm} \tag{6.20}$$

$$\text{So} \qquad b_{c0}^{'} = \sum_{n \neq m}^{N-M} (s_{c0n} a_{cn}) + \sum_{m \neq n}^{M} (s_{c0m} \Gamma_s \, b_{cm}) \tag{6.21}$$

The aim is to calculate this degradation and the corresponding reduced efficiency. Due to the complexity of the problem, it may be solved with the help of the signal flow graph, initially for only one PA failure at the m^{th} port. In Fig. 6.5, a signal graph is drawn for the healthy case (M=0). Fig. 6.6 shows one PA failure at the m^{th} port with the output power wave denoted by b_{1c0}.

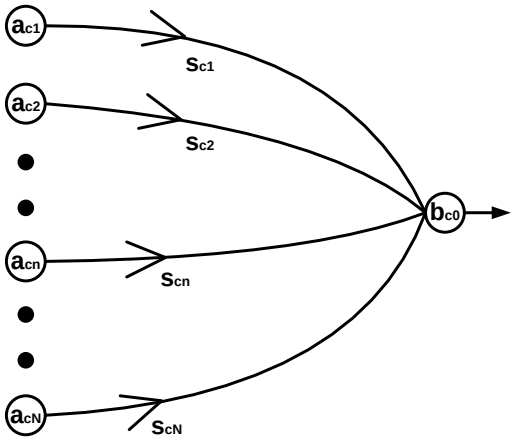


Fig. 6.5: Signal graph for healthy case (M=0)

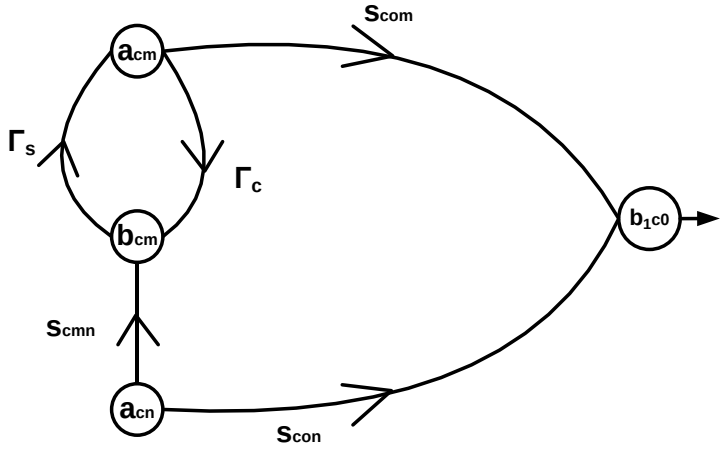


Fig. 6.6: Signal graph for one PA failure (M = 1)

From this signal graph (Fig. 6.6), the reflected power wave at the m^{th} port is given as

$$b_{cm} = \Gamma_c a_{cm} + s_{cmn} a_{cn} \tag{6.22}$$

$$b_{1c0} = (s_{c0n} a_{cn}) + (s_{c0m} \Gamma_s \, b_{cm}) \tag{6.23}$$

Eliminating a_{cm} by using (6.20) and solving for b_{cm} we get

$$b_{cm} = \left(\frac{s_{cmn}}{1 - \Gamma_c \Gamma_s}\right) a_{cn} \tag{6.24}$$

Substituting this value in (6.23) we get

$$b_{1c0} = s_{c0n} a_{cn} + \frac{s_{c0m} s_{cmn} \Gamma_s}{1 - \Gamma_c \Gamma_s} a_{cn} \tag{6.25}$$

Effect of all of the N ports can be accounted by summing expression of b_{cm} and using (6.21)

$$b_{cm} = \Gamma_c a_{cm} + \sum_{n=1}^{N-M} s_{cmn} a_{cn} \tag{6.26}$$

$$b_{c0}^{'} = \sum_{n=1}^{N} \left(s_{c0n} a_{cn} + \frac{s_{c0m} s_{cmn} \Gamma_s}{1 - \Gamma_c \Gamma_s} a_{cn}\right) \tag{6.27}$$

$$= \sum_{n \neq m}^{N} \left(s_{c0n} + \frac{s_{c0m} s_{cmn} \Gamma_s}{1 - \Gamma_c \Gamma_s}\right) a_{cn}$$

Thus, the reduction in the power is augmented by an additional factor $\frac{s_{c0m} s_{cmn} \Gamma_s}{1 - \Gamma_c \Gamma_s}$. In fact, we can rewrite the above equation as

$$b_{c0}^{'} = \sum_{n \neq m}^{N} \left(s_{c0n}^{'}\right) a_{cn} \tag{6.28}$$

With

$$s_{c0n}^{'} = s_{c0n} + \frac{s_{c0m} s_{cmn} \Gamma_s}{1 - \Gamma_c \Gamma_s} \tag{6.29}$$

For an equal output signal from all the healthy PAs ($a_{cn} = a_{ce}$) and a symmetric combiner ($s_{c0n} = s_{c0e}$), the contribution to the reflected node (b_{cm}) is also equal from all of the PAs, *i.e.* $s_{cmn} = s_{cme}$. So

$$b_{c0}^{'} = (N - 1) \cdot \left(s_{c0e} + \frac{s_{c0m} s_{cme} \Gamma_s}{1 - \Gamma_c \Gamma_s}\right) a_{ce} \tag{6.30}$$

For an increased number of failures, one needs to take the power transfer between the failed ports. This situation should be accounted in order to generalise the degraded power output for M number of PAs failure. In order to account this situation, once again due to complexity, we calculate the output power wave when two PA fails (M=2). Let, the sub-scripts l and m refer to the failed PAs while n still used for the healthy PA's power waves. The signal flow graph for this condition is drawn in Fig. 6.7. By observing different nodes and power waves in this graph, we get following three relations.

$$b_{cl} = s_{cln}a_{cn} + s_{cll}a_{cl} + s_{clm}a_{cm} \tag{6.31}$$

$$b_{cm} = s_{cmn}a_{cn} + s_{cml}a_{cl} + s_{cmm}a_{cm}$$

$$b_{2c0} = s_{c0n}a_{cn} + s_{c0l}a_{cl} + s_{c0m}a_{cm}$$

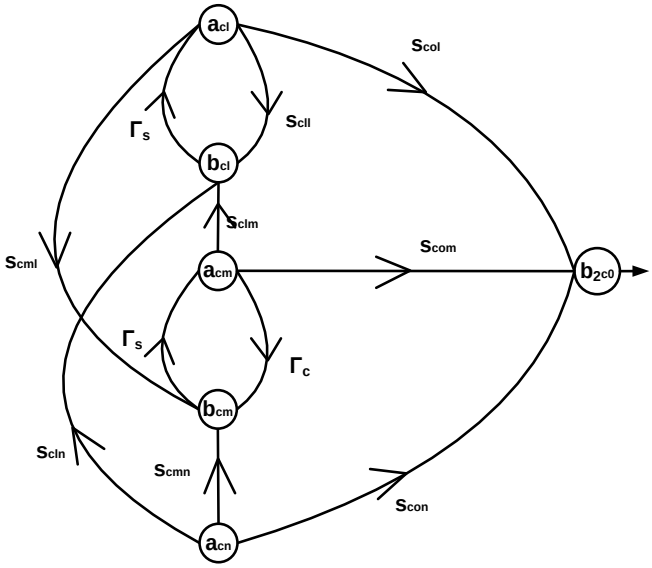


Fig. 6.7: Signal flow graph for failure of two PAs (M = 2)

For identical failure, as assumed earlier, we have

$$b_{cl} = b_{cm} \tag{6.32}$$

$$a_{cl} = a_{cm}$$

$$s_{clm} = s_{cml}$$

$$s_{cll} = s_{cmm} = \Gamma_c$$

So

$$b_{cm} = b_{cl} = s_{cmn}a_{cn} + (\Gamma_c + s_{cml}) \cdot a_{cm} \tag{6.33}$$

Using (6.20) we get

$$b_{cm} = s_{cmn}a_{cn} + (\Gamma_c + s_{cml}) \cdot \Gamma_s\, b_{cm} \tag{6.34}$$

Rearranging this equation we get

$$b_{cm} = \left(\frac{s_{cmn}}{1 - \Gamma_s\,(\Gamma_c + s_{cml})}\right) a_{cn} \tag{6.35}$$

This can be compared with (6.24), derived for one PA failure. Addition of the term s_{cml} can bee seen here. Once again, for a symmetric combiner ($s_{c0l} = s_{c0m}$), the contribution to the reflected node (b_{cm}) is also equal from all PAs. i.e. $s_{cmn} = s_{cme}$ so that

$$b_{2c0} = s_{c0n}a_{cn} + 2s_{c0m}a_{cm} \tag{6.36}$$

Putting the value of a_{cm} from (6.20), we get

$$b_{2c0} = s_{c0n}a_{cn} + 2\Gamma_s\, s_{c0m}b_{cm} \tag{6.37}$$

Substituting the value of b_{cm} from (6.34) and rearranging, we get

$$b_{2c0} = s_{c0n}a_{cn} + \left(\frac{2 \cdot s_{cmn}s_{c0m}\Gamma_s}{1 - \Gamma_s\,(\Gamma_c + s_{cml})}\right) a_{cn} \tag{6.38}$$

Studying this equation (for M=2), it can be concluded that the interaction between failed ports (i.e. s_{cml}) increase as (M-1). For the N port system with two failed PAs, this equation can be easily extended (with $s_{cmn=}\, s_{cme}$) as

$$b_{c0}^{'} = (N-2) \cdot \left(s_{c0e} + \frac{2 \cdot s_{cme}s_{c0m}\Gamma_s}{1 - \Gamma_s\,(\Gamma_c + s_{cml})}\right) a_{ce} \tag{6.39}$$

It should be noted that the term s_{cml} in above equation, represents the interaction between two failed ports. With similar logic, for M failed ports

$$b_{c0}^{'} = (N-M) \cdot \left(s_{c0e} + \frac{M \cdot s_{cme}s_{c0m}\Gamma_s}{1 - \Gamma_s\,(\Gamma_c + (M-1)s_{cml})}\right) a_{ce} \tag{6.40}$$

In order to quantify the power degraded at the combined output, we need to calculate

$$b_{c0}^{'} - b_{c0} = (N-M)\cdot\left(s_{c0e} + \frac{M\cdot s_{cme}s_{c0m}\Gamma_s}{1-\Gamma_s\,(\Gamma_c+(M-1)s_{cml})}\right)a_{ce} - N\cdot s_{c0e}a_{ce} \quad (6.41)$$

The fractional reduction in the output power can be deduced as

$$\frac{\left|b_{c0}^{'}\right|^2}{|b_{c0}|^2} = \left(\frac{N-M}{N}\right)^2 \cdot \frac{|s_{coe}(1-\Gamma_s\,(\Gamma_c+(M-1)s_{cml})) + M\Gamma_s s_{c0m}\,s_{cme})|^2}{|s_{coe}(1-\Gamma_s\,(\Gamma_c+(M-1)s_{cml}))|^2} \quad (6.42)$$

These expressions for the power reduction summarise the performance of amplifiers for a graceful degradation when M amplifiers fail with the impedance mismatch between the output port of the failed PAs and the combiner's input port. If these PAs are not matched with the combiner under healthy condition, this approach needs to be modified. Eccleston [220] deduced an upper bound in the efficiency due to the finite isolation and a mismatch effect of the combiner under the equal signal excitation ($b_{si} = b_{se}$ for $i = 1$ to N). However, the condition of equal signal excitation is rarely achieved in a practical SSPA system.

6.2.3 Analysis for Amplitude and Phase Imbalance

The graceful degradation analysis is useful for estimating the allowable power degradation in an SSPA system due to full or partial failure of PAs. It can predict the number of PAs, which can fail before maintenance of the system is required, for a specified power degradation. However, this analysis accounts for only the amplitude imbalance among PAs. In general, the degradation in the output power can happen due to the amplitude as well as phase imbalance, at various interfaces of the SSPA system. Being an active component, a PA is prone to such situation. Hence, there is need to account for all such possibilities in order to estimate its real time performance.

To illustrate the problem, let M out of N PA signals have same the amplitude imbalance (P_{ave} reduced by the factor p) and same phase difference, with respect to remaining (N-M) signals, by an angle δ_p. Then signals must be added vectorially, in a linear combiner, for obtaining P_{out}. Thus (6.12) can be written as

$$P_{out} = \frac{\eta_{c,max}}{N}\left[\left\{M\sqrt{pP_{ave}}\cos\delta_p + (N-M)\sqrt{P_{ave}}\right\}^2 + \left\{M\sqrt{pP_{ave}}\sin\delta_p\right\}^2\right] \quad (6.43)$$

After rearranging and using trigonometric identities we get

$$P_{out} = \frac{\eta_{c,max}}{N} P_{ave}\left[p\cdot M^2 + (N-M)^2 + 2M(N-M)\sqrt{p}\cos\delta_p\right] \quad (6.44)$$

This equation is useful for a small (N) system having amplitude and phase imbalance by a fixed factor. In general, an SSPA system may consist of unsymmetrical combiner ($s_{coi} \neq s_{coe}$) as well as PAs with unequal imbalance in their output signals ($a_{cn} \neq a_{ce}$). For such problem, the analysis, subject to the varying constraints or boundary conditions, is available in the literature. For such system, York [77] performed a statistical analysis, to deduce the effect of the amplitude and phase imbalance. Perhaps analysis reported by Gupta [76] is more useful for estimating the permissible tolerance in the uniformity of components used therein, as a function of the maximum acceptable efficiency degradation. He quantified the worst case efficiency for a specified imbalance, in b_{si}, under the assumption of a perfect matching among the PA, combiner and load (*viz.* $\Gamma_{si} = \Gamma_L = 0$). The salient points of this analysis are summarised here. For real time design, such imbalance may be controlled within a range by means of impedance tuning and tight fabrication tolerances.

Such ranges can be defined as follows

$$a_{min} \leq |a_{ci}| \leq M_b\, a_{min} \quad (6.45)$$

$$s_{min} \leq |s_{coi}| \leq M_S\, s_{min}$$

$$\delta_{min} \leq \angle(a_{ci}.s_{coi}) \leq \delta_{min} + 2\delta_{max}$$

Where,

M_b = is the ratio of maximum to minimum input (to the combiner) signal amplitude.

M_S = is the ratio of maximum to minimum amplitude of s_{c0i} for the combiner.

$2\delta_{max} =$ is the difference between the maximum and minimum phase of the product term $a_{ci}.s_{coi}$

For such PA-combiner system, the worst case or a minimum possible system efficiency [76] is given as

$$\text{Min}[\eta_{pc}] = \frac{4\, M_s\, M_b \cos^2 \delta_{max}}{(1 + M_s\, M_b\,)^2} \cdot \sum_{i=1}^{N} |s_{c0i}|^2 \tag{6.46}$$

The second factor $(\sum_{i=1}^{N} s_{c0i})$ reduces to $\eta_{c,max}$, for a symmetrical combiner, as discussed earlier. In actual case, the efficiency may be better than predicated by (6.46). This is a useful closed form expression to predict the worst case system performance for a general case, provided the combiner is matched to the PAs at its input and to the load at its output. Such usefulness is demonstrated below for the two different cases of the N-way combiner.

6.2.3.1 Case 1 (N=2)

Let, in a two way (N=2) symmetrical combiner ($M_s = 1$), one input signal has reduced in the amplitude (by a power reduction ratio p) and has undergone a phase shift (by angle δ_p) with respect to the other. Thus, for $M_b = \frac{1}{\sqrt{p}}$ and $2\delta_{max} = \delta_p$, the worst case efficiency from (6.46) is given by

$$\text{Min}[\eta_{pc}] = \eta_{c,max} \frac{2\sqrt{p}(1 + \cos \delta_p)}{\left(1 + \sqrt{p}\right)^2} \tag{6.47}$$

For this particular case, the computation can also be carried out using (6.44) with M/N=0.5, resulting in

$$\eta_{pc} = \eta_{c,max} \left(\frac{1}{2} + \frac{\sqrt{p} \cdot \cos \delta_p}{p + 1} \right) \tag{6.48}$$

A comparison of the worst case and actual efficiencies, calculated using (6.47) and (6.48), respectively, is given in Fig. 6.8, for various values of phase shift from 10° to 40°. It is assumed that the combiner is lossless and $\eta_{c,max}$ is equal to unity.

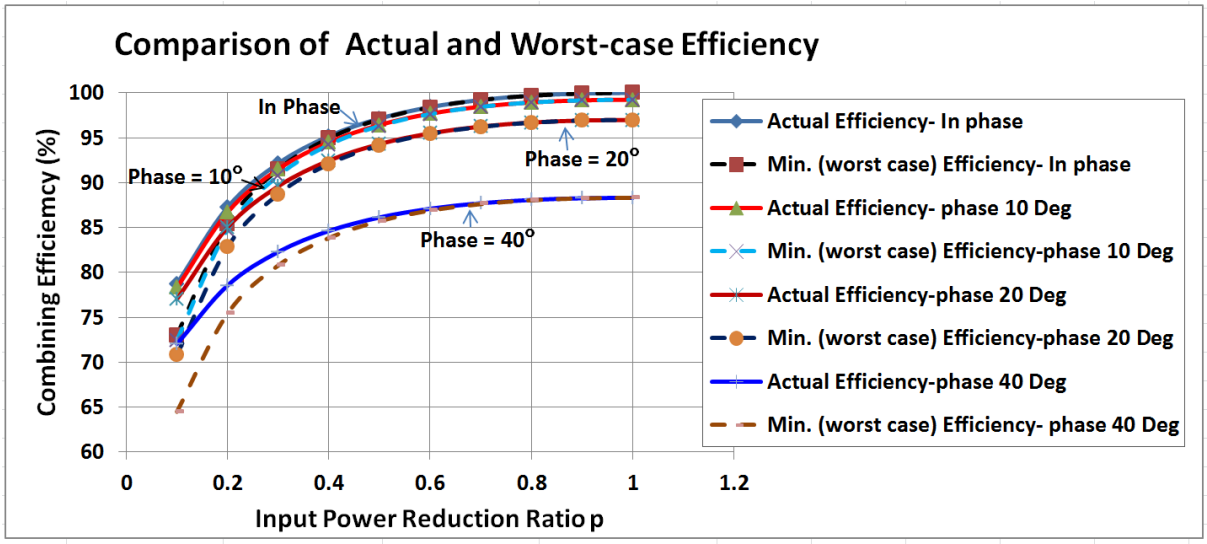


Fig. 6.8: Comparison of worst case efficiency with the actual efficiency

It can be seen that $\text{Min}[\eta_{pc}]$ is within 2% of η_{pc} for an input power reduction ratio p > 0.75, within 10% of η_{pc} for p > 0.52. It deviates increasingly from η_{pc} when p becomes smaller. As expected, efficiency falls rapidly with increasing imbalance in phase. In practice, it is easier to control the amplitude of the PA than its phase.

6.2.3.2 Case 2 (N-way System)

For an N-way system again let $M_s = 1$ for a symmetrical combiner. The parameters M_b and δ_{max} depends on the PAs employed in the SSPA system. Then worst case combining efficiency for such symmetric combiner is given by

$$\frac{\text{Min}[\eta_{pc}]}{\eta_{c,max}} = \frac{4\, M_b\, \cos^2 \delta_{max}}{(1 + M_b)^2} \tag{6.49}$$

Let the available power gain of PAs lies within ± ΔG dB of its nominal value Go. The available power gain G_i of the i^{th} amplifier, expressed in absolute scale, lies in the interval

$$10^{\frac{(Go-\Delta G)}{10}} \leq G_i \leq 10^{\frac{(Go+\Delta G)}{10}}$$

So the ratio of the maximum and minimum power gain is $10^{\frac{2\,\Delta G}{10}}$. Hence

$$M_b = 10^{\frac{(\Delta G)}{10}} \tag{6.50}$$

By substituting this value in (6.49), the worst case combining efficiency degradation can be determined. A contour plot showing degradation in the combining efficiency, as a function of the gain and phase deviation, is plotted in Fig. 6.9. The specific efficiency zones in this plot show that either gain or phase shift can be traded-off.

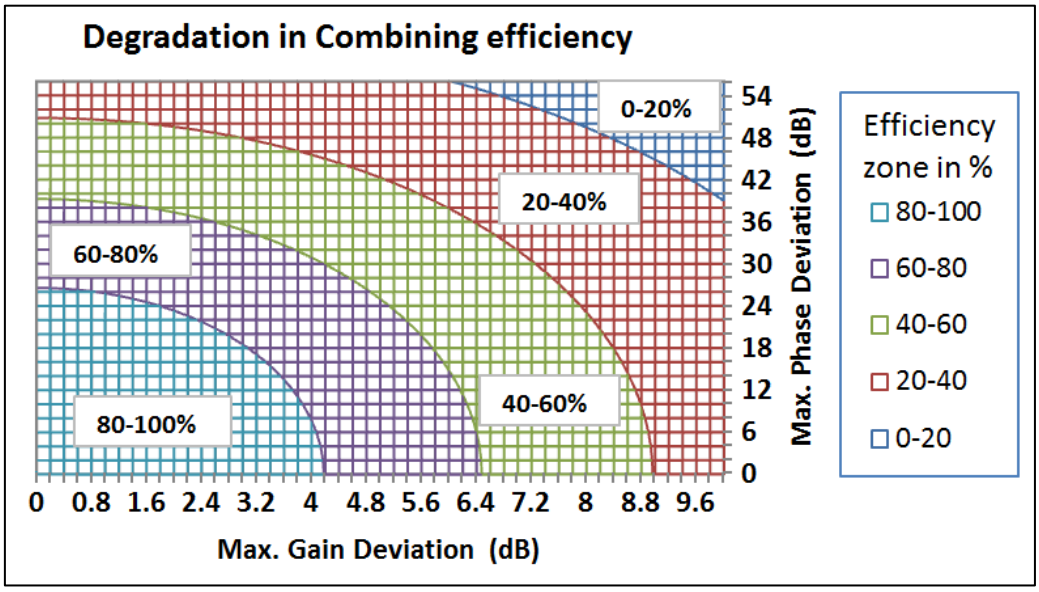


Fig. 6.9: Contour plot of efficiency as a function of gain and phase deviation

6.2.4 System Level Simulation for High Power SSPA Design

The analysis and guidelines from the research literature for specific cases, discussed in previous sections, are useful for the component and system level design of high power SSPA. However, in practice, for a real time SSPA system, more general situation needs to be considered. Due to the finite isolation s_{cij} (with $i \neq j$, and both varying from 1 to N) in a lossy combiner and nonlinear variation (AM-AM/AM-PM) in the PA output (b_{si}), an impedance mismatch (Γ_{si}) can occur between the PA output and the combiner input. Also the load

reflection Γ_L may be nonzero under some cases. One such case is possible when the multi-way combiner is a part of the multi-stage *divide and combine* hierarchy. Another such case is a particle accelerator where an RF cavity presents a dynamic load to the SSPA, in presence of the charged particle beam. Hence, the first order design study and prediction of the SSPA system behaviour needs to be fine tuned with the help of a computer aided system simulation.

In the present work, this study was carried out with the help of Visual system simulator (VSS™) [221] from AWR Corporation. It is a software suite to design the system architecture and formulate suitable specifications for each of the underlying components. In view of the modular and scalable SSPA architecture, a generic template, for the 16-way divider-combiner (Fig. 6.10), was developed in tune with the behavioural model (section 6.2).

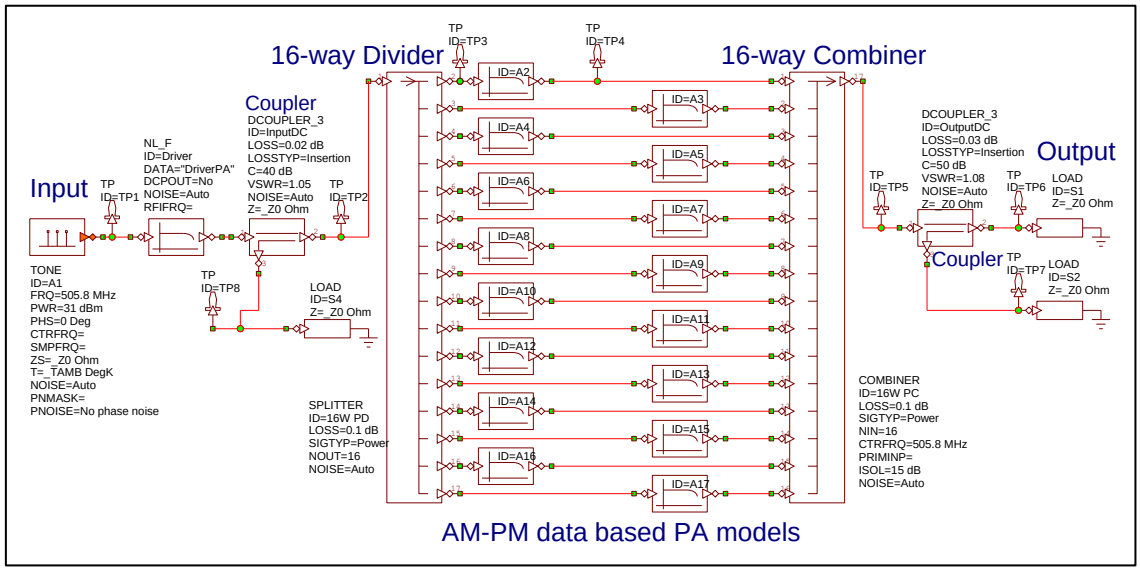


Fig. 6.10: Basic analysis/simulation template for (N=16) SSPA system

Depending upon final output power, many instances of this template can be properly combined as modular amplifier units. For each of the PA, its measured AM-AM and AM-PM data based model was used for its behavioural description. Once complete system is modelled, different calculation like RF power/gain budget and degradation in efficiency/output power can be performed for varying operating conditions. The design methodology devel-

oped at the component level, in earlier chapters, and system level studies, detailed in present and previous sections, have yielded fruitful outcome, in the form of successful physical implementation of four SSPA systems, as described next.

6.3 Experimental Investigation of SSPA Systems

In this section, designs of four SSPAs, all operating in UHF band, are described along with their high power measurement results. The first two SSPAs, each one with an output power of 2 kW CW, were designed at 352 and 505.8 MHz respectively. These two SSPA systems were used for high power testing of different passive components, designed afterwards. Rest of the two SSPAs, each one operating at 505.8 MHz, are capable of delivering 20 kW and 50 kW, respectively. These systems are sufficient in power for energising the actual accelerating structures. This exercise, along with fulfilling the purpose of this research work, provides the design and experimental data concerning real time performance of kW level SSPA systems.

6.3.1 2 kW SSPA systems

This section documents design of two SSPA systems, operating at the centre frequency of 352 MHz and 505.8 MHz, respectively. Each one of these systems is capable of delivering a CW RF power of 2 kW, at the respective centre frequency. This was the first design of kW level SSPA using multiple Pas (described in 2.6.1.2 and 2.6.1.3). It was started just after the successful design of 8-way power combiner and harmonic shorted PAs. The 8-way SSPA architecture (Fig. 6.11), for each of the systems, was selected after accounting the power handling capability of the underlying RF components. In this architecture, an RF signal generator feeds power to a 20 W low power driver (made using two cascaded LPAs) which in turn provide sufficient input power to a high power driver (HPA module). Its output signal is fed to an 8-way radial power divider, described in chapter 4. The divided RF signal is again

amplified by the respective HPA. All of these amplified signals are summed by using an 8-way radial power combiner, providing RF signal with 2 kW of power.

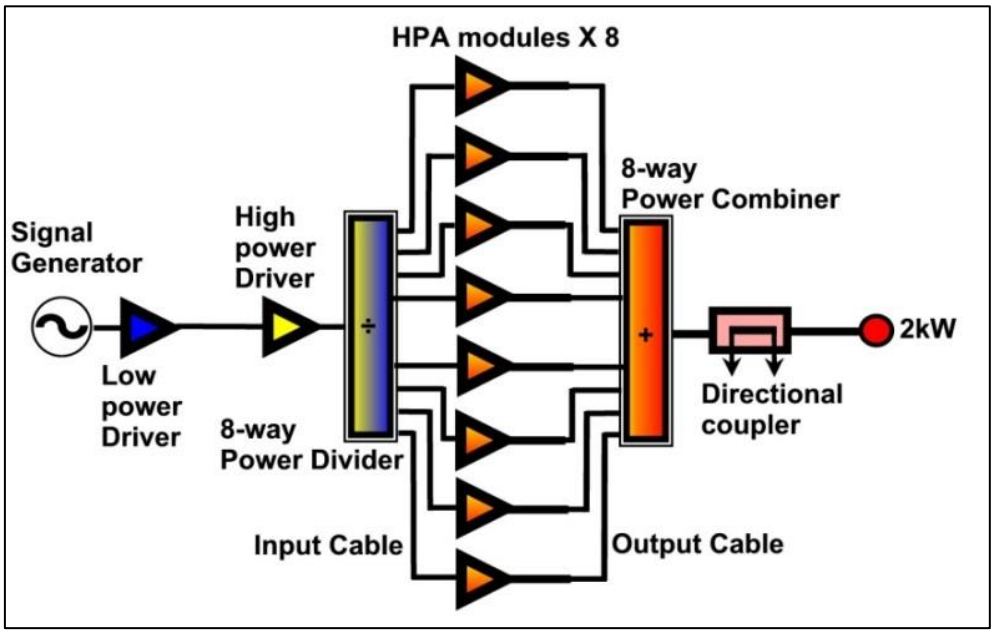


Fig. 6.11: 2 kW SSPA architecture

In this scheme, as mentioned in chapter 4, the 8-way radial combiner can provide combining efficiency better than 90%. For obtaining a minimum of 2 kW of output power, this combining efficiency poses a requirement 260 W (minimum) for HPA modules. Since, the HPA at respective frequencies were already designed with an RF power of 270 W and 400 W (chapter 2), obtained with the 28V, 20A DC bias system, this two SSPA-designs became quite feasible.

The calculated RF gain budget of two SSPA systems, along with the gain break-up for their constituent blocks, is tabulated in Table 6.1. The estimated gain, under ideal conditions, for the 352 MHz SSPA comes out as 53.3 dB, whereas for 505.8 MHz SSPA it is 65.2 dB. In order to compensate the power losses, likely to occur during the real time operation due to impedance mismatch at various junctions, the calculated output power from each system was kept above 2 kW.

Table 6.1: Calculated gain budget for designed 2 kW SSPA systems

Sr.	Constituent block	Parameter (Gain/loss)	Value for 352 MHz SSPA	Value for 505.8 MHz SSPA
1	Driver	Gain	30	30
2	Pre-amplifier	Gain	12	18
3	Power divider	Transmission loss	9.1	9.1
4	High Power Amplifier	Gain	12	18
5	RF cables	Insertion loss	0.2	0.2
6	Power Combiner	Transmission gain	8.9	8.9
7	Directional coupler	Insertion loss	0.2	0.25
8	Output RF cables	Insertion loss	0.1	0.15
	Complete SSPA	**Gain**	**53.3**	**65.2**
		Output power	**2200W**	**2200W**

For each system, four HPA modules (described in 2.6.1.2 and 2.6.1.3) were mounted on a common water-cooled copper plate (Fig. 6.12). This plate also serves as the RF ground plate for the high power PAs.

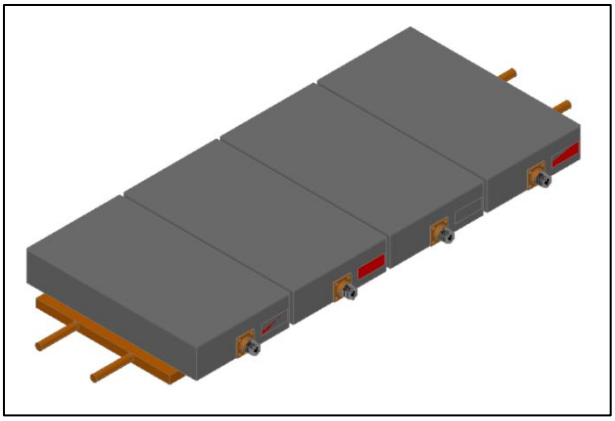


Fig. 6.12: Four HPAs mounted on a common copper based cold plate

Two such cold plates were mounted vertically in opposite direction inside a 32U euro cabinet, with power divider and combiner in the middle space. Including high power driver PA, total 9 HPAs were fabricated and tested for each system. The measured gain, power and drain conversion efficiency for these 9 HPAs at 352 MHz, measured at an input power of 13.8 W, are shown in Fig. 6.13. The conversion efficiency for these PAs varies from 60 to

62.6%. The power gain ranges from 12 to 12.4 dB. The complete SSPA system with all necessary interlocks and control unit was put in operation for high power testing (Fig. 6.14).

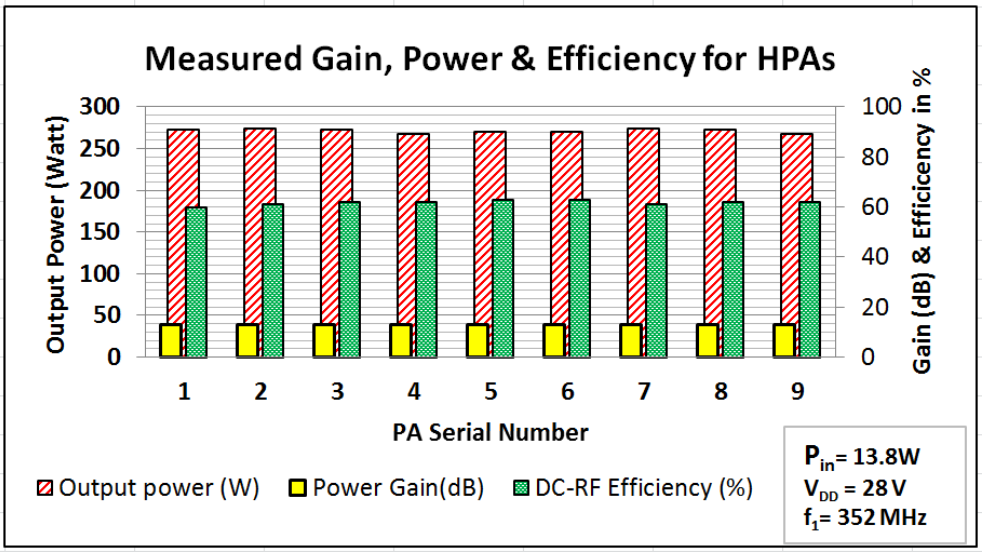


Fig. 6.13: Measured power transfer characteristics of 9 HPA at 352 MHz

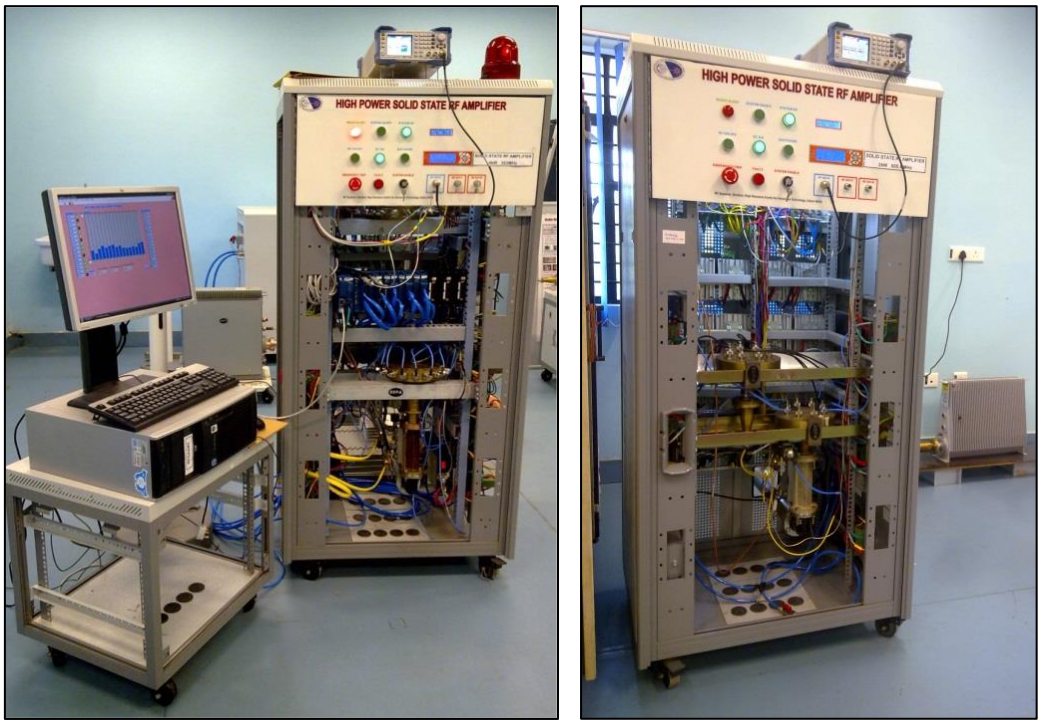


Fig. 6.14: 2 kW SSPAs, centre frequency - 352 MHz (left) and at 505.8 MHz (right)

The mechanical structure of each of the 32U racks was customised, to accommodate all of the RF components. Each SSPA has got its front panel with necessary operating switches,

indicators and emergency shut-off switch. For RF power sampling, the 5-kW directional coupler (described in section 5.3) was connescted, at the output of the 8-way power combiner. The RF measurement, for these two SSPA systems was carried out with a 5 kW dummy load from Bird™. These two systems can be remotely operated with the help of a computer.

The measured CW swept power transfer characteristics and frequency characteristics of these amplifier systems are shown in Fig. 6.15 to Fig. 6.18. For 352 MHz SSPA, as seen in Fig. 6.15, the power gain is nearly flat, maintaining a value of 50 dB above 1 kW of output power. Its input-output power characteristic is quite linear with wall-plug efficiency increasing along with the RF power and approaching nearly 35% at 2.1 kW.

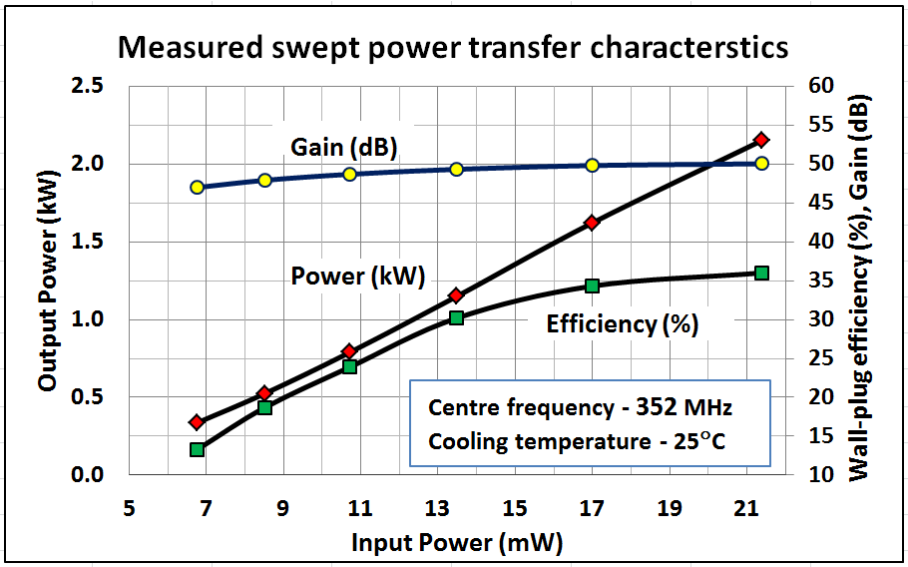


Fig. 6.15: Measured power transfer characteristics of 2 kW SSPA at 352 MHz

For high power RF sources wall-plug efficiency, defined as the ratio of net RF power to total electrical power consumed, is very important. The DC to RF conversion efficiency of the individual PA module is quite good (60-62.6%). But due to power consumption in peripheral components (DC bias supplies, control circuit, cooling components) and impedance mismatch at various junctions of this SSPA, the overall wall-plug efficiency has degraded. Its frequency response (Fig. 6.16) is symmetric around its centre frequency of 352

MHz, with a 1-dB bandwidth of 6 MHz. For particle accelerators' RF systems, narrowband response with 5-10 MHz 1-dB bandwidth is sufficient. The discrepancy in the calculated (Table 6.1) and the measured values of the gain and corresponding power is due to the losses, incurred in various real time circuit components and amplitude/phase imbalance at various interfaces.

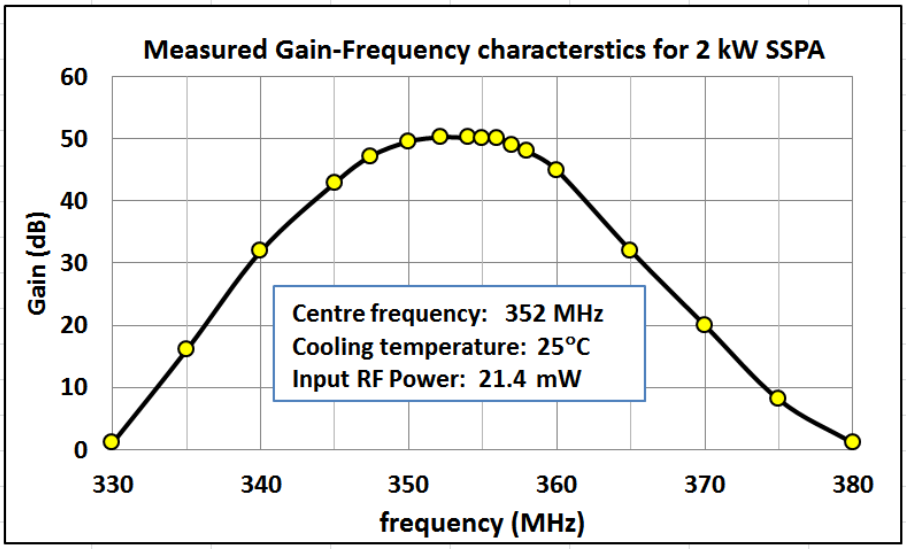


Fig. 6.16: Measured frequency response of 2 kW, 352 MHz SSPA

Similar measured result, for the 505.8 MHz SSPA system, shows (Fig. 6.17) an overall power gain of 60 dB with a wall-plug efficiency of 30%, at 2.1 kW of RF power. The frequency characteristic (Fig. 6.18) of this SSPA shows a maximum gain of 60 dB at 505.8 MHz, with a comparatively sharp roll-off at higher frequencies. Being the first design, emphasis was on qualifying the design rather than the investigation for imbalance.

These two SSPA systems were tested for several hours, at full CW power with a 5 kW dummy load, without any serious problem. The design and development of these SSPA systems was very useful as a breakthrough for the kW level system design. They were used for high power qualification of several passive RF components, designed afterwards. As the first experience of high power SSPA system, their measured data adds confidence for the

design methodology, developed during initial period, for solid state amplifier modules, power combiner/dividers and directional coupler (discussed in chapter 2, 4 and 5).

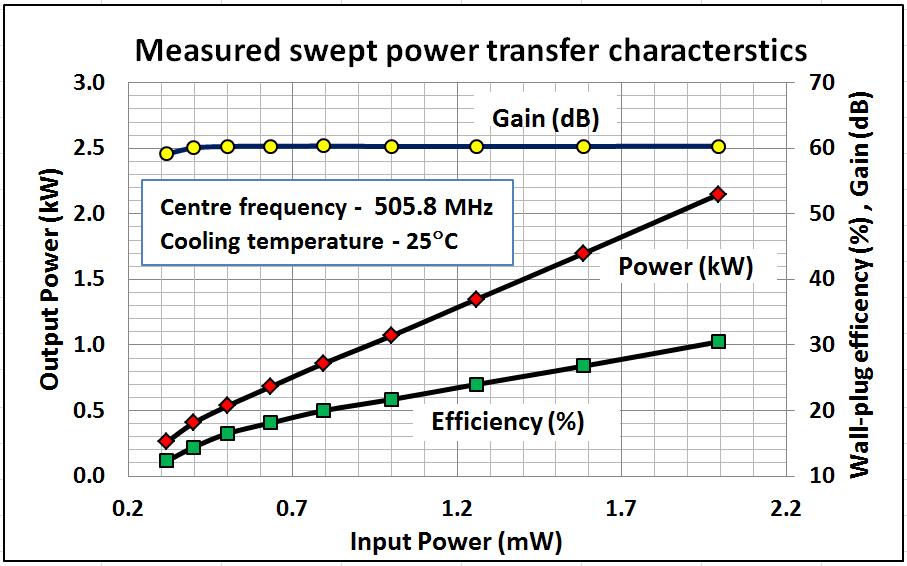


Fig. 6.17: Measured power transfer characterstics of 2 kW SSPA at 505.8 MHz

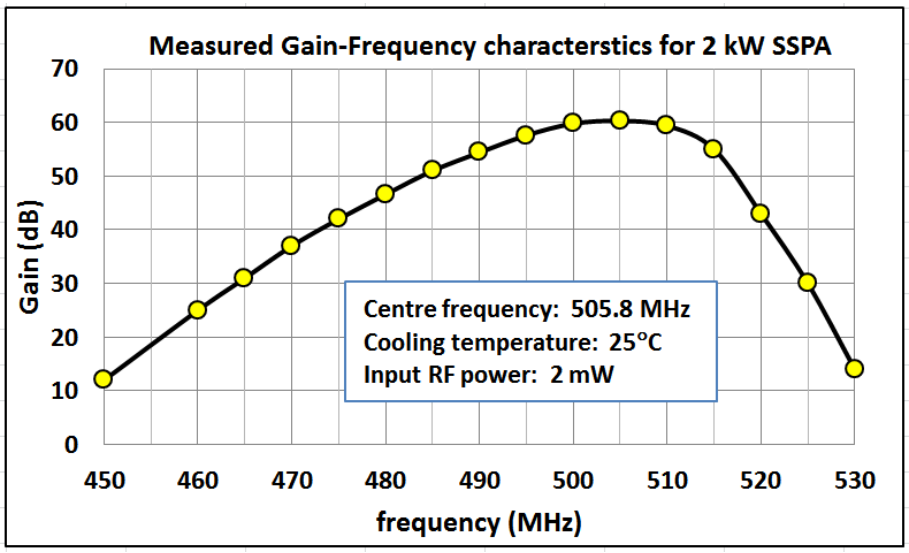


Fig. 6.18: Measured frequency response of 2 kW, 505.8 MHz SSPA

6.3.2 20 kW SSPA System

Encouraged by successful results, detailed in the last section, a 20 kW SSPA system was designed at 505.8 MHz, as a scalable and modular combination of two similar 10 kW amplifier units. Two such 10 kW units give 20 kW of output power after power combining with the

help of a 40 kW binary combiner. Based on the gain/power budget calculation and component selection studies, RF architecture was designed for this 10 kW unit. This architecture (Fig. 6.19) consists of two 5 kW sub-units. In each sub-unit, 16 PA modules (operating at 400 W, described in chapter 2), were combined using a 16-way power combiner. The outputs signals (at 5 kW), received from these sub-units, were combined with the help of a 2-way combiner, to get the required output power of 10 kW.

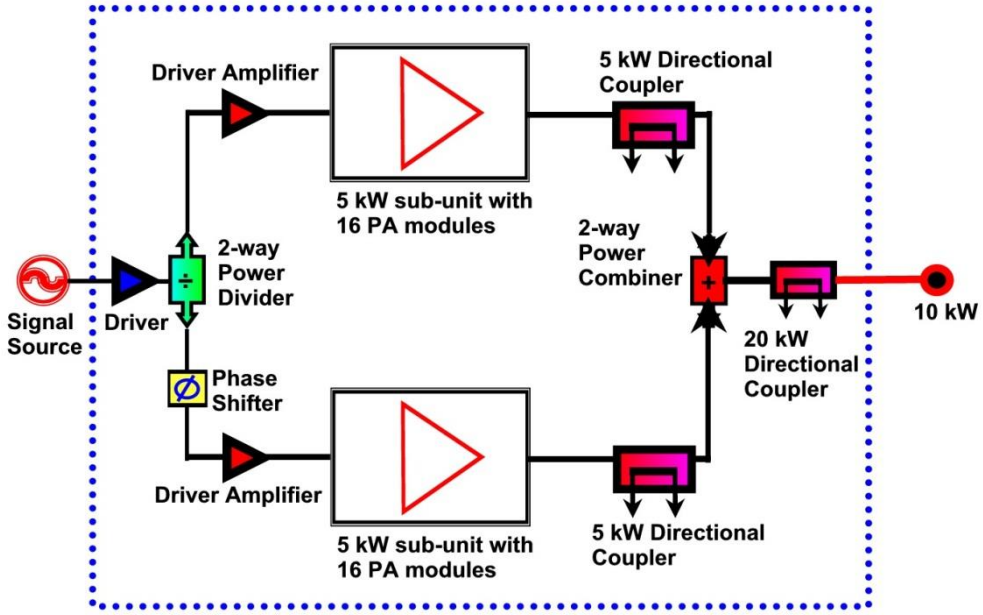


Fig. 6.19: RF architecture of 10 kW SSPA unit

Two directional couplers, operating at 5 kW and 20 kW respectively, were used to sample the RF power at each stage. A 16-way power divider splits about 300 W to feed inputs of all 16 PAs in each group. A 2-way divider splits input signal to feed this 16-way divider in each group, through a driver amplifier. A phase shifter inserted in one of the groups adjusts real time operational phase difference among two groups. A low power (1 kW) directional coupler, inserted between output of each PA and input of the 16-way combiner, monitors the forward and reflected RF component. These RF components, fabricated and tested for the 20 kW SSPA system, are listed in with their required quantity.

Table 6.2: RF components designed for 20 kW SSPA system

Sr.	RF components	Required quantity
1	Power Amplifier	64
2	5 kW, 16- way radial line power divider	4
3	5 kW, 16- way radial line power combiner	4
4	20 kW, 2 way Combiner (F2C)	2
5	40 kW, 2 way Combiner (G)	1
6	1 kW Directional coupler	64
7	5 kW directional coupler	2
8	20 kW bi-directional coupler	1

For each 10 kW unit, these components were mounted inside a 38U euro cabinet. Five PAs were arranged on a common water cooled copper plate as shown in Fig. 6.20. Three PAs were mounted on one side of this plate whereas two PAs are on opposite side, in order to efficiently utilise the thermal power as well as the space, inside the cabinet.

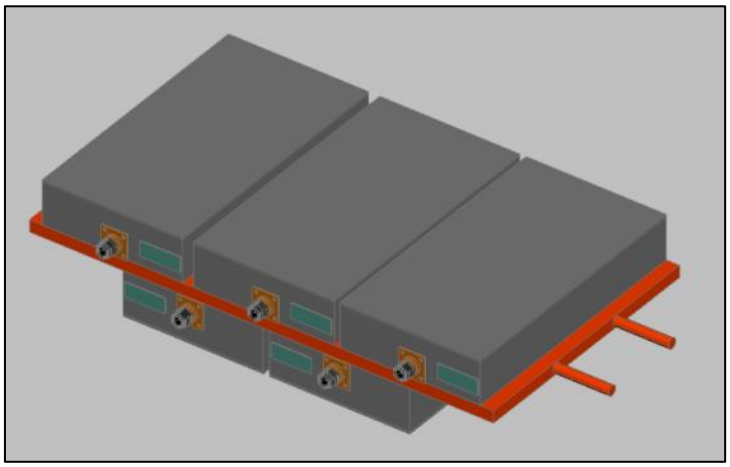


Fig. 6.20: Five PA modules mounted on a common cold plate

The major parameters of different dividers, combiners and directional couplers, drawing attention for this system integration, are insertion loss and deviation in transmission coefficient. The measured values of these parameters, reported earlier, inferred highly efficient divider/combiner and coupler with a symmetric performance of the first ones. Thus, the system performance is influenced appreciably only by the PA cluster. Being an active com-

ponent, its output signal has amplitude and phase variation from one piece to another. The measured amplitude and phase distribution of 32 modules, used in one of the10 kW unit, are shown in Fig. 6.21. The amplitude imbalance is quite low (< 0.3 dB) while maximum phase imbalance is nearly 20°. Fig. 6.22 shows the calculation performed for getting the operating power level and insertion loss of different components of a 5 kW sub-unit, for two operating conditions.

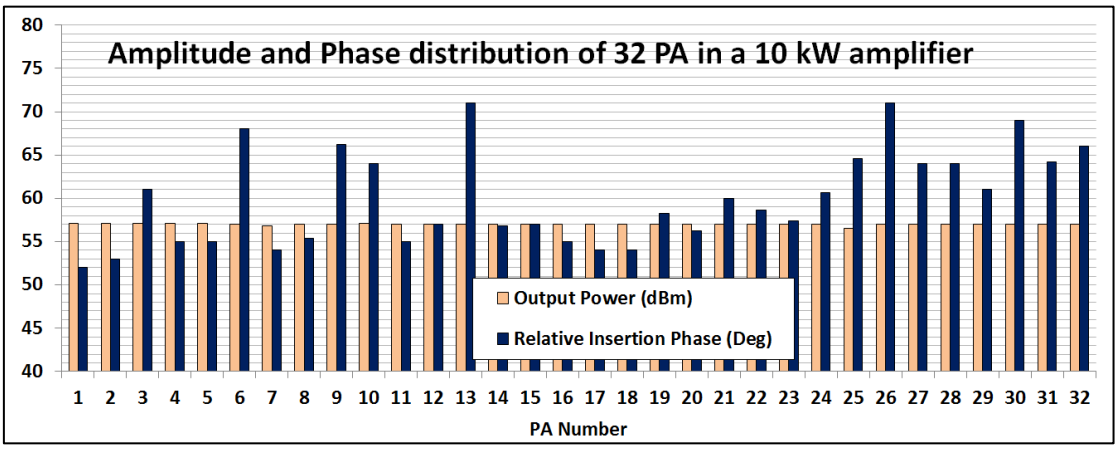


Fig. 6.21: Measured amplitude and phase distribution of 32 PAs, in a 10 kW unit

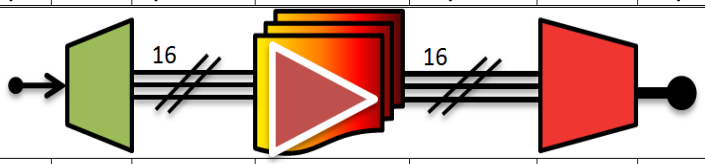
Operating Case	Item ->	Input	Divider	Input cables	Block of 16 PAs	Output cable	Combiner	Output	Effective Efficiency of Combiner η_c
	5 kW SSPA sub-unit ->								
Zero Imbalance	Loss/Gain (dB) ->		-0.05	-0.5	18	-0.3	-0.05		98.9
	Loss (%) ->		1.14	10.87		6.7	1.14		
	RF Power Level (W)	97.5	*97.5*	6.0	*5.37*	338.7	*5057.9*	5000	
	RF Power Loss (W)		*1.12*	0.66		22.6	*57.9*		
With Imbalance	*Imbalace loss (%)*						*88.2*		*87.2*
	Total Loss (%)		*1.14*	*10.87*		*6.7*	12.8		
	RF Power Level (W)	110.5	*110.5*	*6.8*	*6.1*	*384*	*5734.6*	*5000*	
	RF Power Loss (W)		*1.27*	*0.74*		*25.6*	*734.6*		

Fig. 6.22: RF power, loss and efficiency calculation for a 5 kW sub-unit of SSPA

It is clear that the components, contributing to the electrical power loss, are divider, input cables, 400 W PA modules, output cable and combiner. The RF power level here gives an

indication of operating level of the particular component. The values of insertion loss, used here, is the measured one. A power gain of 18 dB is used for all PA modules.

In the first case, this calculation was performed by assuming an ideal behaviour with zero imbalance, for these components. In the second case, an imbalance, observed in amplitude and phase of the PA modules (Fig. 6.21), was incorporated. All of the entries, in this case, are shown by blue and red colour. For getting an output of 5 kW, with zero imbalance, an input power of 97.5 W is needed for this sub-unit. For the input cable, attenuation is 0.5 dB, whereas for the output cable, which is shorter, it is 0.3 dB. As earlier stated, radial power divider and combiner are nearly lossless. In seen from the value of power level for the combiner, it needs to handle highest power of 5057.9 W. As power loss is due to only intrinsic loss of the component, the efficiency of the 16-way radial combiner remains same (98.9%), as reported in chapter 4. For the second case (6.46), with $M_b = 1.07$ (corresponding to amplitude imbalance in gain of 0.3 dB) and $\delta_{max} = 20°$, was used to get the worst case PA-combiner efficiency. It comes out equal to 88.2% (shown in red colour in Fig. 6.22). As such 16 input/output cables were used in this 5 kW sub-unit, the loss shown under input/output cable columns is for a single piece. In the calculation, this imbalance loss was attributed to the power combiner. Thus, loss due to this imbalance, combined with the intrinsic loss of the combiner, make its total loss equal to 12.8%. This increased loss brings down the effective combiner efficiency from 98.9% to 87.2%. It also increases the power handling capability of different components. It puts a demand of increased output power from the PA module, for maintaining the output of the sub-unit at 5kW. In practice, the output cables also present higher loss than shown here, due to handling of forward as well as reflected power. The latter one comes in picture due to amplitude and phase imbalance in PA outputs.

For the designed 20 kW SSPA, the electrical power budget, at 31°C of water temperature, was calculated (Fig. 6.23), based on the calculation for the first case. This budget includes the efficiency of bias power supply (SMPS) and drain conversion efficiency of the PA modules. The wall-plug efficiency for the complete system, from this calculation, comes equal to 42% in zero imbalance case. For the finite imbalance case, this efficiency comes equal to 36%.

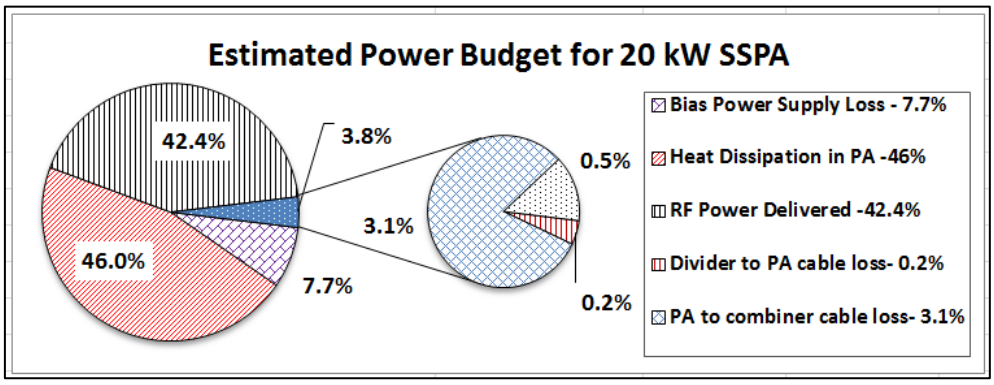


Fig. 6.23: Electrical power distribution for the 20 kW SSPA system

6.3.2.1 Power Supply and Data Acquisition

For bias power supply, in present scheme, every 400 W PA module was powered by a dedicated switched mode power supply (SMPS), capable of delivering 20 A at 50 V DC with the 3-phase AC input. Table 6.3 gives useful electrical specifications and safety interlocks of the system.

Table 6.3: Main electrical specifications and safety interlocks for 20 kW SSPA

Sr.	Parameter	Value
1	Front Panel indicators and control	System Enable, System ON/OFF, RF ON/OFF, system Shutdown, Emergency Trip and alert beep
2	Main interlocks	Water flow, fire alarm and SSPA ready
3	Primary Power	300-415V, 47-63Hz, 3 Phase
4	External Protection	Excessive Reflection, over temperature, RF overdrive
5	Input and output	Input- N connector, Output- 3-1/8” EIA port
6	Cooling	Water cooled at 31°C

For data acquisition, the 10 kW amplifier unit, together with its interlocks, form an independent system with its own local monitoring and data acquisition system performed by a graphical code, which was developed in-house using LabView™ RT software. From data monitoring and control point of view, the 20 kW SSPA system works as a distributed system, centrally coordinated by a master PC. The parameters acquired from each module are output forward and reflected power, and heat sink temperature.

6.3.2.2 20 kW SSPA: Overall System and Measured Results

The fully assembled 20 kW SSPA system (Fig. 6.24) was put for the RF measurement and testing. Each of the 10 kW units occupies a floor space of 1X1.2 m^2 with 2 m in height.

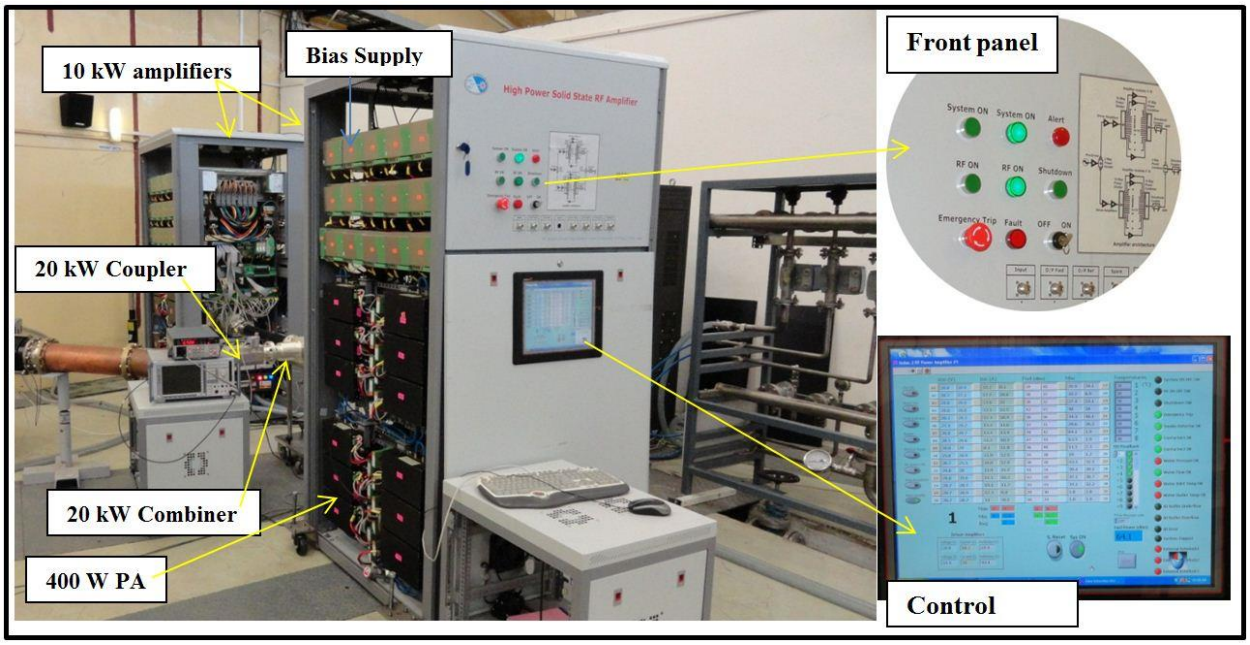


Fig. 6.24: 20 kW Solid State Power Amplifier system at 505.8 MHz

Due to high power involved, RF radiation intensity measurement was carried out for each unit. Very near to the PA modules, it was measured to be 0.08 mW/cm^2. At a distance of 1 m from the 10 kW units, it was measured as 0.02 mW/cm2, which is much lower than the permitted value (1.7 mW/ cm2 at 505.8 MHz). During operation of this system at full power, an average reflection of 46-47 dBm was observed at the third port of circulator, connected at

the output of each 400 W PA. This reflection was expected due to some variation in amplitude and phase distribution (Fig. 6.21) of PAs, used therein. The measured and calculated swept power transfer characteristics and gain of 20 kW system is plotted in Fig. 6.25.

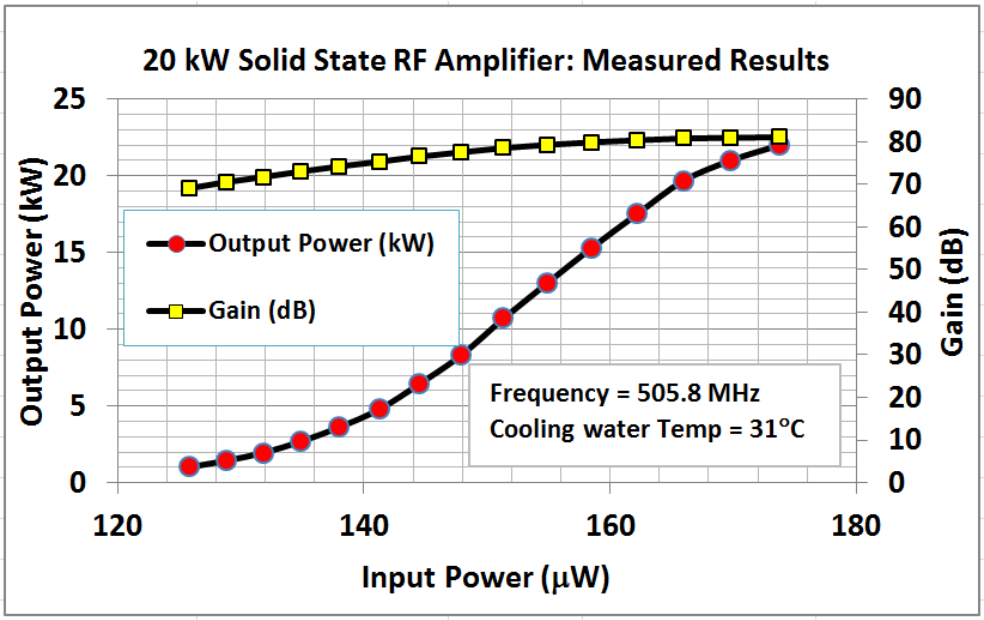


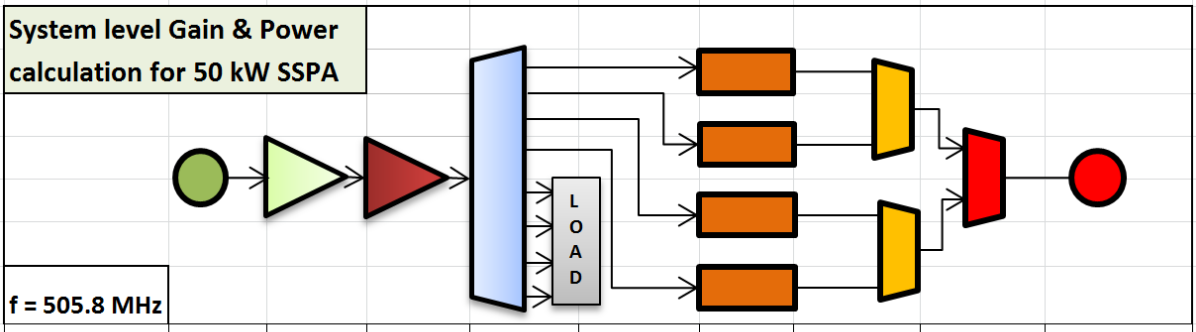
Fig. 6.25: Measured power transfer characteristics of 20 kW SSPA system

This characteristic is linear in the common operation region (5 kW onwards). As seen here, the one-dB compression point is beyond 10 kW with more than 80 dB RF power gain (including gain of driver amplifier). In actual operating conditions, the measured wall plug efficiency was slightly lower (34.8%). It must be due to the loss incurred due to reflection produced by the amplitude and phase imbalance in the output signals of PA modules.

6.3.3 50 kW SSPA System

The architecture for a 50 kW SSPA is based on a combination of binary and radial power dividing-combining approach materialized with the help of four RF amplifier units, each one capable of delivering 13 kW RF power. Enhancement in RF power from 10 kW (obtained for units used in 20 kW SSPA) to 13 kW was possible due to the successful design of 540 W harmonic tuned PAs, described in chapter 3. These 13 kW units were arranged in a two-tier

binary tree scheme using two-way combiners. This scheme is illustrated in Fig. 6.26, along with the calculated Gain/loss and code of each block, system gain and net forward power at each junction.



Item Code ->	A	B	C	D	E	F	G	H	
Building blocks in 50 kW SSPA ->	***Signal source***	***Pre-driver & RF cable***	***Driver & RF cable***	***8 port Power Divider***	***RF cable***	***13 kW PA Unit***	***40 kW RF Combiner & RF Cable***	***65 kW RF Combiner & RF Cable***	**System Gain (dB)** / **Power (kW)**
Gain/Loss (dB)	0	45.2	15.9	-9.1	-3	34.4	2.9	2.9	**89.2**
Power (dBm)	-12	33.2	49.1	40	37	71.4	74.3	77.2	**52.5**

Fig. 6.26: RF architecture and Gain/power calculation for 50 kW SSPA system

Inserted phase shifters adjust the operating time phase difference for each unit. Different directional couplers (not shown in Fig. 6.26) are used to sample RF power at various junctions. Such system allows easy serviceability and expandability with similar mechanical footprint and peripheral connections even for different frequency selection. Each of the 13 kW units (Fig. 6.27) is composed of two halves, each one having a group of 16 way divider, 16 way combiner (marked with FD and FC in Fig. 6.27) and 16 PAs. Each PA, capable of delivering 540 W at 505.8 MHz, is individually powered by a compact switched mode power supply (20 A at 50 V DC output and 3-phase AC input). The RF power from two such halves is summed with the help of a 2-way combiner (F2C) to get nearly 13 kW power. This ensemble, along with RF power divider (F2D), directional coupler, power supply, protection and monitoring hardware, forms a basic RF power (13 kW) amplifier unit, which is complete in all respect. For the system level simulation and analysis, characteristics and measured per-

formance evaluation of different components of this SSPA is necessary. It is presented in the next section.

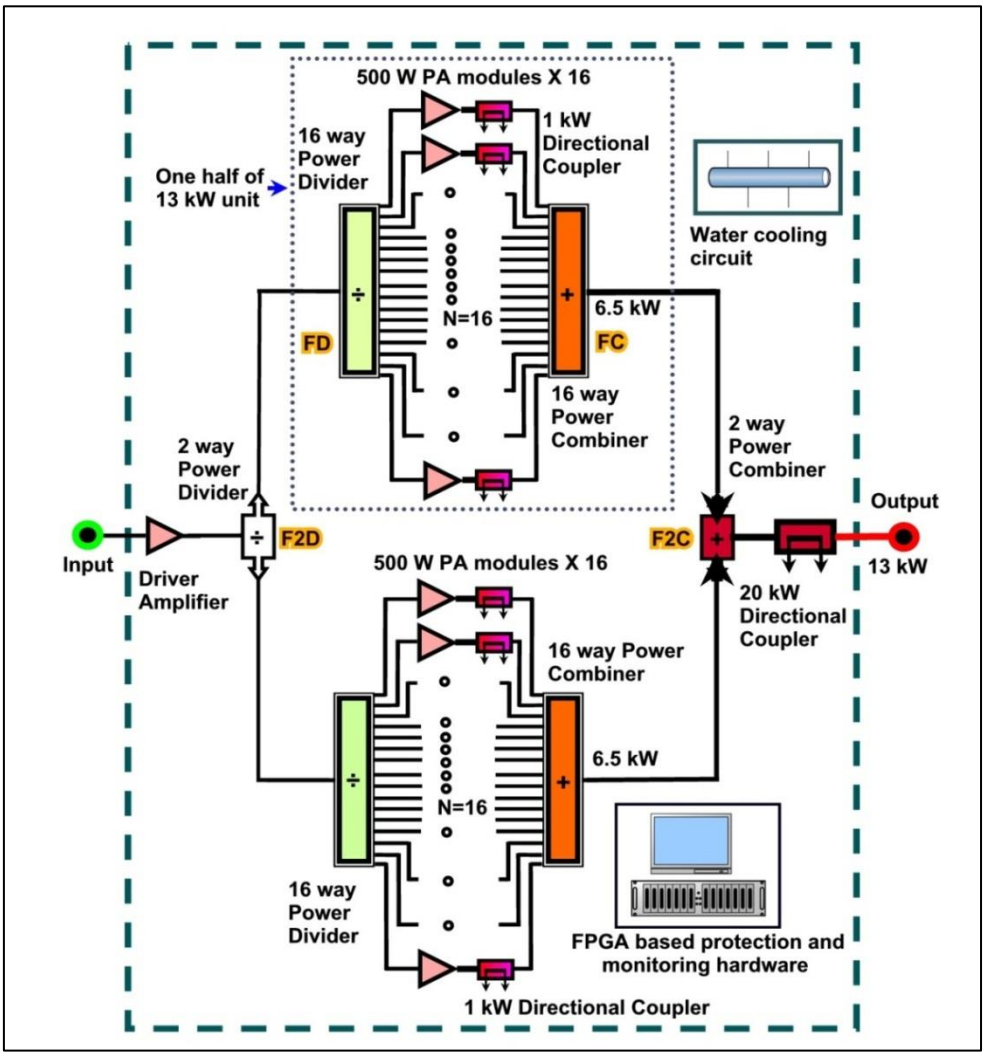


Fig. 6.27: RF hardware scheme for 13 kW SSPA unit

6.3.3.1 RF Performance Estimation before System Integration

Due to a large RF power involved, the performance estimation, prior to system integration, is desired for this 50 kW SSPA system. From RF point of view, its key components are 540 W PA, power divider, combiner and directional coupler. Their design detail was presented in chapter 3, 4 and 5. The measured amplitude and phase distribution of a group of 40 PAs (including spare ones) is shown in Fig. 6.28. Nearly similar data was obtained from the measurement of other sets of PAs.

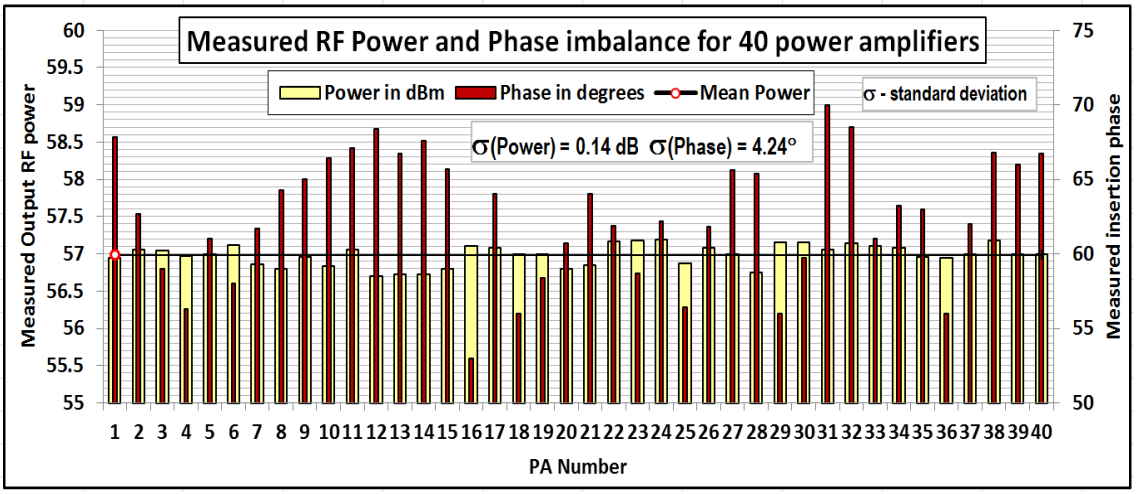


Fig. 6.28: Measured amplitude and phase imbalance for a set of 40 PAs

In order to account the quantitative effect of a large number of RF components, in the present 50 kW system, it is necessary to perform a system level performance analysis for taking mismatch at various interfaces, into account. For the present 50 kW SST, a system level analysis was performed in tune with the scattering parameter model, described earlier. These results were fine-tuned, for including other parasitic behaviour and nonlinear performance of the PA modules, by using the system simulator VSS™. Using two instances of the template, shown in Fig. 6.10, the 13 kW unit was analysed as a sub-system. Finally, using four such sub-systems, the simulation was performed for the complete 50 kW SSPA system. This analysis was performed for ideal as well as for mismatched (real time operating) condition. In the ideal condition, due to absence of impedance discontinuity and matched conditions, reflected power is zero. In this case, the power distribution among different components is shown graphically in Fig. 6.29. The SSPA system efficiency, defined as the ratio of net RF power to the electrical power consumed in major RF component and bias power supplies, is 50%. This efficiency includes actual physical losses in different RF components. The effective combining efficiency for 16-way combiner, calculated using this simulation, matches with the measured value of 98.9%.

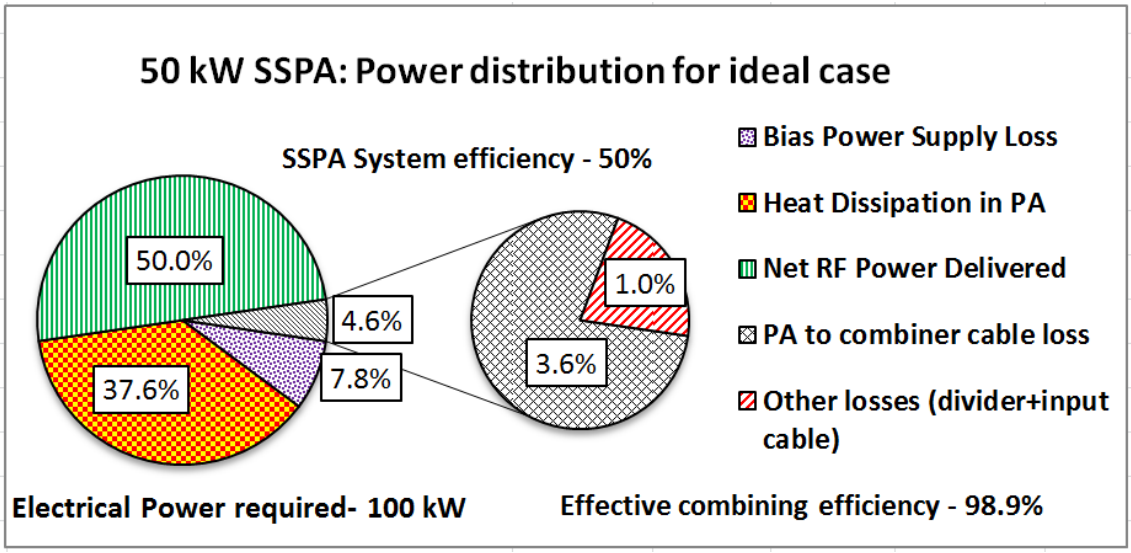


Fig. 6.29: Analysis results for system parameters in ideal case for 50 kW SSPA

In the mismatched condition, the average reflected power, at the interface of PA output and connecting branch port of 16 way combiner, was calculated from the system simulation. Its value comes equal to 46 dBm. This reflection loss arises due to the amplitude/gain and phase imbalance of the PAs, as evident from their measured data (Fig. 6.28). The resulting data for efficiency and power handling capacity for individual system blocks, both as a function of measured reflection at PA-combiner interface, help improving overall design. For such case the system simulation result for power distribution, is shown in Fig. 6.30.

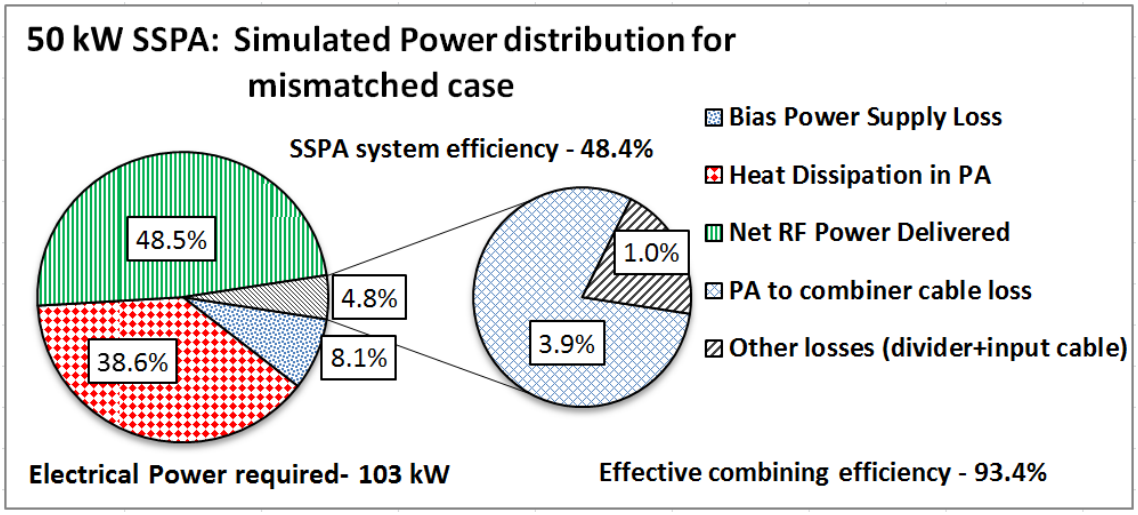


Fig. 6.30: Simulated results for system parameters in real case for 50 kW SSPA

The effect of increased reflection is manifested as a reduction in the net output power. In order to restore this power, more electrical (wall-plug) power is needed with a higher input drive. This increases RF power handled by RF components, correspondingly degrading the system efficiency. Quantitatively, this degradation can be attributed to an effective reduction in the combining efficiency of the 16-way combiner. For keeping the same system output, the heat dissipation in PAs and losses in the passive cables and components get increased, demanding more electrical power and degrading the system efficiency to 48.4%.

6.3.3.2 50 kW SSPA: Measured Performance

For high power RF measurement, the 50 kW SSPA (Fig. 6.31), complete with RF and ancillary components, was interfaced with an 80 kW RF water cooled dummy load. A high power circulator was placed for the safety of this amplifier. The supervisory and the interlock systems of this system were tested in advance.

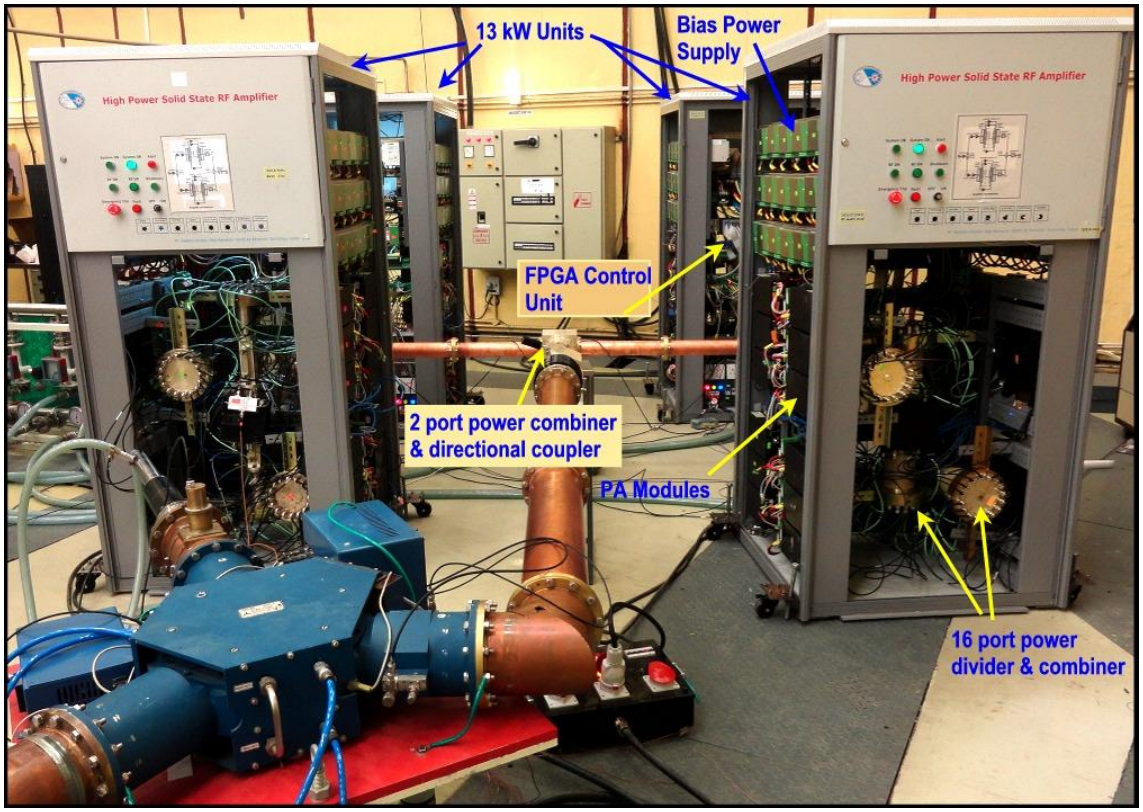


Fig. 6.31: 50 kW SSPA system

The directional couplers were characterized *in-situ* at high power. The RF measurements of output power, gain and efficiency was performed for each of the 13 kW units individually, followed by the same measurement for the complete 50 kW system. The swept power and gain characterization data of the 13 kW units are shown in Fig. 6.32. There is minor deviation in power characteristics for all four 13 kW units. This helps achieving the best possible efficiency of the integrated system. For all amplifiers, power transfer characteristic is linear in the common operating region.

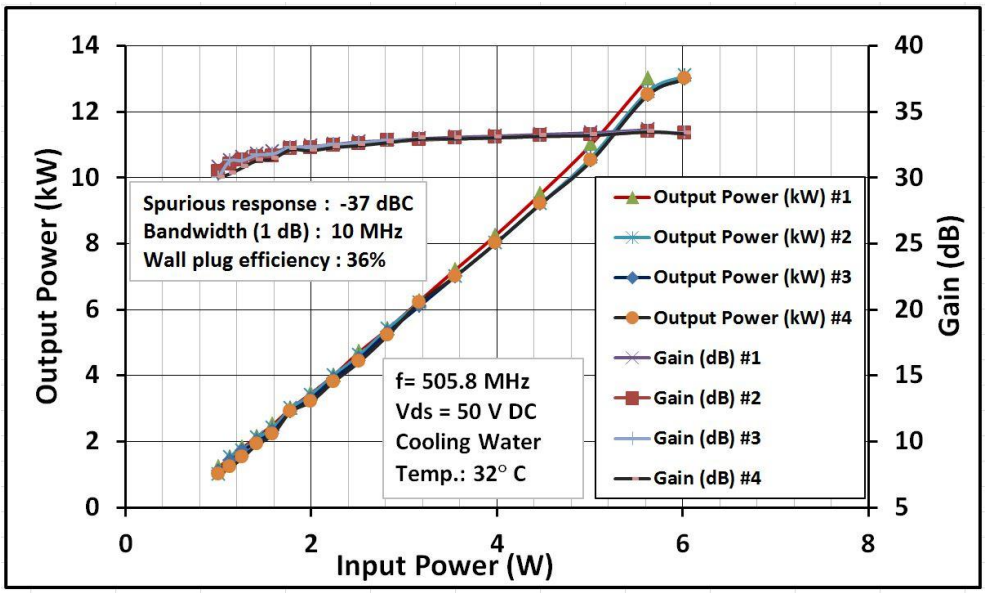


Fig. 6.32: Measured power transfer characteristics for 13 kW SSPA units

The input-output power characteristics, gain and system efficiency, for the 50 kW SSPA is given in Fig. 6.33. The power transfer characteristic is quite linear. The average power gain is 88 dB, while 1-dB gain compression point is beyond 52 kW of output power. The system gain is nearly same as the one calculated earlier (Fig. 6.26). The measured system efficiency (47.6%,) is slightly less than calculated value of 48.4%. Taking the power consumption in other ancillary sub-systems/hardware, the net wall-plug efficiency for the real time operation was measured as 34%. The measured RF radiation at full power was well below the safe limit at 505.8 MHz.

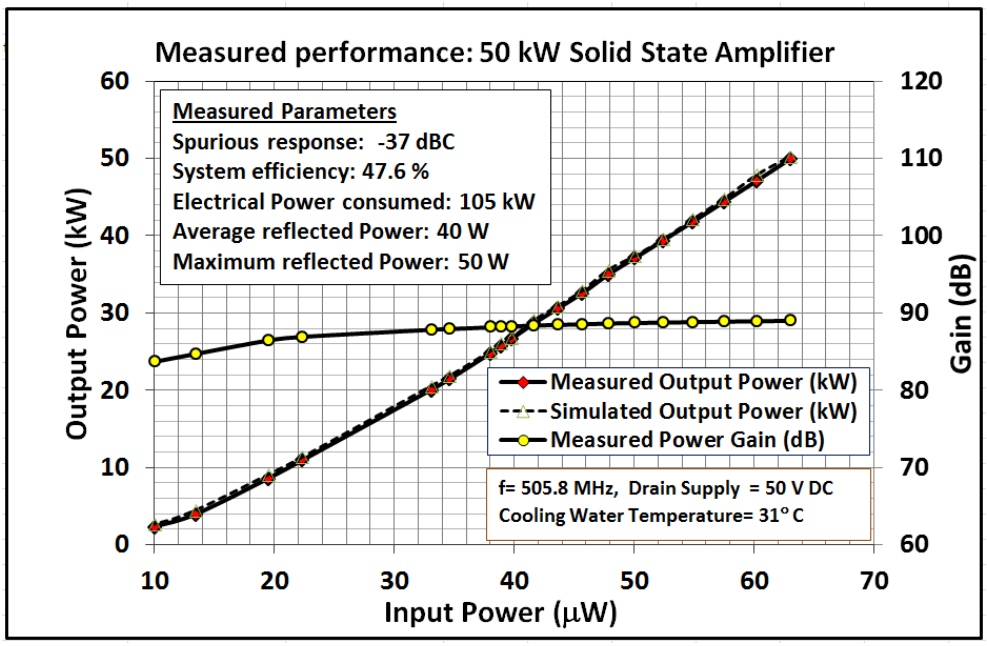


Fig. 6.33: Measured power transfer characteristics for 50 kW SSPA system

In this chapter analysis and design study, related with the graceful degradation and system efficiency, was carried out for the kW level solid state RF amplifiers. It helps making proper trade-off in the selection of amplifier architecture. With the help of a behavioural model and system level simulation, physical designs of four high power amplifier systems were carried out. By imposing tight tolerances in the design and fabrication of individual component, their measured performance, resulted in an acceptable behaviour. However, once these qualified components were integrated as a system, small deviation in amplitude and phase at various interfaces exhibited a loss of energy. Hence, system analysis and simulation of corporate and binary architecture was carried out to predict the real time system performance. The analysis and characterisation for the ideal case as well as the real time operation of kW level amplifiers, together with the measured data, put confidence in the proposed design methodology and also serves as a useful research effort.

Conclusion and Future Scope

In recent years solid-state technology based radio frequency and microwave amplifier, for communication as well as particle accelerators applications, have attracted a good amount of interest in the research community. Numerous advantages of this state-of-the-art technology and practical advancement made for superconducting accelerating structures have made this amplifier as a promising candidate for the kW level power source, compared to its vacuum tube counterparts. Researchers all around the world have made great efforts in order to redeem these promises. Its modularity, inherited from its architecture, makes fitment of different power levels inside the same system, with mass production of its elementary blocks.

Such amplifier system, operating in kW power regime, has modular and scalable architecture due to the moderate power handling capacity of active and passive components used. In view of this, the present research work was focused on the suitable design methodologies for RF power amplifier module, power divider, combiner and directional coupler; all at high power to cater typical requirement of the particle accelerator. The conventional harmonic shorted or tuned load operating modes of amplifier like Class A, B and AB are popular and were studied experimentally in low power (30 W) to high power (270-400 W) regime, at UHF. It helped investigation of emerging design technique of harmonically tuned modes, which are superset of conventional ones.

In harmonic tuned modes, the efficiency and output power of the amplifier module is achieved with enhanced functionalities previously not possible. In these modes nonlinear current and voltage waveform are wave shaped with proper multi-harmonic terminations on load side, to reduce the power dissipation inside the solid state device. This mode seems to address design challenges associated with the LDMOS devices having adequate drain-source

capacitance. Study of such harmonic tuned design space was carried out theoretically and experimentally. The excellent results obtained for these designs demonstrate the success of the developed methodologies for high efficiency and high power solid-state amplifiers.

For N-way power combining, among different configurations, the radial combiner was voted, due to its certain advantages. Different combining structures with 8, 16 and 2 ports were investigated for their suitability at high power and in the long-run operation. Similarly for high power measurements, three types of wideband and fabrication-friendly rigid directional couplers, using square coaxial lines, were designed in the UHF band, at different RF powers. The study of binary divider with loading of dielectric resonator opens a new avenue, for achieving multi-frequencies operation and unequal power division.

These efforts at the component level, made the system design possible for kW level solid state amplifiers. By developing scattering parameter based models, designs of 2 kW, 20 kW and 50 kW amplifiers were carried out. Their analysis, system level computer aided simulation and experimental study were performed for evaluating the system gain, power distribution and efficiency degradation due to impedance mismatch; resulting from the amplitude/phase imbalance in the system components. It was seen that the phase imbalance among signals, feeding to the combiner, is more crucial compared to amplitude imbalance.

The excellent experimental results obtained in these designs demonstrate the success of the investigated design methodologies. Also this exercise provides useful data for performance evaluation, life testing and efficiency enhancement for research community associated with high power solid-state radio frequency and microwave amplifiers.

There are few issues that may be subject matter of further research in the near future. During the course of the present work it was felt that appropriate circuit models of radial combiner is not readily available, even in the circuit simulators. Such model can be established by studying its electromagnetic behaviour and by using its circular symmetry. The

performance enhancement results, obtained by incorporating dielectric resonator with the binary divider, need to be backed by a dielectric loading theory. For high power LDMOS devices, circuit models for harmonic balance simulation are available only from their manufactures. If better models incorporating nonlinear input as well as output capacitors are explored, they will be very useful for the amplifier designers. For harmonic tuned modes, role of balanced to unbalance transformer is important in wave shaping. This role may be further investigated to design newer transformers for efficiency enhancement. For similar modes, role of newly introduced injection power amplifier may be further investigated. In the present work, effect of the amplitude/phase imbalance was studied for high power amplifier, encompassing multiple components. However, a mechanism needs to be devised inside individual amplifier module so as to compensate this imbalance automatically with the help of some data acquisition and control system. Alternatively amplitude and phase trimmers can be incorporated with the power combiner itself. The system level simulation is a versatile tool and it needs to be used for the SSPA system with dynamic load like RF cavity. The model of RF cavity can be appropriately substituted by VHDL coded FPGA emulator. Such exercise can generate data closer to real time operation. Last but not the least, thermal management issues have not been addressed in this work. LDMOS devices are very sensitive to any increase in junction temperature during operation. With increasing power of transistor, one needs to study better liquid cooled or compressed gas cooled heat sink design. Finally from system integration point of view, there is requirement of compact system with higher RF power per unit volume of cabinet/enclosure. Most of the space in such enclosures is occupied by RF cables connecting different components. If some integrated structure is devised, to accommodate amplifier modules, divider and combiner in close vicinity, while maintaining ease of operation and serviceability, it can save lot of energy, which otherwise is lost in such connecting RF cables.

Appendix A: RF Transistor

For the radio frequency and microwave transistors, various improved structures have been proposed, including HBT, VDMOS, LDMOS, MESFET and HEMT. For small signal operation, BJTs are popular while for the upper microwave range (> 4GHz), HBT promise to be a good candidate. For high power operation, in 100 MHz to 4 GHz range, the MOSFETs outperform in terms of input/output impedance, thermal runaway, simple bias design, circuit stability, higher VSWR withstanding capability and better distortion characteristics. This brief discussion is restricted to the one popular variant of MOSFETs (known as LDMOS) and key properties of different semiconductor materials, used for such transistor.

The functional characteristics of an RF power transistor are tied with its frequency of operation, output power, its power gain, DC voltage of operation and package configuration consistent with circuit construction techniques. Hence, the RF transistors need to be constructed with different enclosure/package. A power transistor die is, created by combining a large number of *small-signal* transistor cells on a single die, as shown in Fig. A.1. Its leads are in the form of a ribbon for reducing the lead inductance [120].

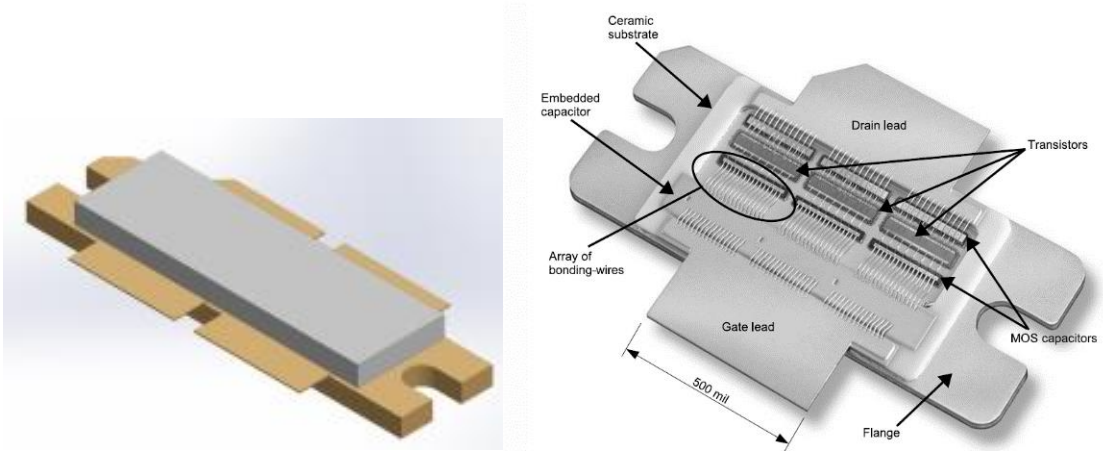


Fig. A.1: RF power transistor in SOE package with (right) and without (left) lid

Such ribbon or stripline type package is known as stripline opposed emitter (SOE) package. As the power transistors are mostly used in "push-pull" configuration, the twin device package (shown in Fig. A.1-left side) is commonly referred to as Gemini or push-pull SOE package. Its base plate/flange, supporting the die and hermetic package, is gold plated and it possesses a low thermal resistance to serve as a common return path for the RF and DC bias currents.

For high power applications, MOSFETs need a reasonable, short channel length and a low doping level in the drain region. Having a low doping level in the drain will ensure the space charge layer at the drain-channel junction spreads into the drain regions instead of the channel region, providing a large blocking voltage capability. Double-Diffused MOSFET (DMOS) transistor and fabrication technology diverged into two main subgroups depending on the direction of current flow, lateral DMOS and vertical DMOS transistors (LDMOS and VDMOS, respectively). Beginning in the early 1990s, RF LDMOS (Fig. A.2) device gained wide acceptance for high-power RF power amplifier applications for frequencies, ranging from 1 MHz to nearly 3.5 GHz.

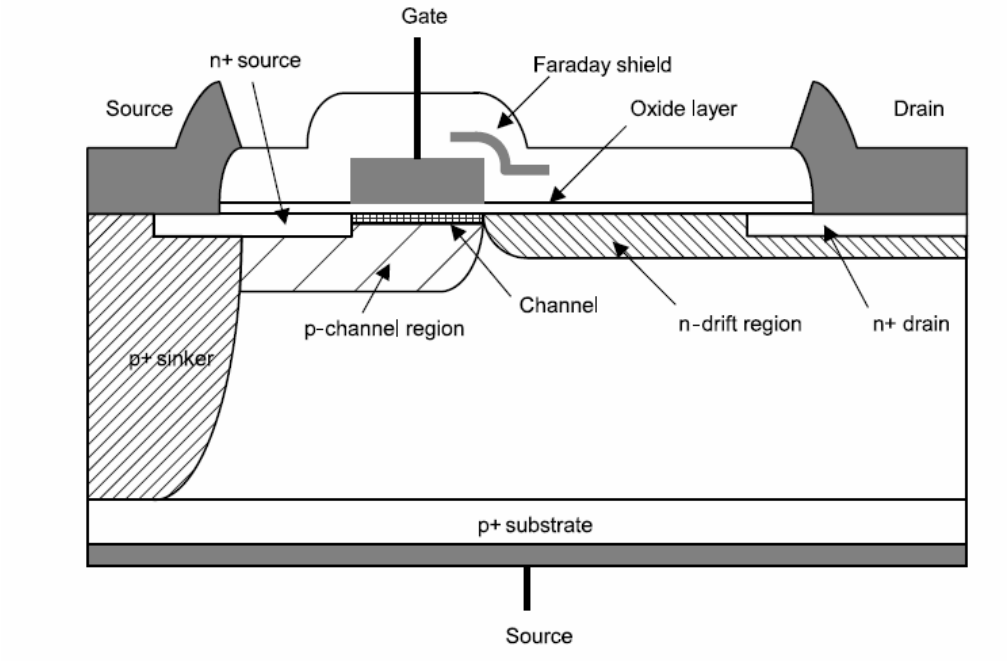


Fig. A.2: Typical LDMOS structure (courtesy – Freescale Inc.)

The difference between this structure and a conventional lateral MOS transistor is that the channel length does not depend on the lithography step; rather it depends on the diffusion processes. Due to its unique structure, it can be easily grounded to an electrically and thermally conductive heat-sink. It also has a very low resistance and inductance connection from the source terminal at the top of the wafer to the back side of the wafer, which simplifies the design of the package, and eliminates the need for source bond wires. Without the source wires, it does not have the additional source inductance resulting in its high gain. The asymmetrical p-channel region of the LDMOS transistor, is created by using the gate to self-align a moderate dose p-type implant to the source edge of the gate of the transistor. A subsequent furnace anneal is used to laterally diffuse (the "D" in LDMOS) this implant into the channel. The source-side structure is completed by the self-aligned implant and subsequent diffusion of the heavily doped n-type source/drain implant. This transistor has significantly lower parasitic capacitances, by virtue of its structure; this feature results in an extended high-frequency response compared with the vertical structure. The gate to- source capacitance, and the drain-to-source capacitance, have inherently lower values, compared with the VDMOS structure. The gate bonding pad and the entire metal layer connected over the field oxide result in a substantial capacitance from the pad to the drain substrate. For this reason, a lightly doped diffusion (p^-) can be placed under the pad. This diffusion layer is connected to the source region and acts as a conductor between the gate pad and the drain substrate, reducing the effect of gate to drain capacitance. The implant done for this method is called the Faraday shield implant. It shifts the parasitic gate-field capacitance over to the input side of the device, which dramatically improves the frequency response. LDMOS allows for a replacement of the toxic BeO packages by environment-friendly ceramic or plastic packages. At UHF and lower microwave frequencies, the LDMOS is especially useful, since the direct grounding of its source eliminates bond-wire inductance that produces negative feedback and

reduces gain at high frequencies. Currently, packaged LDMOS devices [115], typically operating from 28 to 50 V DC supplies, are available with output powers over 1000 W at UHF.

Several competing semiconductor device technologies serve as the backbones in making these RF transistors. They range from silicon to III-V compound semiconductor-based devices. Silicon based devices, with its low-cost, high-volume production, have served the market for many years. The compound semiconductor based devices take advantages of their intrinsic material properties and offer superior device performance in high-frequency applications. In III-V semiconductor materials, GaAs based MESFETs and HBTs, InP based PHEMTs and HBTs are classical devices of choice in RF circuit/MMIC applications. Shown in Table A.1 is an elective list of physical properties of major semiconductor materials. These properties set the fundamental limitation of every device technologies. As seen in this table, a higher bandgap corresponds to a higher breakdown field, which in turns implies the capability of the device to allow higher output voltage swings and thus to attain higher output power levels. Moreover, the high operating and breakdown voltages result in larger output impedance values for a given current density, making impedance matching easier.

Table A.1: Semiconductor properties relevant for RF Transistors

Property ↓ Material⟶	**Si**	**Ge**	**GaAs**	**GaN**	**4H-SiC**	**InP**
Electron mobility ($cm^2\ V^{-1}\cdot s^{-1}$)	1500	3900	8500	1000	900	5400
Hole mobility ($cm^2\ V^{-1}\cdot s^{-1}$)	450	1900	400	350	120	200
Bandgap (eV)	1.12	0.66	1.42	3.2	3.23	1.35
Avalanche field (10^5 V/cm)	3.8	2.3	4.2	50	35	5.0
Saturated drift velocity (10^7 cm/s)	0.7	0.6	2.0	1.8	0.8	2.0
Saturation field (10^3 V/cm)	8		3	15	25	25
Thermal conductivity at 25°C(W/cm·°C)	1.4	0.6	0.45	1.7	4.9	0.68
Dielectric constant	11.9		12.9	14	10	8
Substrate resistance (Ω- cm)			>1000	>1000	1–20	>1000

Similarly, the dielectric constant is an indication of the capacitive loading of a device, thus a low value is generally desired. By increasing the power density in actual devices, the heat disposal becomes a major issue. Hence, the thermal conductivity of the adopted material system becomes critical, to avoid the degradation of the device performance and reliability. Regarding the substrate resistance, this figure becomes critical in laterally developed devices, since an insulating substrate decreases losses at microwave frequencies. Finally, the mobility of electron and hole determine the electrically ON resistance and knee voltage of a power device. A low mobility results in increased parasitic resistance, increased losses and reduced gain, thus clearly limiting the frequency of operation.

Due to highest electron mobility, GaAs material is good choice at microwave for low-noise amplifier. InP-based device can yield the fastest transistors in GHz range at low power. The wide-bandgap materials like GaN and SiC have established a strong commercial base for TV and cellular communication segments, overlapping in frequency with majority of the next generation RF systems for particle accelerators. One advantage with SiC and GaN is due to their larger tolerance to radiation than silicon. This is mainly due to their 3 times larger bandgap, which reduces the electron-hole-pair formation. SiC benefit from the excellent thermal conductivity as device substrate. However, its electron mobility is significantly lower than that of GaN. The processing cost of SiC devices is currently much higher than Si and GaN LDMOS devices. Low thermal resistance and good drift velocity make GaN material perfect for high-power RF applications. Few years back, a new power MOSFET (Super Linear MOSFET) concept has been introduced by B. J. Baliga [127]. Unlike prior MOSFETs which operate by pinch-off of the inversion layer in the channel, the new concept is based upon retaining the channel in the linear mode of operation and relying upon current saturation by utilizing the velocity-field curve for silicon.

Appendix B: Different Waveforms for Drain Current

The regions on Smith chart, where the harmonic tuning can be profitably implemented, are strictly functions of the drain current waveform. The drain current with reduced conduction angle is the most common case. Commonly adopted waveforms for the drain current [80], for different bias and input conditions, are categorized as follows.

1. Reduced angle conduction (Fig. B.1)

$$I_{ds}(\vartheta) = \frac{I_{max}}{1 - \cos\left(\frac{\Phi}{2}\right)} \cdot \left[\cos\vartheta - \cos\left(\frac{\Phi}{2}\right)\right]$$

Here, the current is nonzero only for a small duration ($-\frac{\Phi}{2} < \vartheta < \frac{\Phi}{2}$). Different terms in this expression are with respect to Fig. B.1.

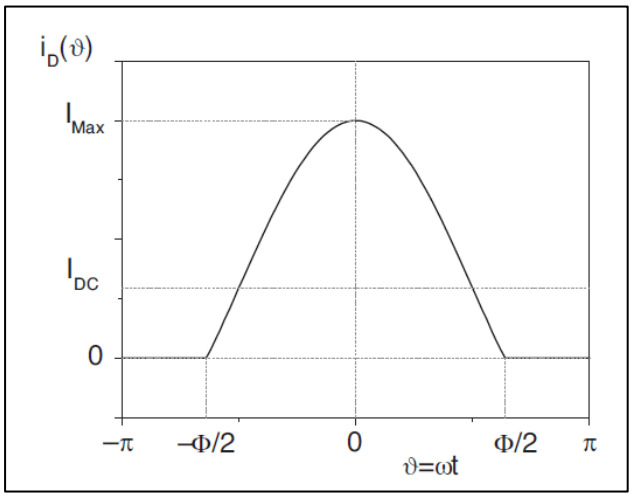


Fig. B.1: Truncated sinusoidal waveform

The expression for DC component, fundamental and first few harmonics are given as

$$I_{DC}(\Phi) = \frac{I_{max}}{2\pi} \cdot \left[\frac{2\sin\left(\frac{\Phi}{2}\right) - \Phi\cos\left(\frac{\Phi}{2}\right)}{1 - \cos\left(\frac{\Phi}{2}\right)}\right]$$

$$I_1(\Phi) = \frac{I_{max}}{2\pi} \cdot \left[\frac{\Phi - \sin\Phi}{1 - \cos\left(\frac{\Phi}{2}\right)}\right]$$

$$I_2(\Phi) = \frac{I_{max}}{6\pi} \cdot \frac{3\sin\left(\frac{\Phi}{2}\right) - \sin\left(\frac{3\Phi}{2}\right)}{1 - \cos\left(\frac{\Phi}{2}\right)}$$

$$I_3(\Phi) = \frac{I_{max}}{6\pi} \cdot \frac{\sin\Phi\,(1 - \cos\Phi)}{1 - \cos\left(\frac{\Phi}{2}\right)}$$

For $\Phi = \pi$ it becomes

$$I_{ds}(\vartheta) = I_{max}\left(\frac{1}{\pi} + \frac{1}{2}\cos\vartheta + \frac{2}{\pi}\sum_{n,even}\frac{(-1)^{\frac{n}{2}+1}}{n^2-1}\cos n\vartheta\right)$$

2. Quadratic drain current (Fig. B.2)

$$I_{ds}(\vartheta) = I_{max} \cdot \left[1 - \left(2 \cdot \frac{\vartheta}{\Phi}\right)^2\right]^2$$

The expression for DC component, fundamental and first few harmonics are given as

$$I_{DC}(\Phi) = \frac{4\,\Phi \cdot I_{max}}{15\,\pi}$$

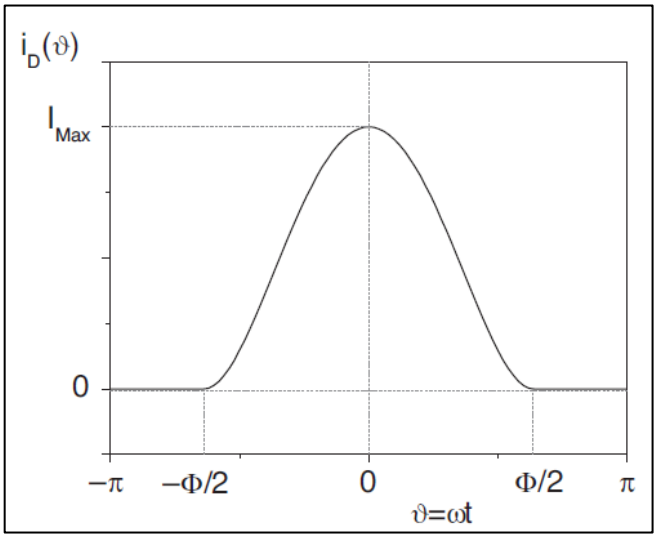


Fig. B.2: Quadratic sinusoidal waveform

$$I_1(\Phi) = \frac{16\,I_{max}}{\pi\left(\frac{\Phi}{4}\right)^4} \cdot \left\{\left[3 - \left(\frac{\Phi}{2}\right)^2\right]\sin\frac{\Phi}{2} - \frac{3\Phi}{2}\cos\left(\frac{\Phi}{2}\right)\right\}$$

$$I_2(\Phi) = \frac{I_{max}}{2}\,\frac{\sin\Phi\,(48 - 16\,\Phi^2) - 48\,\Phi\,\cos\Phi}{\pi\Phi^4}$$

$$I_3\,(\Phi) = \frac{16\,I_{max}}{\pi\left(3\,\frac{\Phi}{2}\right)^4}\cdot\left\{\left[1-\frac{1}{3}\left(3\,\frac{\Phi}{2}\right)\right]\sin\frac{3\Phi}{2}-\frac{3\Phi}{2}\cos\left(\frac{3\Phi}{2}\right)\right\}$$

3. Rectangular drain current (Fig. B.3)

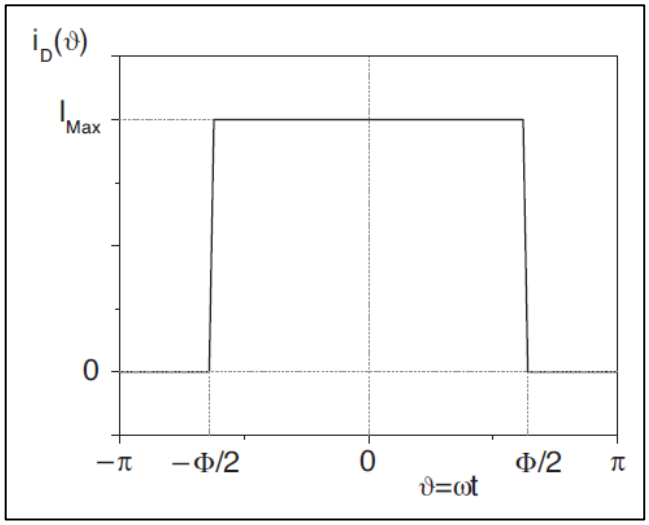


Fig. B.3: Rectangular waveform

$$I_{DC}\,(\Phi) = \frac{I_{max}}{2\,\pi}\cdot\Phi$$

$$I_1\,(\Phi) = \frac{2\,I_{max}}{\pi}\cdot\sin\left(\frac{\Phi}{2}\right)$$

$$I_2\,(\Phi) = \frac{I_{max}}{\pi}\cdot\sin\Phi$$

$$I_3\,(\Phi) = \frac{2\,I_{max}}{3\pi}\cdot\sin\left(3\,\frac{\Phi}{2}\right)$$

In order to perform harmonic tuning using second harmonic only, it is mandatory to have the fundamental and second harmonic components $I_1(\Phi)$ and $I_2(\Phi)$, respectively, being opposite in phase (i.e. opposite sign). In order to perform harmonic tuning via third harmonic only, it is necessary to have the fundamental and third harmonic components $I_1(\Phi)$ and $I_3(\Phi)$, being opposite in phase (i.e. opposite sign).

Appendix C: X Parameters

RF and microwave signal levels that are of the same order of magnitude as the operating range of the device are referred as the large-signal operating conditions. In practice, this corresponds to operating the amplifying device with at least 1-dB of compression. For system with such large signal operation, X-parameter characterises the nonlinear performance (harmonic generation, intermodulation performance, etc.) through complete measurements of the vector spectrum at the input/output ports. Unlike linear S-parameters (function of frequency and DC bias), nonlinear X-parameters depend upon the signal power (Fig. C.1) and must account for the harmonic content of the input and output signals since energy can be transferred to other frequencies in a nonlinear device.

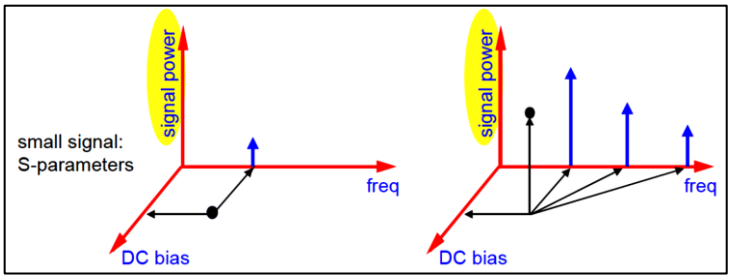


Fig. C.1: Small Signal S parameters and Large signal Parameter domain

The large signal parameters based research was tightly involved with the parallel development of corresponding software and measurement hardware. Due to this reason, X parameters [117], first reported in 2005, were patented by Agilent Technology. Similar parameters, named as S functions, were promoted by NMDG, a Belgium company. In fact both X-parameters and S-functions are extensions of the poly-harmonic distortion (PHD) modelling approach and relate the spectra found at the device terminals to a given set of stimuli and termination impedances.

The Poly-Harmonic Distortion (PHD) approach is based on frequency-domain measurements and is identified from the responses of a device under test (DUT) stimulated by a set of harmonically-related discrete tones. The fundamental tone is dominant and the harmonically- related tones are relatively small, so that the principle of harmonic superposition can be accurately applied. This principle asserts that the magnitude of the small test signals is such that the perturbation can be viewed as a linear process. Similar to S-parameters, the basic quantities are traveling voltage waves. The incident waves (**A**-waves) and the scattered waves (**B**-waves) are defined as follows

$$\mathbf{A} = \frac{\mathbf{V} + Z_c\mathbf{I}}{2}$$

$$\mathbf{B} = \frac{\mathbf{V} - Z_c\mathbf{I}}{2}$$

Z_c is the characteristic impedance. Here, **A** and **B** are full harmonic spectra (not small-signal phasors). These waves are defined based on a pure mathematical transformation of the signal port voltage and current and are not associated with a physical wave transmission structure. The concept is illustrated in Fig. C.2 in terms of fundamental waves A_{pm} and B_{pm}. The subscript *p* refers to port number, whereas *m* refers to the multiplier for the fundamental frequency or the harmonic index. A_{11} is the dominant large signal input component.

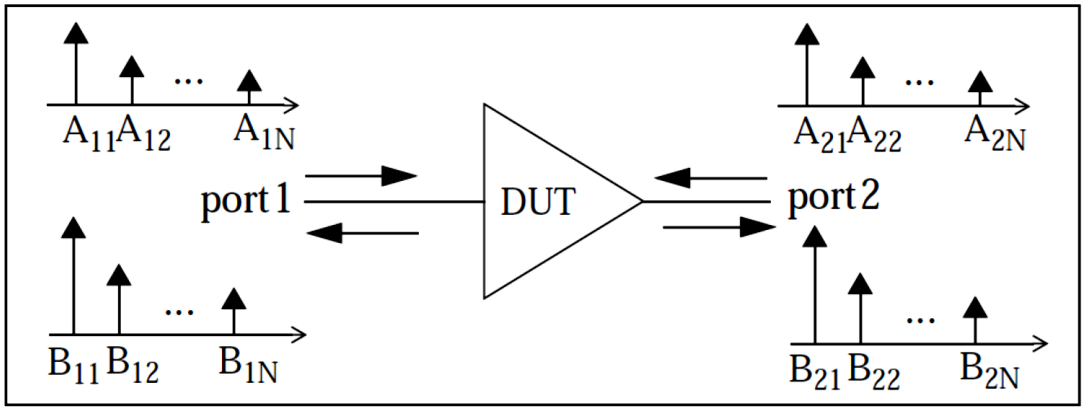


Fig. C.2: The concept of wave quantities

In order to relate **A** and **B** (nonlinear functional relationships between the wave quantities) some describing functions are needed similar to S parameters. These functions do the mapping of the input signal to the spectral components appearing at all the device ports, generated by device non-linearity.

In general, under large-signal, nonlinear operating conditions the superposition principle is not valid. However, the superposition principle can be applied for the relatively small harmonic components. This is called the harmonic superposition principle. This is nothing but linearization of nonlinear function around a stable single-valued and continuous operating point in mathematics by writing **A** and **B** as $\mathbf{A=A_0+a}$ and $\mathbf{B=B_0+b}$. Here $\mathbf{B_0}$ is the large-signal steady-state response to the large steady-state excitation A_0, and b is the response to a small excitation signal a superimposed on $\mathbf{A_0}$. After linearizing the functional relationship between **A** and **B** [117], we get X parameter equation as

$$B_{pm} = \sum_{qn} X^{(S)}_{pq,mn}(|A_{11}|)P^{+m-n}A_{qn} + \sum_{qn} X^{(T)}_{pq,mn}(|A_{11}|)P^{+m+n}\,\text{conj}\,(A_{qn})$$

X-parameters are an extension of S-parameters to large signal conditions. The $X^{(S)}_{pq,mn}$ relate the scattered wave having the harmonic index m at port p of the network (i.e, B_{pm}) with the incident waves of harmonic index n at port q of the network (i.e., A_{qn}). Similarly, the set of $X^{(T)}_{pq,mn}$ relate the scattered wave having the harmonic index m at port p of the network (i.e., B_{pm}) with the conjugate of incident waves of harmonic index n at port q of the network (i.e.,A^*_{qn}). The $X^{(S)}_{pq,mn}$ term is hot S_{22} measurements, including harmonic mismatch at input and output ports. It relates the mismatch at one frequency to performance at another. The $X^{(T)}_{pq,mn}$term gives the phase-dependence of mismatch at the output port at the fundamental, and also the phase dependence of harmonic mismatches at both ports. There is no analogue of this term in linear S-parameter theory. Its contribution vanishes in the small-signal limit.

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