A Novel scheme for DSP based Power Converter Control

By

ANIRBAN DE

Enrolment No.: ENGG04200804001

Variable Energy Cyclotron Centre, Kolkata, India

A thesis submitted to the

Board of Studies in Engineering Sciences

In partial fulfillment of requirements

for the Degree of

DOCTOR OF PHILOSOPHY

of

HOMI BHABHA NATIONAL INSTITUTE

September, 2016

Homi Bhabha National Institute

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DECLARATION

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List of Publications arising from the Thesis

Journal publications

1. Anirban De, "A Novel Design Methodology for Low Pass Filter Stage of a Voltage Source Inverter", Sadhana (Academy Proceedings in Engineering Sciences), Vol 41, No. 5, May 2016, pp 561-570.

2. Anirban De, S. Kumari, V.K. Khare, S.S. Pal, A. Sadhukhan, V.K. Meshram, S.K. Thakur, S. Saha, "Design Analysis and Implementation of a Dynamic Voltage Restorer", Journal of Low Power Electronics (JOLPE), Vol 9, No. 3, Oct 2013, pp. 340-349.

3. U. Bhunia, J. Pradhan, A. Roy, V. Khare, U. Panda, A. De, S. Bandopadhayay, T. Bhattacharyya, S. Thakur, M. Das, S. Saha, C. Mallik, R.K. Bhandari, "Design, fabrication and cryogenic testing of 0.6 MJ SMES coil", Cryogenics, Vol 52, Issue 12, Dec 2012, pp. 719-724.

Conference proceedings

1. Anirban De, U. Bhunia, S. Bandopadhayay, J. Pradhan, Subimal Saha, "Design, development and testing of a 0.6MJ/3.4kW Prototype Superconducting Magnetic Energy Storage System based Dynamic Voltage Restorer", 26th International Cryogenic Engineering Conference International Cryogenic Materials Conference (ICEC 26 - ICMC 2016), Manekshaw Centre, New Delhi, India, Mar 7-11, 2016.

2. Anirban De, Santwana Kumari, V.K. Khare, S.S. Pal, Anindya Sadhukhan, V.K. Meshram, S.K. Thakur, Subimal Saha, "Design, Develop-

ment and Testing of a DSP based Dynamic Voltage Restorer", Proceeding of the 3rd International Symposium on Electronic System Design (ISED2012), BESU, Shibpur, Howrah, Dec 19-22, 2012.

Other related oral presentations

1. "SMES based Dynamic Voltage Restorer: A Prototype", DAE-BRNS Workshop on Superconductivity and its Application in Electrical Systems (SAES-2015), VECC, Kolkata, Dec 17-18, 2015.

2. "Evolving Trends in Power Converters for Accelerators", Theme Meeting on Unveiling Future with Cyclotrons, VECC, Kolkata, Jun 28-29, 2012.

ANIRBAN DE

To

The Creator

and

Amrita, Arghya, Adrija

and

My Parents

ACKNOWLEDGEMENTS

At the very outset I would like to express my sincere gratitude to my PhD guide Dr. Debranjan Sarkar for his technical guidance and invaluable suggestions during the course of the thesis. Several inspirational hours of fruitful discussions with him had been instrumental to the research. His optimistic way of dealing with situations motivated me against several odds that are usual in a serious study but may prove a source of irritation and frustration if not dealt in time. Not only did he encourage me in times of stress but also taught me ways to find solutions to most problems.

My technical advisor, Shri Subimal Saha, the then Head, ATG, VECC showed deep interst and unconditionally supported all my efforts to pursue the studies. My thanks to my doctoral committee whose constructive suggestions had ultimately paved the way for what the research ultimately bore. I also acknowledge the project members of SMES Technolohy Development and the colleagues and staff of PE & MCDS, VECC and ATG Office for their wholeheared support during experiments for the resarch work.

I would also like to acknowledge Dr. Jan-e Alam, Dean Academic, Physical Sciences, VECC, HBNI and once again my guide, Dr. Sarkar, who introduced me to the world of latex that immensely helped me during the organization of documentations at each step of the research including writing this thesis. Dr. Kaushik Banerjee, Experminetal Physics Group, VECC, and Dr. Paramita Mukherjee, Dean Academic, Engineering Sciences, VECC, HBNI are also acknowledged for their advice on the organization of the document. My deepest respect to Dr. Mukherjee whose insistence and urgency on my PhD updates

regularly kept me focussed on the work.

I am deeply grateful to my family members for their love and patience during the reaserch years that provided all the moral enouragements I needed. My father had been my inspiration to take up research as a career option and I had never regretted the decision ever since. I am thankful for his insistence that made me enrol for the programme and allowed me to enrich my knowledge and understandings to a great extent. A major part of any research is based on extensive literature survey and patient investigations. Whatever little patience I possess and the reading habits that I have developed over the years, I owe it all to my mother who had infused in me the qualities right from my school days. I am also very much indebted to my wife who took care of all the major domestic responsibilities that allowed me precious hours at home for my research work. She had always been at my side in the hours of need. During my research years, my spirits have been revived time and again by my son and daughter whose unconditional love allowed me refreshing moments in between long hours of serious study.

Acknowledgements are also due to Dr. Kaustav Bhattacharya and Shri Supratim Majumder, BARC, Mumbai, Shri S. Balabharathi and Smt. A. Bhowmick, SIRF (Library), VECC for their support in retrieveing several important journals during the course of the research.

I would also wish to acknowledge the anonymous reviewers and examiners for their valuable comments and suggestions that helped fine tune the study.

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Contents

Synopsis

The aim of the present research is to devise a novel scheme for DSP based Power Electronics Converter coupled to a Superconducting Magnetic Energy Storage (SMES) system to mitigate voltage sags originating in the utility mains so as to keep the load voltage free of any interruptions.

The power quality is one of the most important issues in power distribution system. Many critical machines or industrial processes, especially those controlled by computers, are sensitive to any voltage sag or short interruptions in supply. These disturbances increase the down time of the machine or industrial process and hence the cost of production. The increasing demand for quality power has resulted in a growing interest in SMES based systems. SMES is a clean environment-friendly attractive solution for the power quality problems. SMES can mitigate short time voltage fluctuation and sag. The associated power control philosophy is based on correctly identifying the voltage sag in the AC utility lines (the instantaneous operating points of each phase) and efficiently compensating the sag by appropriately switching the power devices. Maintaining the quality of power is very important to a particle accelerator laboratory and steady electrical power is required during the beam delivery period for most of its sub-systems. Temporary voltage dips in line may cause

beam detuning or complete shut down of entire sub-systems, thus causing interruptions to experiments. For this a SMES based Dynamic Voltage Restorer (DVR) has been envisaged to mitigate the voltage sag in line.

The advantage of the huge energy that can be stored in a superconducting magnet coil may be exploited in an efficient Power Converter System (PCS) for providing reliable power to mitigate voltage sag which constitutes, among others, one of the most popular approaches to the Flexible AC Transmission System (FACTS) based devices. IEEE standard 1159-1995 defines voltage sag as a decrease to 10%-90% of the rated rms voltage at the power frequency for a duration of 0.5 cycles to 1 min which is again categorised in three different classes termed as instantaneous, momentary and temporary sag based on the time for which the sag persists. Accelerator laboratories deploys a large number of Low Conductivity Water (LCW) pumps and vacuum pumps which are predominantly motor driven. These are sensitive to voltage sags and following a sag in the line initiates break in the interlock chain leading to partial or complete shutdown of the accelerator system. Thus the PCS that is to be employed for voltage sag mitigation must compensate the voltage both in amplitude and in phase within a pre-defined time window.

Based on the schemes elaborated in literature, the fundamental FACTS controllers were introduced and their applicability discussed. A technical comparison is made based on which the selection of the proposed series scheme viz., Dynamic Voltage Restorer, was justified. Further, the switching scheme of the central power device i.e., the VSI was elaborated and arguments for its applicability as regards to efficient DC bus utilization and voltage sag identification were reviewed. Along with the efficient utilization of the DC bus,

it is shown how this particular scheme viz. Space Vector Pulse Width Modulation (SVPWM), may be used to constitute the heart of the controller to satisfy the control requirement of effectively locking the incoming phase and correcting the amplitude so as to maintain a constant voltage across the load. The inverter model based on the SVPWM switching scheme and the necessary mathematical transformations viz. transforming the rotating 3-ϕ to a stationery 2-ϕ system, for the control requirement were analysed. The rest of the chapters describe the development a control system to regulate the power electronics controller and a novel power filter system to attenuate the high frequency components while retaining the AC signal.

Control System Development

The heart of the controller is a Software Phase Locked Loop (SPLL) that is utilized to lock the incoming phase, thus nullifying any phase error. The phase information, thus corrected, is finally used in the amplitude controller to mitigate the voltage sag. Thus, in effect, both phase error and magnitude error are compensated for. Literatures report various SPLL designs, especially the design of the loop filter in several of which, there are references to the double frequency component that is inherent in the model but refers to the fact that the low pass nature of the SPLL itself attenuates the component. Also a few literatures further stress the need of an input filter that selectively allows bandlimited signal in the loop. The present work develops the SPLL with two additional blocks viz., an input bandpass filter to condition the voltage prior to its introduction in the loop and a band stop filter that is tuned to filter out the double frequency component and the loop filter is designed separately to

reduce the steady state error.

Based on the signal translation and the field parameters, the entire functionality of the system, starting from the field measurements to the generation of the inverter output, is mathematically summarized and signal flow is explained. The entire control system was initially designed in the analog domain that was transformed appropriately to the discrete domain. Based on the study of the scheme, the control system was formulated and a generalized mathematical modelling was done for the purpose. The mathematical realization of the control model, forms a generalized mapping of field parameters in the control block, which offers future designers to use it for general applications.

A digital controller is proposed for the control system. For this a Digital Signal Processor based controller was selected. Following this, an instrumentation interface was designed that feeds the Analog to Digital Converter (ADC) front end of the central controller with the field signals. The associated signal translation block was modelled and appropriately scaled for the DSP core. The isolation and component level design is also explained here. This design provides the basic scaling factors utilized during coefficient calculations.

Power Filter Development

Single phase and three phase Voltage Source Inverters (VSI) are typically the final interface between the power grid and the energy source in several applications. Pulse Width Modulation (PWM) based VSIs invariably constitute a Low-Pass Filter (LPF) stage for attenuating the higher frequencies arising due to the particular switching schemes.

While a first-order L filter is a simple solution for the LPF stage but the

second-order LC filter and more popularly, the third-order LCL filters are fast gaining momentum as the alternatives. With the increase in the order of the filter, additional control schemes are required for system stability that include methods reported in literatures such as current control strategy of a VSI with an LCL filter, a large signal stabilizer design based on the circle criterion theory to reject resonant oscillations, a nonlinear controller based on the composite nonlinear feedback control theory, a model predictive direct current control strategy incorporating virtual resistor based active damping, a two-degree-of-freedom PID active damping method to attenuate the resonance that is caused by the LCL filter based systems, a 7^{th} order LTCL filter which filters the harmonics efficiently but does not decrease the control difficulties. One of the basic requirements of higher order filter stems from the fact that a higher rating of the inductors (in case of L filter) and capacitors (in case of LC filters) that comprise the lower order filters are costly and voluminous. Work in this regard includes a design methodology to derive the lower value of the inductor based on inverter output peak current and the capacitor is determined according to the requirement of the resonant frequency of the LC filter. Another design perspective was based on the relation among the filter, inverter and the controller assuming the load to be a pure resistor for a worst case scenario. In yet another work, a design was proposed, based on active damping but this too, like others, assumes a 1:1 isolation transformer only. Further developments have included design based on multiple impact factors but here the unit is transformerless. A few literatures refer to the importance of the filter design and uses a step-up transformer but does not discuss the design of the filter components. The present work, in this regard, is to sup-

plement these by defining several performance indices to characterize a filter system and utilizes the transformer turns ratio i.e. the ratio of the number of turns in the secondary to that in the primary, advantageously in the design. In this, the transformer leakage inductance is considered to be negligible compared to the other inductances in the circuit. The design attempts to offer a practical choice of the filter components and proposes a novel LC filter topology for a $3-\phi$ VSI system that reduces the volume of the filter and assures a satisfactory attenuation thus eliminating the control overhead required in higher order filters.

In this regard, the common-mode noise, generated by the VSI switching, needs to be properly taken care of to prevent interference with sensitive loads. This may be attenuated by choke type inductor filters which are effective yet bulky. Reduction of capacitive coupling between the primary and secondary windings of the injection transformer may also be made, though this requires a trade-off with its leakage inductance. A bypass capacitor may also be used in between the primary and secondary grounds as an alternative route to the ground instead of the earth point. A Faraday shielding by employing an electrostatic shield close to the primary side may also be used to provide a return path so that the switching noise from the primary source is confined. This will actually reduce the overall common-mode noise.

Implementation and Test Results

An IGBT (450A/1200V) based 3-ϕ full-wave inverter with compatible gate triggering interface was fabricated for the experiment. A 32 bit fixed point DSP based controller with a 12.5MSPS 12 bit integrated ADC was pro-

grammed for the controller design. The testings were carried out in phases. In the first phase, to test the functionality of the controller, a load of $\sim$ 200 VA was selected, well within the short circuit capacity of the Injection Transformer (IT) and a breakerless scheme was tested. A programmable voltage source was used to introduce sag in the line which triggered the compensation. Oscilloscope recorded sag mitigation within half a cycle. In the next phase, the filter system was upgraded and a higher power load ($\sim$ 3.45 kVA) was used to test the inverter in the standalone mode. Subsequent to this the VSI and the IT was integrated to the SMES system with breaker to bypass the secondary during healthy mains. The programmable voltage source was used to simulate the sags and the final result indicated the almost instantaneous generation of the gating signals while steady state is achieved within 2 cycles. As it was integrated to the SMES system, the maximum amount of time for which the sag compensation could be maintained was limited by the coil and its charge, discharge system and so a maximum time of 6 seconds of sag mitigation was recorded. This encompassed the entire momentary voltage sag zone as defined in IEEE 1159-1995 as per the time limits and also overlaps part of the instantaneous and temporary sag zones. The results are published and are reported in conferences and workshops.

Conclusion

A summary of the completed work is presented and the scope of future work has been discussed in the concluding chapter. In the entire work, a generalized formulation has been given so as to allow designers to utilize it for future applications.

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Nomenclature

Abbreviations

ADC: Analog to Digital Converter

AGC: Automatic Generation Control

BESS: Battery Energy Storage System

CLTF: Closed Loop Transfer Function

CRGOS: Cold Rolled Grain Oriented Steel

CS: Cryogenic System

CSC: Current Source Converter

DSC: Digital Signal Controller

DSTATCOM: Distribution STATCOM

DVR: Dynamic Voltage Restorer

EMALS: Electromagnetic Aircraft Launch System

FACTS: Flexible AC Transmission System

GCF: Gain Crossover Frequency

GM: Gain Margin

HTS: High Temperature Superconductor

IPFC: Interline Power Flow Controller

IT: Injection Transformer

LCW: Low Conductivity Water

LF: Loop Filter

LPF: Low Pass Filter

LTS: Low Temperature Superconductor

LVE: Low Voltage Electronics

OLTF: Open Loop Transfer Function

PCF: Phase Crossover Frequency

PCS: Power Converter System

PD: Phase Detector

PF (or p.f.): Power Factor

PHES: Pumped Hydroelectric Energy Storage

PI: Proportional+Integrator

PLL: Phase Locked Loop

PM: Phase Margin

PT: Potential Transformer

PWM: Pulse Width Modulation

SCC: Superconducting Cyclotron

SMES: Superconducting Magnetic Energy Storage

SPLL: Software PLL

SPWM: Sine PWM

SSG: Static Synchronous Generator

SSSC: Static Synchronous Series Compensator

STATCOM: Static Synchronous Compensator

SVC: Static Var Compensator

SVPWM: Space Vector PWM

SVS: Static Var System

TCBR: Thyristor Controlled Braking Resistor

TCPAR: Thyristor Controlled Phase Angle Regulator

TCPST: Thyristor-Controlled Phase-Shifting Transformer

TCR: Thyristor Controlled Reactor

TCSC: Thyristor Controlled Series Capacitor

TCSR: Thyristor-Controlled Series Reactor

TF: Transfer Function

THD: Total Harmonic Distortion

TSC: Thyristor Switched Capacitor

TSR: Thyristor Switched Reactor

TSSC: Thyristor-Switched Series Capacitor

TSSR: Thyristor Switched Series Reactor

UPFC: Unified Power Flow Controller

UPQC: Unified Power Quality Controller

UPS: Uninterrupted Power Supply

VAR: Reactive Volt Ampere

VCO: Voltage Controlled Oscillator

VEC: Variable Energy Cyclotron

VECC: Variable Energy Cyclotron Centre

VSC: Voltage Source Converter

VSI: Voltage Source Inverter

ZOH: Zero Order Hold

Symbols/notations

B_c: critical magnetic field of the superconducting material

c: offset of DSC block

c_{equiv}: equivalent offset of the instrumentation block

$\cos\theta_r$: load pf $= \dfrac{P_r}{S_r}$

C_p: capacitance of filter capacitor placed in IT primary

c_{PTADC}: offset of PT-ADC block

C_s: capacitance of filter capacitor placed in IT secondary

E: magnetic energy stored in coil

e_{LI}: performance index for inductor based on stored energy

F(s): TF of loop filter

G(s): CLTF of PLL system

$G_{BP}(s)$: TF of bandpass filter

$G_{BP}(z)$: z transformed TF corresponding to $G_{BP}(s)$

$G_{BS}(s)$: TF of the bandstop filter

$G_{BS}(z)$: z transformed TF corresponding to $G_{BS}(s)$

$G_e(s)$: TF of the phase error w.r.t. the input phase

$G_f(s)$: TF of the loop filter part cascaded with bandstop filter

$G_{leadlag}(s)$: TF of lead-lag type loop filter $= k_{leadlag}\dfrac{(1+T_1 s)}{(1+T_2 s)}$

$G_{LP}(j\omega)$: filter TF w.r.t. inverter line to line voltages

$G_{PI}(s)$: TF of PI type loop filter $= (k_p + \dfrac{k_i}{s})$

$G_{PI}(z)$: z transformed TF corresponding to $G_{PI}(s)$

$G_{VCO}(z)$: z transformed TF corresponding to $G_{VCO}(s)$

$G_(z)$: z transformed TF corresponding to $G_(s)$

I_{Cp}: current through filter capacitor placed in IT primary = $\begin{bmatrix} I_{Cpa} & I_{Cpb} & I_{Cpc} \end{bmatrix}^T$

I_{Cs}: current through filter capacitor placed in IT secondary = $\begin{bmatrix} I_{Csa} & I_{Csb} & I_{Csc} \end{bmatrix}^T$

I_{dc}: dc currect flowing through the coil

$I_{inv,ll}$: line current at inverter output = $\begin{bmatrix} I_{ab} & I_{bc} & I_{ca} \end{bmatrix}^T$

I_L: inductor current = $\begin{bmatrix} I_{La} & I_{Lb} & I_{Lc} \end{bmatrix}^T$

I_l: load current = $\begin{bmatrix} I_{la} & I_{lb} & I_{lc} \end{bmatrix}^T$

i_{lp}: load phase current matrix = $\begin{bmatrix} i_{la} & i_{lb} & i_{lc} \end{bmatrix}^T$

$I_{l,ph}$: load current per phase

I_p: IT primary current = $\begin{bmatrix} I_{pa} & I_{pb} & I_{pc} \end{bmatrix}^T$

I_s: IT secondary current = $\begin{bmatrix} I_{sa} & I_{sb} & I_{sc} \end{bmatrix}^T$

I_{supply}: supply current

J_c: critical current density of the superconducting material

k_{bs}: gain of bandstop filter

k_{bp}: gain of bandpass filter

K_d: gain block representing part of the PD for linearized PLL model

k_i: integral constant of PI controller

k_{inj}: magnitude of series injection voltage perpendicular to current

K_m: gain of PD

K_o: VCO gain for linearlized PLL model

k_p: proportional constant of PI controller

k_{sag}: depth of voltage sag

k_t: correction term incorporating both the magnitude and phase compensation factors

L_p: inductance of filter inductor placed in IT primary

L_s: inductance of filter inductor placed in IT secondary

m: gain of DSC block

$m_{ADC} = \dfrac{2^n - 1}{v_{ADCFS}}$: ADC gain

m_{equiv}: equivalent gain of the instrumentation block

m_{PT}: PT turns ratio

m_{PTADC}: gain of PT-ADC block

n_{ADC}: ADC bits

$n_{Cl}(j\omega)$: filter capacitor voltage normalized to corresponding load voltage

$n_{Cpl}(j\omega)$: voltage across filter capacitor placed at IT primary in $L_pC_pC_s$ configuration, normalized to corresponding load voltage

$n_{Csl}(j\omega)$: voltage across filter capacitor placed at IT secondary in $L_pC_pC_s$ configuration, normalized to corresponding load voltage

$n_{Ll}(j\omega)$: current through filter inductor normalized to corresponding load current

Q_{bp}: quality factor of bandpass filter

Q_{bs}: quality factor of bandstop filter

L_{coil}: inductance of the coil

R_l: load resistance per phase

S: rated power of coil

(S_1, S_2, S_3): binary states (0, 1) of the switches in the three legs of the VSI

S_l: total load KVA

T_c: critical temperature of the superconducting material

(t_x, t_y, t_z): weights assigned to space vectors

v_{ADC}: the ADC output digital word corresponding to v_{PTADC}

v_{ADCFS}: Full scale analog voltage of ADC

V_{coil}: voltage generated across the coil

V_{Cp}: voltage across filter capacitor placed in IT primary = $\begin{bmatrix} V_{Cpa} & V_{Cpb} & V_{Cpc} \end{bmatrix}^T$

V_{Cs}: voltage across filter capacitor placed in IT secondary = $\begin{bmatrix} V_{Csa} & V_{Csb} & V_{Csc} \end{bmatrix}^T$

v_d: PD output

V_{dc}: DC bus voltage

v_{dq}: Park transformed $2-\phi$ equivalent of $3-\phi$ voltages = $\begin{bmatrix} V_d & V_q \end{bmatrix}^T$

v_{dqn}: Park transformed voltages normalized w.r.t. V_{ref}

v_i: injected sinusoid to a PLL

V_{inject}: injected voltage = $V_{pre-sag} - V_{sag}$

V_{invll} (or $V_{inv,ll}$): inverter line to line voltage matrix = $\begin{bmatrix} V_{ab} & V_{bc} & V_{ca} \end{bmatrix}^T$

$V_{invll\alpha\beta}$: stationery $2-\phi$ equivalent of V_{invll}

V_{invpp}: inverter phase to neutral voltage matrix = $\begin{bmatrix} V_{an} & V_{bn} & V_{cn} \end{bmatrix}^T$

V_L: inductor voltage = $\begin{bmatrix} V_{La} & V_{Lb} & V_{Lc} \end{bmatrix}^T$

V_l: load phase voltage matrix = $\begin{bmatrix} V_{la} & V_{lb} & V_{lc} \end{bmatrix}^T$

v_m: any element of $\begin{bmatrix} V_{mp} \end{bmatrix}$

V_{mp}: mains phase voltage matrix = $\begin{bmatrix} V_{ma} & V_{mb} & V_{mc} \end{bmatrix}^T$

v_o: VCO output

V_p: IT primary voltage = $\begin{bmatrix} V_{pa} & V_{pb} & V_{pc} \end{bmatrix}^T$

v_p: the corresponding digital word as fed to the control block

V_{pn}: matrix of mains phase voltage translated to the DSC core = $\begin{bmatrix} V_{pa} & V_{pb} & V_{pc} \end{bmatrix}^T$

v_{pref}: rated mains voltages synchronized to mains phase = $\begin{bmatrix} V_{aref} & V_{bref} & V_{cref} \end{bmatrix}^T$

$= V_{ref} \begin{bmatrix} cos(\omega t + \theta_m) & cos(\omega t + \frac{2\pi}{3} + \theta_m) & cos(\omega t - \frac{2\pi}{3} + \theta_m) \end{bmatrix}^T$

$V_{pre-sag}$: voltage prior to sag

v_{PT}: the PT output corresponding to v_m

v_{PTADC}: the PTADC block output corresponding to v_{PT}

V_{ref}: peak reference phase voltage

V_s: IT secondary voltage $= \begin{bmatrix} V_{sa} & V_{sb} & V_{sc} \end{bmatrix}^T$

$V_s' \angle \theta$: space vector

V_{sag}: sag voltage

$\Theta_d(s)$: Laplace transformed phase error

θ_d: phase error

$\Theta_i(s)$: Laplace transformed phase of input signal to PD

θ_i: phase of input signal to PD

θ_{inject}: phase angle between V_{inject} and V_{sag}

θ_m: mains phase angle

θ_o: phase of output cosine signal from VCO

θ_{sag}: phase angle between $V_{pre-sag}$ and V_{sag}

ω_{bp}: centre frequency of bandpass filter

ω_{bs}: angular centre frequency of the bandstop filter

ω_i: angular frequency of input signal to PD

ω_n: natural frequency of oscillation for a second-order filter

ω_o: angular frequency of output signal from VCO

ζ: damping coefficient for a second-order filter

Operators

$$S_{+1} = \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix}, \text{ where } a = e^{j\frac{2\pi}{3}}$$

$$S_{-1} = \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix}, \text{ where } a = e^{j\frac{2\pi}{3}}$$

$$T_1 = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

$$T_2 = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

$$T_{3s2r}(\theta)\text{: Park transformation} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta+\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta+\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) \end{bmatrix}$$

$$T_{3s2s}\text{: peak invariant Clarke transformation} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$$

$$T_{p2l}\text{: phase parameter to line parameter transformation matrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Chapter 1

Introduction

1.1 Superconducting Magnetic Energy Storage system

The power quality is one of the most important issues in power distribution system[1]. Special electrical equipments have much higher requirements about continuity and reliability of power. Many critical machines or industrial processes, especially those that employ embedded processors and controllers have much stringent requirements about continuity and reliability of power system and are sensitive to voltage sags or short interruptions in supply. These disturbances in supply can increase the down time of the machines and hence the cost of production.

To counter these, a number of energy storage technologies have evolved. Ali et al[2] states that the most viable of them are Battery Energy Storage System (BESS), Pumped Hydroelectric Energy Storage (PHES) system and the Superconducting Magnetic Energy Storage (SMES) system. However, both

BESS and PHES have some serious drawbacks. Limited life cycle, voltage / current limitations, potential environmental hazards are the weak points of BESS[2, 3] and large unit sizes, topographic and environmental limitations are the weak points of PHES[2]. SMES scores over the other energy storage technologies in respect of efficiency ($> 95\%$), lifetime, response time and high power density [4, 5] which is more as compared to capacitive storage and fly-wheel energy storage systems. Owing to its static nature, the maintenance requirement is low [6] that ensures a long life (30 to 40 years) and a high reliability[7, 8]. It is also environmentally clean. Thus it may be summarised as a clean, environment-friendly, attractive solution for the power quality problems having the ability to mitigate short time voltage fluctuations and sags. Several commercial and test bed projects have been launched to provide power quality at manufacturing plants requiring ultra-clean power, such as microchip fabrication facilities [9].

Another way of describing SMES is by stating that SMES is a grid-enabling device that stores and discharges large quantities of power almost instantaneously. The system is capable of releasing high levels of power within a fraction of a cycle to replace a sudden loss or dip in line power. Strategic injection of brief bursts of power can play a crucial role in maintaining grid reliability especially with increasingly congested power lines of today and the high penetration of renewable energy sources, such as wind and solar.

1.1.1 Theory of energy storage

An SMES unit stores energy in the form of magnetic field generated by the dc current flowing through the superconducting coil (SC). The stored

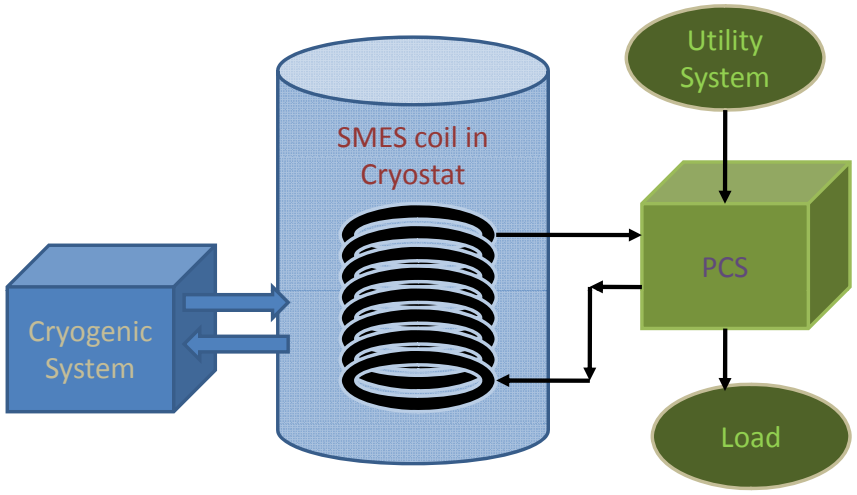

Figure 1.1: The scheme of an SMES system

energy (E) and the rated power (S) can be expressed as follows

$$E = \frac{1}{2} L_{coil} I_{dc}^2 \qquad \& \qquad S = \frac{dE}{dt} = L_{coil} I_{dc} \frac{dI_{dc}}{dt} = V_{coil} I_{dc} \tag{1.1}$$

To maximize E, the current flowing through the coil is to be made as high as possible. Now, a superconductor, if kept within the critical parameters of the material of the superconducting coil viz. critical current density (J_c), critical magnetic field (B_c), critical temperature (T_c), has very very low (theoretically zero) resistance to dc current. In this way, the current can be increased to very high values, thus storing a significant amount of energy in the superconducting coil, without losing any energy by dissipation. This is the principle behind the SMES systems.

1.1.2 General scheme

The scheme of the SMES system may be understood from Fig. 1.1. The SMES coil is energized to its rated capacity during healthy mains con-

dition through a Power Conditioning System (PCS). As and when there is a requirement of the stored energy, be it due to a voltage sag in mains affecting the critical load or as a backup power source[2], the same PCS is dynamically reconfigured to use the stored energy to feed the critical loads.

1.1.3 SMES sub-systems

An efficient SMES system essentially consists of four sub-systems [6, 10] as listed in the following with a brief outline of the scope of each.

i. Superconducting (SC) Magnet and the related support systems: The material for SC cable could be selected from Low Temperature Superconductor (LTS) and the High Temperature Superconductor (HTS) that requires cooling to 4.2K (using liquid helium) and 77K (cooled by liquid nitrogen) respectively. Inspite of HTS material being cheap, the price of the HTS cable is significantly higher compared to LTS one [11, 12] as it is difficult to give shape to HTS material due to its high brittleness. Also an SMES coil, being subjected to frequent charge discharge cycles, will be having greater AC losses which is less for LTS cables [6]. Once the wire is selected, the coil configuration is another important issue. The three factors that generally guide the mechanical design of the same are strain tolerance, thermal contraction on cooling and Lorentz force during charging of the coil. Though several types of coils like linear multipole, spherical coils are proposed but generally the design is a choice between solenoid and toroid. For small SMES, the coil is generally solenoidal but for larger ones, toroidal coils are opted. Basically this is due to the fact that though it requires more material than the solenoid, which is also simpler in struc-

ture, but toroid is much better in containing the fringe field effectively [6, 9, 13].

ii. Cryogenic System (CS): The CS comprises the cryostat, vacuum pumps and other refrigeration systems to keep the coil in the superconducting stage. Further, the CS is intrinsically related to the performance and the overall health of the coil. The losses in the cryostat and the other eddy current related AC losses increase the heat load which must be met effectively by this sub-system so as to maintain the operating temperature [6]. The cooling also improves stability of the magnet and serves as one of the highest priority interlocks to maintain the condition of the coil. The design of the magnet and the CS is supplemented by a protection system so as to prevent a quench and limit its effect [14].

iii. Power Conditioning System (PCS): This handles the power transfer between the superconducting coil and the ac system. There are various types of PCS design, which may be categorised as Thyristor based PCS, Voltage Source Converter (VSC) based PCS and Current Source Converter (CSC) based PCS. The Thyristor based PCS can control only the active power and has little or no control on the reactive power while both the VSC and CSC have independent control over both the active and reactive power components. Also, both the VSC and the CSC based SMES have lower Total Harmonic Distortion (THD) than the thyristor based PCS. Again, the VSC based system has a complex control system with respect to the other two. [2].

iv. Control Unit that essentially regulates the proper functionality for which

the system is designed. The SMES control generally requires measurement of AC signals, extracting both amplitude and phase information from the same and providing pre-driver signals to the bridge circuits. Though analog control can effectively do all the above but due to complexity of implementation, digital approach is preferred. To implement phase comparison and correction in the control algorithm, various mathematical transforms are needed that generate the required reference signal and allow phase lock. Though in principle, an analog control and instrumentation may achieve the purpose but the mathematical manipulation, namely the transform and the scaling of the signals, is easier to implement in the digital domain. Not only is the control hardware minimized but the complexity of the processing circuits is replaced by software codes that makes the system faster in the development stage and avoids the effects of component bias and tolerance. Thus the scheme allows a provision of DSP based control system implementation.

1.1.4 Applications

The main applications of SMES may be categorised as follows:

1. Energy Storage: An SMES unit could provide the potential for energy storage (around 5000MWh) with a high efficiency (95%) and a rapid response time for dynamic change of energy flow (msec). Thus it serves as an efficient spinning reserve which may be used both for frequency control and load leveling that find use in industrial manufacturing plants, nuclear power plants, high speed railway system substations. Also SMES finds use in energy management as a storage and transfer point for bulk

quantity of energy that potentially lowers the electricity cost [2, 6, 15–18].

2. Pulsed Power Supply: Owing to its high energy density, SMES is an interesting choice in military applications like Electromagnetic (EM) Railgun, Electromagnetic Aircraft Launch System (EMALS), that needs a pulse power source with a stored energy range of tens of kJ to several GJ and instantaneous power ranging in 20 GW [2, 6, 14, 19, 20]. Also SMES based long-pulse klystron modulator has been deployed that avoids disturbance in the electric power network which a power surge loading in the grid might have caused [21].

3. Flexible AC Transmission System (FACTS): The SMES systems are easily configured to provide energy storage to FACTS devices which, otherwise, operates with power from the grid. Thus the SMES improves the performance of FACTS by supporting the real power requirement in addition to the reactive power control of the devices. Therefore the integrated device is able to supply and absorb both active and reactive power. The SMES unit, as a whole, can dampen dynamic oscillations in power system, improve stability and power quality of a transmission grid, regulate transmission voltage and can also damp $3-\phi$ fault induced electromechanical transient oscillations if connected near the generating bus[2, 6, 15].

4. Uninterrupted Power Supply (UPS), Power Quality and Reliability: The SMES also proves to be an alternative to backup power supply which means it can serve as an UPS for large industrial equipments / systems,

in case of loss of utility mains power. These can smooth out disturbances of power systems within a cycle ensuring quality power and countering the perturbations due to transmission line flashovers, voltage dips due to lightning, line trips that adversely affect sensitive loads. This is more prominent in industrial scenario where there is no direct access to improve system or equipment. Thus the only option is to improve on the system-load interface. Also on clearance of a fault, the protective relays prevent fast reclosure of circuit breakers if power angle difference across it is large. By briefly compensating for a small amount of power, the SMES can reduce the power angle across the breaker allowing a quicker restoration of power following a major outage [2, 6, 15, 22].

5. Other: The other areas of SMES utilization, not explicitly mentioned above include automatic generation control, reactive Volt Ampere (VAR) control and power factor (PF) correction, black start capability, dynamic voltage stability, tie line control, underfrequenccy load shedding reduction, subsynchronous resonance damping, wind generation stabilization, minimization of power and voltage fluctuations of wind generator [2].

1.2 Theme of the present work

1.2.1 Background

Particle accelerator laboratories require steady electrical power during its beam delivery period for many of its subsystems. Temporary voltage dips in line may cause beam detuning or complete shut down of an entire sub-system, thus causing a lot of interruptions to experiments. Home to the K-130 Variable

Energy Cyclotron (VEC) and K-500 Superconducting Cyclotron (SCC), Variable Energy Cyclotron Centre (VECC), Kolkata had undertaken to develop an SMES system in-house to offer a general solution to particle accelerator laboratories, as well as to R&D laboratories in the country and critical industries, process plants where voltage sag amounts to a great financial loss[7, 23].

1.2.2 Focus

Though SMES can be utilized for short-term voltage mitigation as well as a back-up power source, here the focus is to develop a system to counter any voltage sag in the utility lines so as to deliver clean power to the load free from any disturbances. In this regard, the IEEE standard 1159-1995 may be referred to that standardizes voltage sag as a decrease of 10% to 90% of the rated rms voltage at the power frequency for the duration of 0.5 cycles to 1 min [1, 24], illustrated in Table 1.1. Thus the control philosophy is based

Magnitude→	**0 - 10%**	**10%-90%**	**>110%**
Duration			
0 - 0.5 cycles	Transients and oscillations	Transients and oscillations	Transients and oscillations
0.5 cycles - 30 cycles	Momentary interruption	Instantaneous sag	Instantaneous swell
30 cycles - 3 sec	Momentary interruption	Momentary sag	Momentary swell (upto 140%)
3 sec - 1 min	Temporary interruption	Temporary sag	Temporary swell (upto 120%)
>1 min	Sustained interruption	Undervoltage	Overvoltage

Table 1.1: Illustrating some of the IEEE 1159-1995 standard nomenclatures

on correctly identifying the region of operation of the AC utility lines (the instantaneous operating points of each phase) so that a sag in the same can be efficiently compensated by appropriate switching of the PCS.

1.2.3 Motivation

The PCS that is required to be developed for the system entails several interesting aspects from the electrical and electronics point of view. In an accelerator laboratory, where the SMES is targeted to be used, the most problematic area identified during voltage sag for a running system is the stoppage of the Low Conductivity Water (LCW) pumps and the vacuum system pumps. The phase matching at the load side is thus, one of the utmost important requirement. Being predominantly a motor driven system, it is very sensitive to the voltage sag and is primarily responsible in initiating the break in the interlock chain leading to complete or partial shutdown of the related subsystems which results in stoppage of the machine. So correctly identifying the voltage phase and the amount of sag allows the control system to trigger the PCS to operate in the required mode. Thus it requires fast sampling of the input for generating the required triggering to the final converter. So the entire work can be subdivided under two major heads:

1. Control system: Deals with the instrumentation and digital controller that samples the utility mains and processes the same for interpreting the phase and sag magnitude and finally trigerring the power electronic switches according to requirement.

2. Power system: Deals with the power electronic based converter system

including transformers, harmonic filters, etc.

These will be discussed in the following chapters but we may briefly discuss here the rationale of the choice of the type of the control system. Though in principle, both analog and digital control system, may be used in the situation but the digital system is selected for the following distinct advantages over its analog counterpart.

1. The digital controllers are capable of performing computations with constant accuracy [25].

2. Algorithms in digital controllers replace the heart of the analog controller thus making it immune to drift, ageing effect and noise [26, 27].

3. Digital controllers are flexible, modifiable and provide improved sensitivity to parameter variations. Also any updation in the system does not generally require hardware modifications [26–28].

4. The control system developed is easier to test and commission [29].

5. The debugging and advanced autodiagnosis facilities are available[29].

6. There is adequate bandwidth for FACTS controller applications though it is somewhat limited in extremely fast complex control loops[29].

7. Storage of digital signals are easier[25].

8. The digital controllers are less expensive and more reliable than their analog counterparts[30].

However, as the field signals are inherently of analog type, the use of a digital control system requires an elaborate instrumentation interface so as to isolate and efficiently convert the analog signals to digital and vice versa. Thus the low voltage instrumentation also becomes an integral part of the control. These have been discussed in detail in the subsequent chapters.

Chapter 2

Study of FACTS devices

A very brief outline of the FACTS based devices is presented so as to understand its requirement and the rationale of choosing the SMES based Dynamic Voltage Restorer (DVR) system for the present study.

2.1 Introduction to FACTS devices

The FACTS technology may be summarised as a collection of controllers, which can be applied individually or in coordination with others to control one or more of the interrelated system parameters, such as series impedance, shunt impedance, current, voltage, and damping of oscillations [31]. The conventional control mechanisms like Automatic Generation Control (AGC), Excitation Control, Transformer Tap-Changer Control, Phase-Shifting Transformers, were basically generating station controllers to maintain the power line frequency and the rated voltage. The FACTS controllers secure the required flexibility in the transmission system to offer fast controllers for ensuring low losses by making the best utilization of the transmission capacity

[29]. FACTS controllers can be broadly categorized [32] as:

1. Shunt Controller
2. Series Controller
3. Combined Series-Shunt Controller
4. Combined Series-Series Controller

2.2 Shunt controller

The shunt controllers inject current to the system at the point of contact where they are connected [32] e.g. Static Compensator (STATCOM), Static Synchronous Generator (SSG) (Fig. 2.1), Static Var Compensator (SVC) (Fig. 2.2), Static Var Generator or Absorber (SVG), Static Var System (SVS), Thyristor Controlled Braking Resistor (TCBR) (Fig. 2.3). These can be used to control voltage around the point of connection by injecting active and reactive current into the system. Normally it handles only reactive power if the injected current is in phase quadrature with the line voltage but will supply or consume real power as well if phase relationship is anything else than that.

2.3 Series controller

A series controller may be either a variable impedance or a power electronics based variable source of mains frequency [31] or other frequency according to the need that protects critical loads from the effects of faults at the point of common coupling. If the line voltage is in phase quadrature

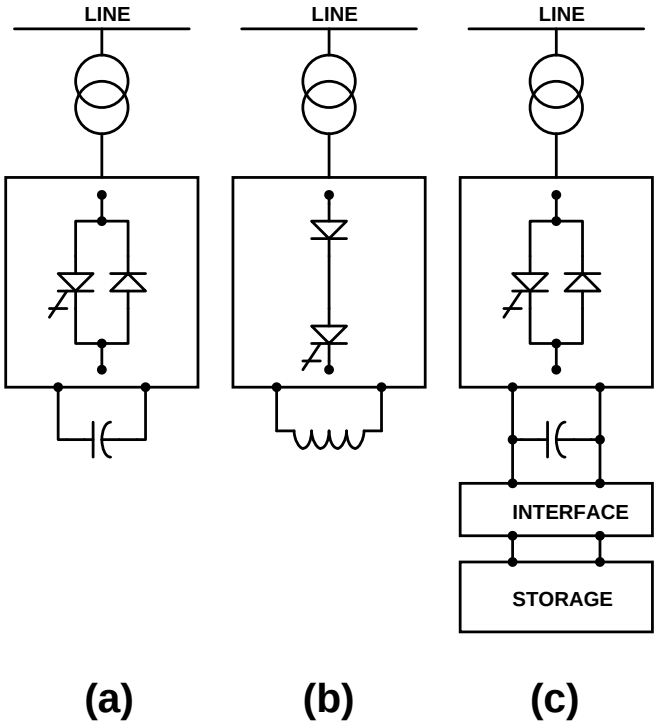

Figure 2.1: (a), (b) STATCOM and (c) SSG

with the line current, the series controller absorbs or produces reactive power. While if it is not, the controller must involve real power as well [31, 32]. Static Synchronous Series Compensator (SSSC) (Fig. 2.4), Thyristor-Switched Series Capacitor/Reactor (TSSC/TSSR), Thyristor-Controlled Series Reactor/Capacitor (TCSR/TCSC) (Fig. 2.5, Fig. 2.6), Dynamic Voltage Restorer (DVR) (Fig. 2.7) are a few examples of the series controllers. The other applications of series controllers are controlling current and power flow in system and to damp system oscillations.

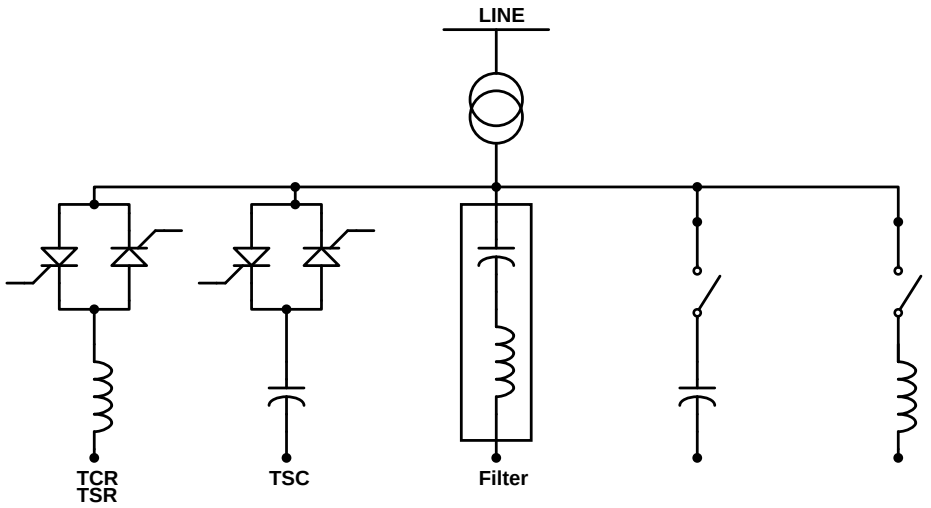

Figure 2.2: SVC

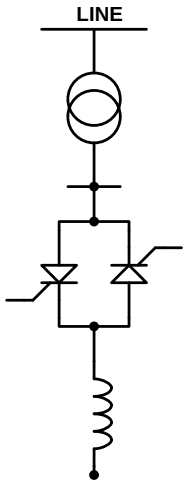

Figure 2.3: TCBR

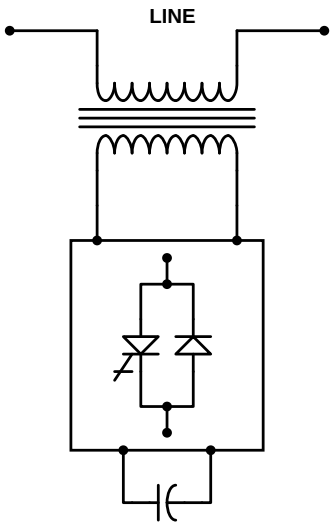

Figure 2.4: SSSC

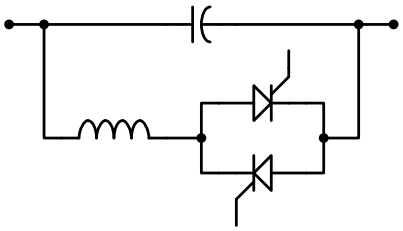

Figure 2.5: TCSC and TSSC configurations

2.4 Combined series-shunt controller

A combined series-shunt controller may have two configurations, one being two separate series and shunt controllers that operate in a coordinated manner and the other one being an interconnected series and shunt component. In each configuration, the shunt component injects a current into the system while the series component injects a series voltage. When these two elements

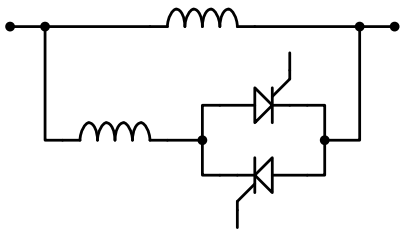

Figure 2.6: TCSR and TSSR configurations

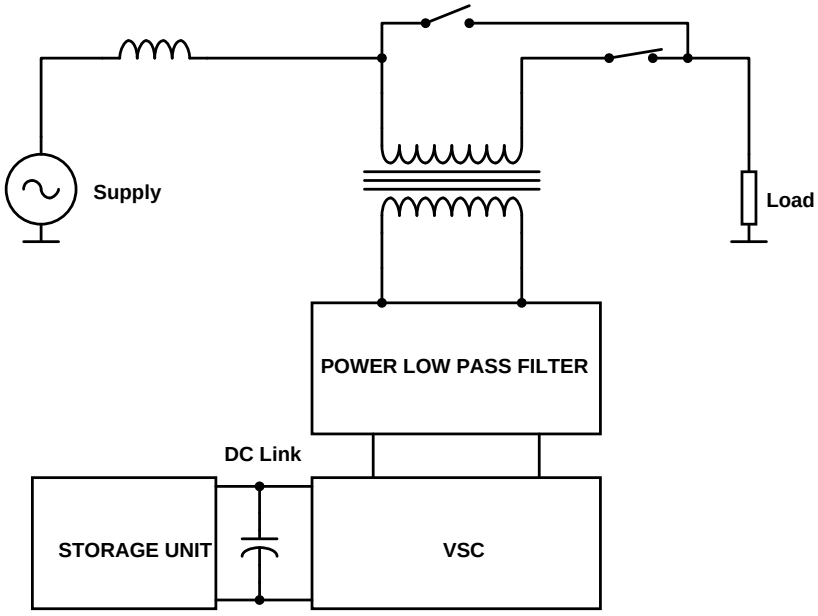

Figure 2.7: DVR

are unified, a real power can be exchanged between them via the power link. Examples of such controllers are Unified Power Flow Controller (UPFC) (Fig. 2.8) and Thyristor-Controlled Phase-Shifting Transformer (TCPST) / Thyristor Controlled Phase Angle Regulator (TCPAR) (Fig. 2.9)[33, 34]. These make use of the advantages of both series and shunt controllers and, hence, facilitate effective and independent power/current flow and line voltage control

[32].

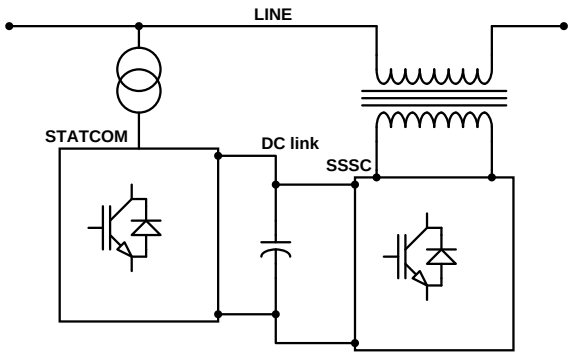

Figure 2.8: UPFC

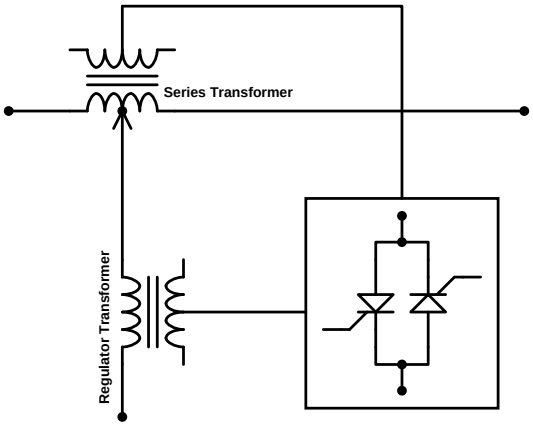

Figure 2.9: TCPST or TCPAR

2.5 Combined series-series controller

This could be a combination of separate series controllers controlled in a coordinated manner in a multiline transmission system or a unified controller

in which series controllers provide independent series reactive compensation for each line and, at the same time, facilitates real power transfer through the power link. An example of this type of controller is the Interline Power Flow Controller (IPFC) (Fig. 2.10)[35], which helps in balancing both the real and reactive power flows on the lines [32].

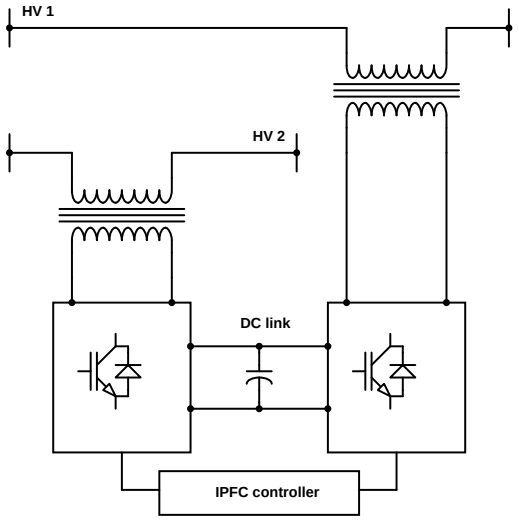

Figure 2.10: IPFC

2.6 Comparison of the various FACTS controllers and selection of the FACTS device for the present application

The comparison of FACTS controllers may be done based on several aspects. One such comparison that summarises the specific controllers used in transmission and distribution systems is available in [36]. Table 2.1 lists the

features pertinent to the present study.

FACTS in Transmission	**FACTS in Distribution**	**Preferred task in Tranmission**	**Preferred task in Distribution**
STATCOM	DSTATCOM (Distribution STATCOM)	voltage control, oscillation damping, VAR regulation	flicker compensation, VAR compensation, harmonic filter
SSSC	DVR	power flow, transient stability, oscillation damping	sag (swell) compensations
UPFC	UPQC (Unified Power Quality Controller)	SSSC, STATCOM features	under (over) voltage compensations, DVR, DSTATCOM features

Table 2.1: Comparison of FACTS devices used in transmission and distribution systems

Also for identical active power demand by the load terminal, for a short transmission line, the series compensator has a lesser VAR requirement than a shunt controller[31]. Series compensators are generally suitable choices for transient stability in transmission lines and sag compensation in distribution lines [36, 37].

The proposed application aims at voltage sag mitigation for accelerator laboratories with possible application to industrial loads as well. This clearly comes under the category of distribution system. Also the device is meant to utilize SMES system. So an energy storage supported series compensator or

more specifically an SMES based DVR is selected for the purpose.

2.7 DVR with its control objective

As has already been described in the previous section, a series compensator scheme viz., DVR is selected for the purpose. A DVR is an SSSC designed to keep the load voltage constant irrespective of transients or voltage sags that represent a dynamic change of real power to the load[38–40]. It injects voltage in series compensating for the difference between faulty utility voltage and the nominal ideal voltage. The active and reactive power required for generating the voltages are supplied by the VSC, fed from a DC link (see Fig. 2.7). This is due to the established fact that a VSC with its internal control can be considered as an ideal electromagnetic generator that can produce a set of AC voltages at the desired fundamental frequency with controllable amplitude and phase angle thus generating or absorbing reactive power and exchange active power with the AC system when the DC terminals are connected to a suitable DC energy storage [31]. The DVR normally protects critical loads from the effects of faults at the point of common coupling. During a voltage dip, it is able to inject the required voltage to reestablish the load supply voltages [41]. For line currents exceeding the inverter rating, a bypass scheme can be incorporated to protect the power electronic converter. Owing to the advantages and success of VSC based SMES system [2, 37], this has been utilized but with one basic difference i.e. the focus is on the voltage sag mitigation by feedforward control assuming the DC bus system to remain fixed during the SMES discharge. This had practically been established by decoupling the control systems of the DC-DC chopper and the Voltage Source

Inverter (VSI) with a handshaking between them. Thus concentrating on the VSI development, the principal elements and functionalities of its basic blocks are as listed below.

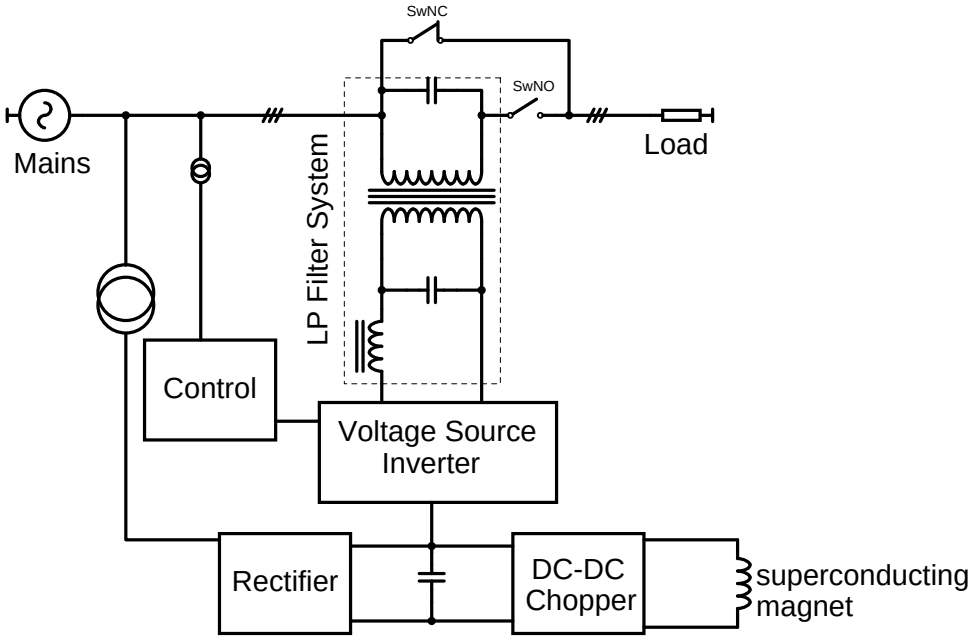

Figure 2.11: The DVR power and control block schematics

2.7.1 The power system

The system, as shown in Fig. 2.11, consists of a VSI, a Low Pass Filter (LPF) system and the Injection Transformer (IT) all of which are $3-\phi$ systems. The requirement of the DVR for mitigating sag according to the IEEE standard requires variable voltage injection which is achieved by Pulse Width Modulation (PWM) scheme [42]. The LPF is required to suppress the high frequency PWM switching to keep the load voltage smooth and the IT is utilized to step up the filtered AC according to the load requirement.

2.7.2 The control system

The control strategy is to simultaneously mitigate voltage sag at the same phase where it occurred. The most popular methods are briefly discussed in the following

i. **Pre-sag compensation**: In this method, the voltage injected by the DVR is the difference between the voltage just prior to the sag and the sagged voltage at the correct angle (Fig. 2.12). This is best suited for phase sensitive loads as well as for the voltage sensitive ones [41, 42].

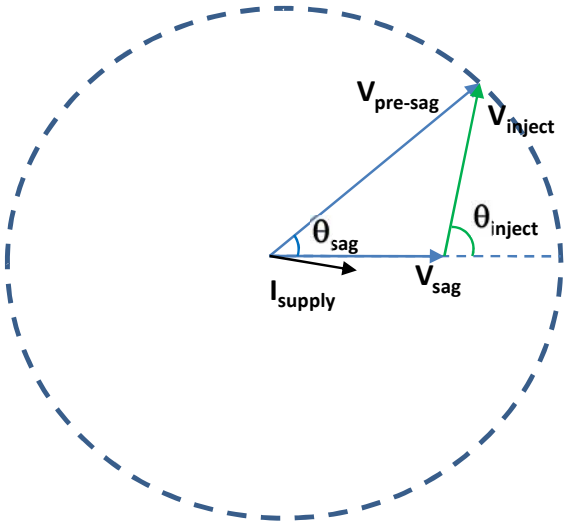

Figure 2.12: Pre-sag compensation

ii. **In-phase compensation**: In this case the DVR injects the voltage difference between the voltage just prior to the sag and the sagged voltage in-phase with the supply and thus deviating from the pre-sag load (Fig.

2.13). This, though compensates for the voltage magnitude, but cannot escape the inherent phase jump associated with it [41, 42].

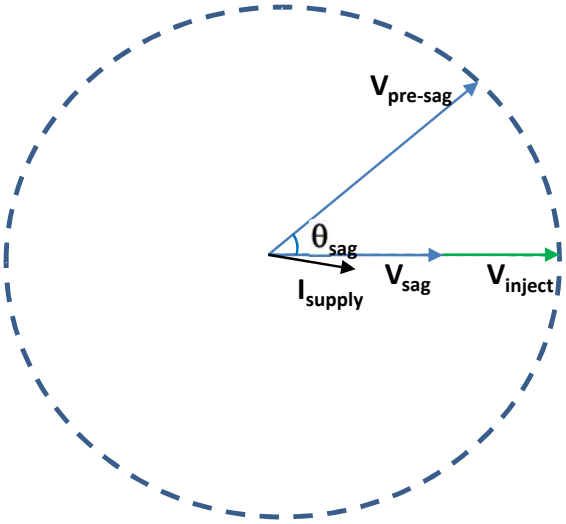

Figure 2.13: In-phase compensation

iii. **Energy-optimized compensation**: In this strategy, the DVR injects the maximum reactive power by drawing as much active power from the grid as possible. The principle of the method is to make the active injection power zero[43]. Thus the voltages are injected normal to the supply current (Fig. 2.14). This restores the voltage magnitude with a phase jump and is only applicable with small voltage sags [41].

From the previous discussions it is evident that the strategy that generalizes the control for both voltage and phase compensations is the pre-sag compensation technique which meets the objective of the proposed system.

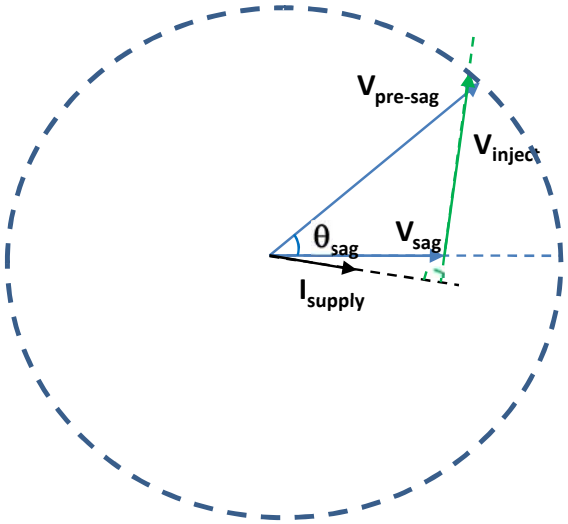

Figure 2.14: Energy-optimzed compensation

2.8 Sag detection and power generation

The power and control system thus finalized, the aim of the exercise is to obtain a generalized model of the integrated system and realize the control system by a digital controller. The two principle functions of the VSI based DVR with pre-sag compensation are

1. Detection of the sag magnitude and the phase in which it occurs.

2. Compensating for the balance amount of the amplitude at the correct phase in the load by suitable power electronic system.

An elegant way for simultaneous phase and sag magnitude detection for each phase voltage is to use Clarke Transformation [44] or Park Transformation [45] of the $3-\phi$ signals. For details about these transformations, Appendices A and B may be referred. This transforms a stationery $3-\phi$ signal to a rotating $2-\phi$ signal whose elements on normalization provides the necessary

information to lock the phase as well as compute the sag. The second function of the VSI can be achieved by utilizing a suitable Pulse Width Modulation (PWM) scheme for the $3-\phi$ inverter system to inject the necessary difference voltage. Among the two most popular switching scheme[46–48], viz., the Sine PWM (SPWM) and the Space Vector PWM (SVPWM) (Appendix C), the latter is chosen because of the following advantages [49–51].

1. Achieving wider modulation range associated with PWM third harmonic injection automaticaly without the need for distorted modulation.

2. SVPWM has lower base band harmonics than other sine based modulation methods.

3. SVPWM is fast and convenient to compute.

4. More efficient DC bus utilization than conventional SPWM.

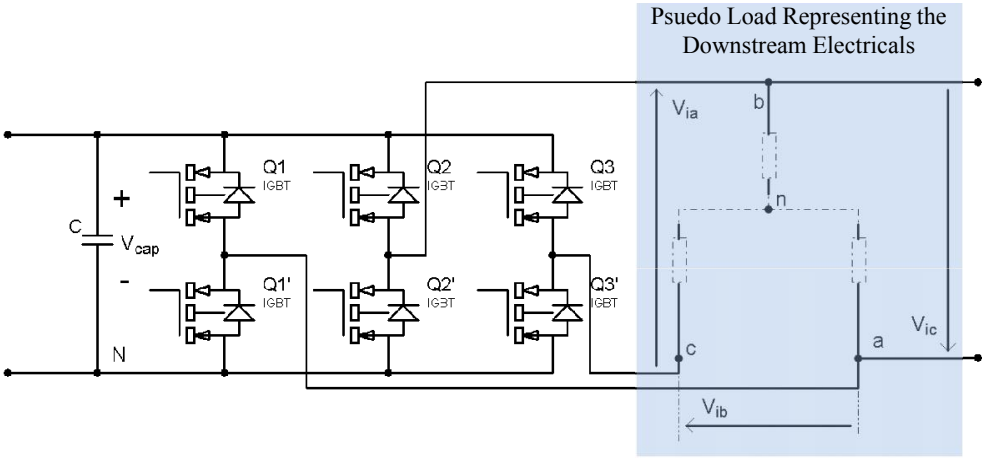

Figure 2.15: The IGBT switch based VSI feeding the load

The VSI design is based on Fig. 2.15, the details of which will be discussed in the following chapters. The load is represented in the lumped form as a star connected system which essentially consists of the downstream electricals viz. the low pass filter, the IT, the mains and the final load.

2.9 Novel strategies in control and power modules

The discussions, so far, had been limited to the description of the general scheme and the rationale behind selection of the digital controllers. The two salient features of the thesis will now be introduced. The VSI system is the final downstream element of the SMES based DVR. To achieve the basic objective of sag detection and mitigation two major developments are proposed for the control and the power filter blocks.

2.9.1 Scheme of the control system

The heart of the controller is a Software Phase Locked Loop (SPLL)[52, 53] that locks the mains phase and utilizes the information to mitigate the voltage sag. Thus, in effect, both phase and magnitude errors are compensated. Literatures describing various SPLL designs[54], refer to the presence of high frequency components from the phase detector that is inherent in the model[55–57] but state that the low pass nature of the loop filter itself attenuates those high frequency components[52, 53, 58–62]. Other literatures further stress the need of an input filter that selectively allows bandlimited signal in the loop[55, 62, 63]. The present work develops the SPLL with two additional blocks viz., an input bandpass filter to condition the voltage prior

to its introduction in the loop and a band stop filter that is tuned to filter out the higher frequency component and the loop filter is designed separately to reduce the steady state error.

The subsequent chapter will discuss the design of the instrumentation interface and the SPLL based control system that forms a generalized structure for future developments as well. In this respect, the mathematical realization for signal translation will also be reported. The instrumentation interface was developed to feed the Analog to Digital Converter (ADC) front end of the central controller with the field signals. The associated signal translation block was modelled and appropriately scaled for the DSP core. The isolation and component level design is also explained here. This design provides the basic scaling factors utilized during coefficient calculations. A theoretical analog controller was first envisaged which was then transformed to its corresponding digital equivalent and finally implemented using a fixed point DSP controller. The related modelling will be elaborated along with the result.

2.9.2 Scheme of the power block

The $3-\phi$ VSI is the final interface between the load and the energy source in SMES based DVR. PWM based VSIs invariably constitute an LPF stage for attenuating the higher frequencies arising due to the switching.

The earlier popular first-order L filter for the LPF stage had been gradually replaced by the second-order LC filter and more popularly, the third-order LCL filter which is fast gaining momentum as the alternatives. But with increasing filter order, additional control schemes are required for system stability that include methods such as current control strategy with an LCL filter [64], large

signal stabilizer design based on the circle criterion theory[65] to reject resonant oscillations, controller based on the composite nonlinear feedback control theory[66], a model predictive direct current control strategy[67] incorporating virtual resistor based active damping, a two-degree-of-freedom PID active damping method to attenuate the resonance that is caused by the LCL filter based systems[68], 7^{th} order LTCL filter[69] that efficiently filters the harmonics but does not decrease the control difficulties.

One of the basic requirements of higher order filter stems from the fact that the inductors (in case of L filter) and capacitors (in case of LC filters) required for the lower order filters are, owing to their higher ratings, generally costly and voluminous as well. The passive filter system, if lumped in the converter side of the step up injection transformer, has the advantage that voltage ratings of the components are reduced but the voltage drop across the inductor needs to be accounted for in the control scheme. Conversely, if these are lumped in the high voltage side, the harmonic currents will flow in the transformer windings[70]. In effect, the design becomes costly and voluminous.

Work in this regard includes a design methodology[71] to derive the lower value of the inductor based on inverter output peak current and the value of the capacitor is determined according to the requirement of the resonant frequency of the LC filter. Another design perspective was based on the relation among the filter, inverter and the controller assuming the load to be a pure resistor for a worst case scenario[72]. Design based on active damping is also proposed based on 1:1 isolation transformer[73]. Further developments have included design based on multiple impact factors[74] but here the unit is transformerless. Some literature[42] refers to the importance of the filter design and uses

a step-up transformer but does not discuss the design of the filter components. The present work, in this regard, is to supplement these by defining several performance indices to characterize a filter system and utilizes the transformer turns ratio i.e. the ratio of the number of turns in the secondary to that in the primary, advantageously in the design. In this, the transformer leakage inductance is considered to be negligible compared to the other inductances in the circuit. The design attempts to offer a practical choice of the filter components and proposes a novel LC filter topology for a $3-\phi$ VSI system that reduces the volume of the filter and assures a satisfactory attenuation thus eliminating the control overhead required in higher order filters.

Chapter 3

Control system

The Voltage Source Inverter (VSI) for the Dynamic Voltage Restorer (DVR) that is developed for the present study functions to keep the load voltage constant in case of any voltage sag at the mains with the assumption that the system is a balanced $3-\phi$ system. The controller samples the input mains, locks the phase and computes sag and ultimately injects the necessary series compensating voltage by the secondary of the Injection Transformer (IT). The present chapter explains the control module that locks the phase and computes the voltage sag. For this, a preliminary discussion on how the output voltage is to be synthesized is taken and also the low voltage instrumentation interface explained.

3.1 Synthesis of the output voltage

Once the sag amount is known, the rest of the exercise is to synthesize the compensating voltage to be injected in series with the mains to feed the load. Before the power electronic actuation is discussed, it may be noted that

besides the already available information regarding the amplitude and phase, a further correction is necessary which is due to the passive devices downstream to the power electronic bridge that contributes to both the amplitude and phase of the final inverter output. The instantaneous load voltage (V_l) requirement is to be accordingly translated to the inverter line-to-line output voltage (V_{invll}). But this requires deriving the phasor relationship between them. While deriving the characteristics of the LPF and its subsequent utilization in the DVR, it will be shown that the relation may be expressed in terms of the rated synchronized mains phase voltage (v_{pref}) and a correction term (k_t) which incorporates both the magnitude and phase compensation factors, as

$$V_{invll} = k_t v_{pref}$$

$$where,$$

$$k_t = |k_t| \angle \theta_t \tag{3.1}$$

This will be synthesized from the DC bus voltage (V_{dc}) and by appropriate switching of the power electronic switches of the VSI. From Appendix C it is seen that the phase voltages at a star-connected load may be represented as a function of the switching states of the inverter and the DC bus voltage. So the phase voltages of the pseudo star connected downstream load (Fig. 2.15)

will be

$$V_{invpp} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} = \frac{V_{dc}}{3}\begin{bmatrix} (2S_1 - S_2 - S_3) \\ (2S_2 - S_3 - S_1) \\ (2S_3 - S_1 - S_2) \end{bmatrix} \tag{3.2}$$

The phase matrix may be converted to the line voltages by transforming it with phase to line transformation (T_{p2l}) as

$$\begin{aligned} V_{invll} = T_{p2l}V_{invpp} &= T_{p2l}\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \\ &= \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \\ &= \frac{V_{dc}}{3}\begin{bmatrix} 3 & -3 & 0 \\ 0 & 3 & -3 \\ -3 & 0 & 3 \end{bmatrix}\begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} \\ &= V_{dc}\begin{bmatrix} (S_1 - S_2) \\ (S_2 - S_3) \\ (S_3 - S_1) \end{bmatrix} \end{aligned} \tag{3.3}$$

Both (3.2) and (3.3) may be used according to convenience of the phase configuration of the IT primary windings. The Clarke transformed matrix and its equivalent space vector computational steps are illustrated in Appendices A and C. The amplitude invariant Clarke transformed stationary $2-\phi$ line

signals will be

$$
\begin{aligned}
V_{invll\alpha\beta} &= \frac{2V_{dc}}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} (S_1 - S_2) \\ (S_2 - S_3) \\ (S_3 - S_1) \end{bmatrix} \\
&= \frac{2V_{dc}}{3}\begin{bmatrix} \frac{3}{2}(S_1 - S_2) \\ \frac{\sqrt{3}}{2}(S_1 + S_2 - 2S_3) \end{bmatrix} \\
&= V_{dc}\begin{bmatrix} (S_1 - S_2) \\ \frac{1}{\sqrt{3}}(S_1 + S_2 - 2S_3) \end{bmatrix} = \begin{bmatrix} V_{invll\alpha} \\ V_{invll\beta} \end{bmatrix}
\end{aligned} \tag{3.4}
$$

So the space vectors corresponding to the $2^3 = 8$ unique states of the power electronic switches may be listed as in Table 3.1. The same is illustrated

S_3	S_2	S_1	$V_{invll\alpha}$	$V_{invll\beta}$	$V_{invll\alpha\beta} = V_{invll\alpha n} + jV_{invll\beta n}$
0	0	0	0	0	0
0	0	1	V_{dc}	$\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{j\frac{\pi}{6}}$
0	1	0	$-V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{j\frac{5\pi}{6}}$
0	1	1	0	$\frac{2}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{j\frac{\pi}{2}}$
1	0	0	0	$-\frac{2}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{-j\frac{\pi}{2}}$
1	0	1	V_{dc}	$-\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{-j\frac{5\pi}{6}}$
1	1	0	$-V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}e^{-j\frac{\pi}{6}}$
1	1	1	0	0	0

Table 3.1: Clarke transformed vectors corresponding to the inverter line to line output voltages

in Fig. 3.1. Again from the derivations and illustrations in Appendix A, it becomes obvious that $(V_{invll\alpha}, V_{invll\beta})$ represents the required peak invari-

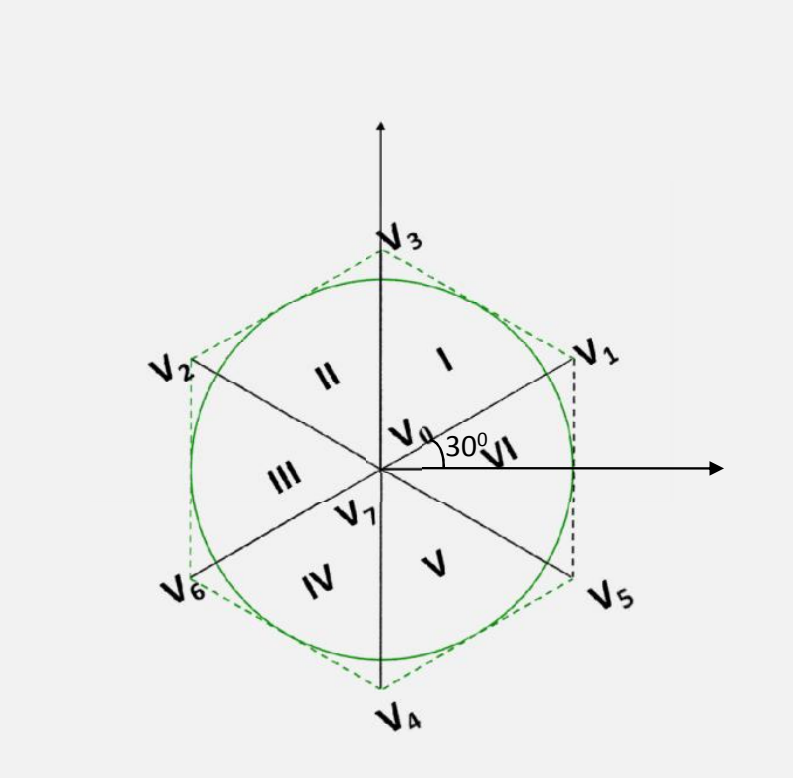

Figure 3.1: The space vectors corresponding to the VSI output line voltages

ant phase locked Clarke transformed compensating voltages. Following the same exercise as (C.11), (C.12) and (C.13) the sector and finally the weights (t_x, t_y, t_z) for the corresponding space vector $(V_s' \angle \theta)$ lying inside the n^{th} sector of the hexagon are obtained.

3.2 Modelling of the instrumentation scheme

The instrumentation of each phase is shown in Fig. 3.2. Potential Transformer (PT) is used to isolate and step-down the supply phase voltage (v_m) that is fed to control system electronics. The low voltage electronics processes the signal for interfacing with the ADC. This interface, termed as PTADC electronics (with parameters m_{PTADC} and c_{PTADC}), is required to

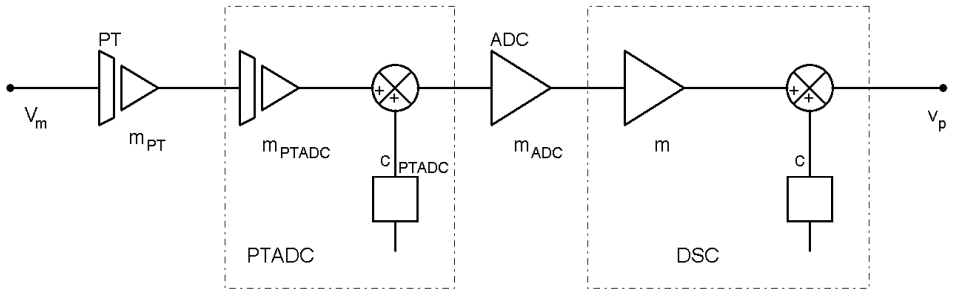

Figure 3.2: Instrumentation from mains to control system

scale and shift the signal according to ADC requirement. The selected ADC, integrated to the DSP chip, being unipolar cannot interface with negative signals with respect to its ground point. So the bipolar AC signal, available at the PT output, was needed to be accordingly shifted and further attenuated preserving both the magnitude and phase signature of the mains. The ADC converts this signal to its corresponding digital word, represented by the gain block (m_{ADC}), which is fed to the DSP based Digital Signal Controller (DSC) core. The DSC again shifts (c) and scales (m) the signal according to the requirement of the control system. The summary of the signal translation is listed as

$$v_{PT} = m_{PT} v_m \tag{3.5}$$

$$v_{PTADC} = m_{PTADC} v_{PT} + c_{PTADC} = m_{PTADC} m_{PT} v_m + c_{PTADC} \tag{3.6}$$

$$v_{ADC} = m_{ADC} v_{PTADC} = m_{ADC} m_{PTADC} m_{PT} v_m + m_{ADC} c_{PTADC} \tag{3.7}$$

$$v_p = m v_{ADC} + c = m m_{ADC} m_{PTADC} m_{PT} v_m + (m m_{ADC} c_{PTADC} + c) \tag{3.8}$$

or in a more compact form, as

$$v_p = m_{equiv} v_m + c_{equiv} \tag{3.9}$$

representing the equivalent gain and offset block as illustrated in Fig. 3.3, where,

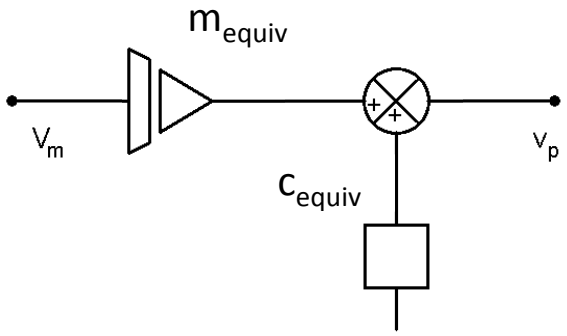

Figure 3.3: Equivalent block representing signal translation from mains to control system

$$\begin{aligned} m_{equiv} &= m m_{ADC} m_{PTADC} m_{PT} \\ c_{equiv} &= m m_{ADC} c_{PTADC} + c \end{aligned} \tag{3.10}$$

Now, the controller selected for the VSI system was TI make TMS320F2812 DSP controller with an internal SVPWM engine and an internal multichannel 12 bit ADC which was used to sample the input signal. Thus once the controller is fixed, so is the ADC and thus m_{ADC}. Again the input range of the ADC is 0 - 3 V and the range of the phase voltage is governed by the mains

supply which is 240 V rms. So m_{PT}, m_{PTADC} and c_{PTADC} will have to adjusted to step down and shift the input bidirectional medium voltage sinusoid to unidirectional low voltage range of 0 - 3 V. Thus these gains and offset will be fixed accordingly. So the only variables left to adjust are m_{equiv}, c_{equiv}, m and c. Now, in eq (3.9), a condition is imposed so that the final variable (v_p) is numerically equal to v_m. So, for two distinct cases of $v_{p1} = v_{m1}$ and $v_{p2} = v_{m2}$ the following simultaneous equations will be obtained

$$\left.\begin{aligned} v_{p1} &= m_{equiv}v_{m1} + c_{equiv} = m_{equiv}v_{p1} + c_{equiv} \\ v_{p2} &= m_{equiv}v_{m2} + c_{equiv} = m_{equiv}v_{p2} + c_{equiv} \end{aligned}\right\} \tag{3.11}$$

which, on solving, will give

$$m_{equiv} = 1,\ c_{equiv} = 0 \tag{3.12}$$

we get, from eq (3.9), $v_p = v_m$. So the last remaining set of variables, i.e., the DSC gain and offset are calculated as

$$\begin{aligned} m &= \frac{m_{equiv}}{m_{ADC}m_{PTADC}m_{PT}} = \frac{1}{m_{ADC}m_{PTADC}m_{PT}} \\ c &= c_{equiv} - mm_{ADC}c_{PTADC} = -\frac{c_{PTADC}}{m_{PTADC}m_{PT}} \end{aligned} \tag{3.13}$$

Thus, other values being known, m and c may be calculated for the DSC. A detailed computation illustrating the gains and offsets are recorded in the following subsection.

3.2.1 Computing the instrumentation gains and offsets

For the present case, the electronics consisted of stepping down the input signal by an LEM make LV 25 P voltage transducer and scaling and shifting the low voltage output by a properly biased instrumentation amplifier so as to match the ADC full scale input as shown in Fig. 3.4. Thus, essentially

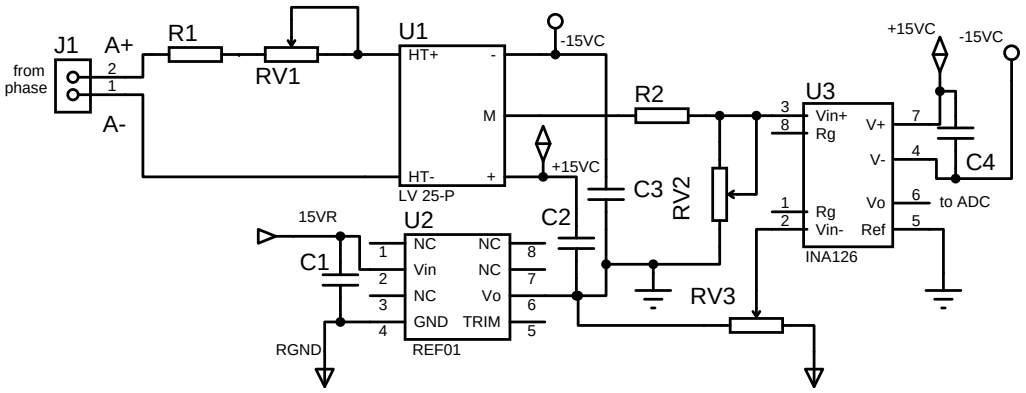

Figure 3.4: Scheme to transmit the phase signal to the ADC

for a 240 V rms (i.e. $240\sqrt{2}$V peak to peak), the input to the ADC will range from 0 to 3 V. Using these values in (3.6) for v_m and v_{PTADC} we obtain

$$\left.\begin{aligned} 240\sqrt{2}m_{PTADC}m_{PT} + c_{PTADC} &= 3 \\ -240\sqrt{2}m_{PTADC}m_{PT} + c_{PTADC} &= 0 \end{aligned}\right\} \tag{3.14}$$

Solving these simultaneously gives the equivalent gain and offset of the combined PT and PTADC block as

$$\left.\begin{aligned} m_{PTADC}m_{PT} &= \frac{1}{160\sqrt{2}} \\ c_{PTADC} &= 1.5 \end{aligned}\right\} \tag{3.15}$$

The ADC used was the integrated 12 bit ADC of the TI make TMS320F2812 digital signal controller. So,

$$m_{ADC} = \frac{(2^{12} - 1)}{3.0} = 1365.0 \tag{3.16}$$

Now, to satisfy (3.12) the gain and offset of the DSC block are computed as

$$m = \frac{1}{m_{ADC} m_{PTADC} m_{PT}} = \frac{160\sqrt{2}}{1365} = 0.1658 \tag{3.17}$$

$$c = -\frac{c_{PTADC}}{m_{PTADC} m_{PT}} = -1.5.160\sqrt{2} = -339.4113 \tag{3.18}$$

These values are set in the DSC to estimate the instantaneous phase voltages.

3.3 Control system model

Once the signal is acquired from the mains, it is used for sag detection and correction. The computational model is discussed here. The system is designed for mitigating voltage sag for a balanced $3 - \phi$ system i.e.,

$$\begin{aligned} V_{la} + V_{lb} + V_{lc} &= 0 \\ i_{la} + i_{lb} + i_{lc} &= 0 \end{aligned} \tag{3.19}$$

The DVR functions to keep the load voltage synchronised to the mains. Thus the control reference, v_{pref} needs to be defined. This information cannot be generated by a fixed DC reference as in a DC regulated power converter, but needs to be generated online to match the load phase angle requirement instantaneously. Also the phase contribution of the downstream electricals

needs to be computed and added to the phase of the mains in this regard. Though apparently this seems to be constant owing to the presence of passive components, but actually the phase angle contribution is also affected by the sag as will be derived later.

The phase lock for the mains and the detection of sag is based on Park Transformation (Appendix B) and Software Phase Locked Loop (SPLL) [52, 53] which will be discussed subsequently.

3.3.1 Detection of phase and sag magnitude at mains by SPLL

Phase angle and frequency information is critical for the control of FACTS and custom power devices[58, 60] like DVR. Appropriate provision must be kept so that under the condition of voltage sag at the utility mains, the phase of the mains is quickly locked to ensure quality output. A Phase Locked Loop (PLL) is an automatic choice for phase locking and to provide reference signal without distortion[75]. Among the several tasks accomplished by PLL like carrier recovery, clock recovery, tracking filters, frequency and phase demodulation, phase modulation, frequency synthesis[55], etc., these also find use in application with FACTS controllers. PLL actually forms the heart of controllers used for synchronizing tasks[62]. Here too, the PLL is the most popular choice due to its fast and accurate tracking of phase angle of utility voltages[76]. The PLLs can be configured as analog or hybrid but most of them belong to the hybrids composed of both analog and digital components[54]. The signal processing of the PLL, if carried out by a digital processor, is usually called Software PLL (SPLL) which have several advantages over its

hardware counterparts including immunity to ambient conditions, accuracy, reconfiguration capability, etc.[77]. Further, these are better suited for low frequency applications.

PLL basics

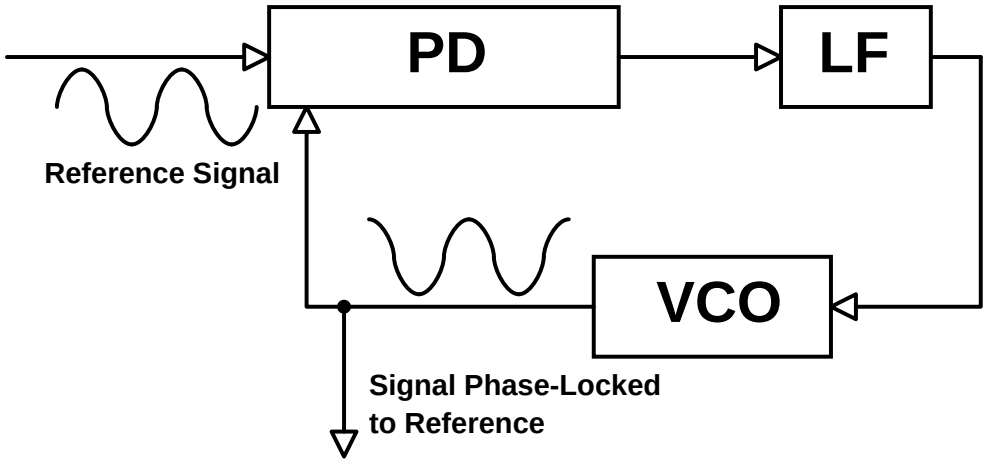

Figure 3.5: Basic block diagram of a PLL

The PLL, in its most basic representation, contains a Phase Detector (PD), a Voltage Controlled Oscillator (VCO) and a Loop Filter (LF) in closed loop. As illustrated in its general form in Fig. 3.5, the three components are arranged in a closed loop to achieve the desired functionality. The system contains two nonlinear devices - the PD whose output contains the phase difference between the two oscillating input signals and the VCO that produces an oscillation whose frequency is controlled by its input voltage. The LF, which may be omitted in a 1^{st} order PLL, is required otherwise for filtering that is essential for its correct functioning.

The basic idea of a PLL is that if any sinusoid is injected at its reference input, the internal oscillator in the loop will lock to the reference sinusoid in such a way that the frequency and phase differences between the reference and the internal sinusoids, depending on the type of system, are driven to 0 or some constant value. The internal sinusoid then represents a filtered or smoothed version of the reference sinusoid[55].

Analysis of PLL by linearization

Let the injected sinusoid be

$$v_i = R_i(t) = A\sin(\omega_i t + \theta_i) \tag{3.20}$$

and the output of the VCO, without any loss of generality[55], be

$$v_o = VCO_{out}(t) = \cos(\omega_o t + \theta_o) \tag{3.21}$$

The PD is essentially a mixer with gain K_m and it produces

$$\begin{aligned} v_d = Mixer_{out}(t) &= K_m v_i v_o \\ &= K_m A\sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) \\ &= 0.5K_m A\big(\sin((\omega_i + \omega_o)t + (\theta_i + \theta_o)) \\ &\qquad + \sin((\omega_i - \omega_o)t + \theta_d)\big) \qquad [\theta_d = \theta_i - \theta_o] \end{aligned} \tag{3.22}$$

Now, if the 1^{st} term in (3.22) can be attenuated and it can be ascertained that $\omega_i \approx \omega_o$, then for small and slow varying θ_d, the difference can be incorporated in θ_d itself which means, the VCO can be modelled as an integrator. This

leads to the conceptual PLL model of Fig. 3.6 where the PD is replaced by a summer and a gain (K_d), F(s) represents the loop filter and the VCO is replaced by an integrator with a gain (K_o).

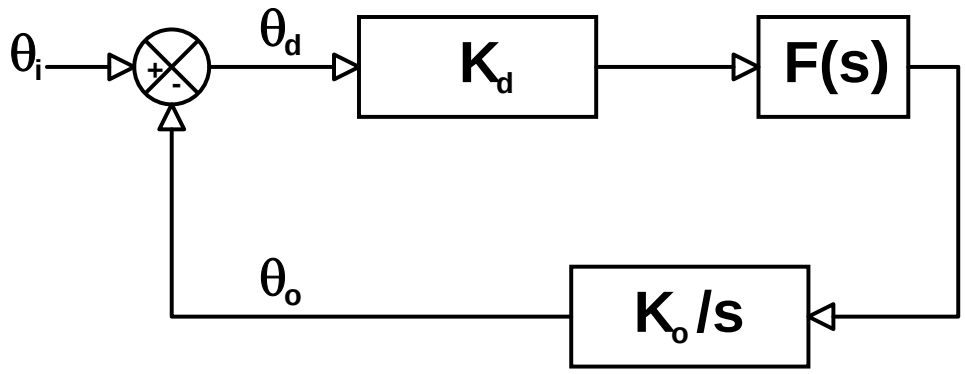

Figure 3.6: Conceptual block diagram of a PLL

Loop filter

Though it has been shown in [55] that the attenuation of the double frequency term of the PD output may be achieved by a high frequency low pass filter, a better option would have been a bandstop or a notch filter[56, 78] followed by the LF. Thus the Transfer Function (TF) of the LF may be expressed as

$$F(s) = G_{BS}(s)G_f(s) = k_{bs}\frac{s^2 + \omega_{bs}^2}{(s^2 + \frac{\omega_{bs}}{Q_{bs}}s + \omega_{bs}^2)}G_f(s) \tag{3.23}$$

To design the loop filter, the transfer function, $G_e(s)$, of the phase error, $\Theta_d(s)$ w.r.t. the input phase $\Theta_i(s)$ is investigated.

$$G_e(s) \triangleq \frac{\Theta_d(s)}{\Theta_i(s)} = \frac{1}{(1 + K_d F(s)\frac{K_o}{s})} = \frac{s}{(s + K_d K_o F(s))} \tag{3.24}$$

The presence of the integrator in VCO already makes it a type I system that produces zero steady state error to any phase step of $\theta_i(t)$ as follows,

$$\theta_d(t)_{ss}\Big|_{\Theta_i(s)=\frac{1}{s}} = \lim_{s\to 0} s\frac{1}{s}\frac{s}{(s + K_d K_o F(s))} = 0 \qquad [if\ F(0) \neq 0] \tag{3.25}$$

But to obtain the same for a ramp change of input phase, i.e. frequency,

$$\theta_d(t)_{ss}\Big|_{\Theta_i(s)=\frac{1}{s^2}} = \lim_{s\to 0} s\frac{1}{s^2}\frac{s}{(s + K_d K_o F(s))} = \frac{1}{K_d K_o F(0)} \tag{3.26}$$

As a non-zero F(0) is assumed to assure null steady state error to phase step, a finite value of the same makes a finite steady state error of the system to a frequency change. Now, the two popular loop filters that can be used are lead-lag[58] type and the Proportional+Integrator (PI) type. Their respective TF may be expressed as

$$\begin{aligned} G_{leadlag}(s) = k_{leadlag}\frac{(1 + T_1 s)}{(1 + T_2 s)} &\to \lim_{s\to 0} G_{leadlag}(s) = k_{leadlag} \\ G_{PI}(s) = (k_p + \frac{k_i}{s}) &\to \lim_{s\to 0} G_{PI}(s) \to \infty \end{aligned} \tag{3.27}$$

Thus it is clear that a PI filter is a better choice as this will track phase ramp signals also. This actually assures an infinite hold-in range, defined in[54] as

$$\omega_H = K_d K_o F(0) \tag{3.28}$$

Again, from the expression of the Open Loop TF (OLTF),

$$OLTF = K_d K_o k_{bs} \frac{s^2 + \omega_{bs}^2}{(s^2 + \frac{\omega_{bs}}{Q_{bs}} s + \omega_{bs}^2)} \big(k_p + \frac{k_i}{s}\big) \tag{3.29}$$

the lock-in range is evaluated as

$$\omega_L \approx \pm K_d K_o F(\infty) = \pm K_d K_o k_{bs} k_p \tag{3.30}$$

Now, keeping both the PD and the VCO gains unity, the Closed Loop TF (CLTF) of the system is given by

$$G(s) = \frac{\frac{G_{BS}(s) G_f(s)}{s}}{1 + \frac{G_{BS}(s) G_f(s)}{s}} = \frac{G_{BS}(s) G_f(s)}{s + G_{BS}(s) G_f(s)} \tag{3.31}$$

As the bandstop filter is affecting the gain of the system at its centre frequency and gives a constant gain at other frequencies, its gain is kept unity and the PI filter is designed by ignoring its effect and is validated by the final results. Thus,

$$CLTF \approx \frac{G_f(s)}{s + G_f(s)} = \frac{(k_p s + k_i)}{(s^2 + k_p s + k_i)}$$

$$= \frac{(k_p s + k_i)}{(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{3.32}$$

Thus,

$$\begin{aligned} \omega_n &= \sqrt{k_i} \\ \zeta &= \frac{k_p}{2\sqrt{k_i}} \end{aligned} \tag{3.33}$$

Now, assuming a lock-in range of ± 5 Hz and a damping coefficient of $\frac{1}{\sqrt{2}}$, the PI parameters are obtained as

$$\begin{aligned} k_p &= 2\pi \text{x} 5 = 31.42 \qquad [\text{from eq. (3.30)}] \\ k_i &= 493.48 \qquad [\text{from eq. (3.33)}] \end{aligned} \tag{3.34}$$

Taking $k_p = 30$ and $k_i = 500$ and the unity bandstop filter parameters with 0.8 quality factor and centre frequency of 100 Hz (as the system frequency is 50 Hz), the bode plots and the step responses are given as Fig. 3.7. The frequency and time response parameters viz. the Phase Margin (PM), Gain Crossover Frequency (GCF), Gain Margin (GM), Phase Crossover Frequency (PCF) and settling time (within 2% of the steady state limit) for both the cases are compared in Table 3.2. In this way it is observed from the plots and

PLL type	**PM** (^{0})	**GCF** **(Hz)**	**GM** **(dB)**	**PCF** **(Hz)**	**2% settling time** **(ms)**
without bandstop	63.55	5.33	0	-	216.30
with bandstop	59.69	5.32	782.67	98.37	210.60

Table 3.2: Comparing some frequency and time response parameters

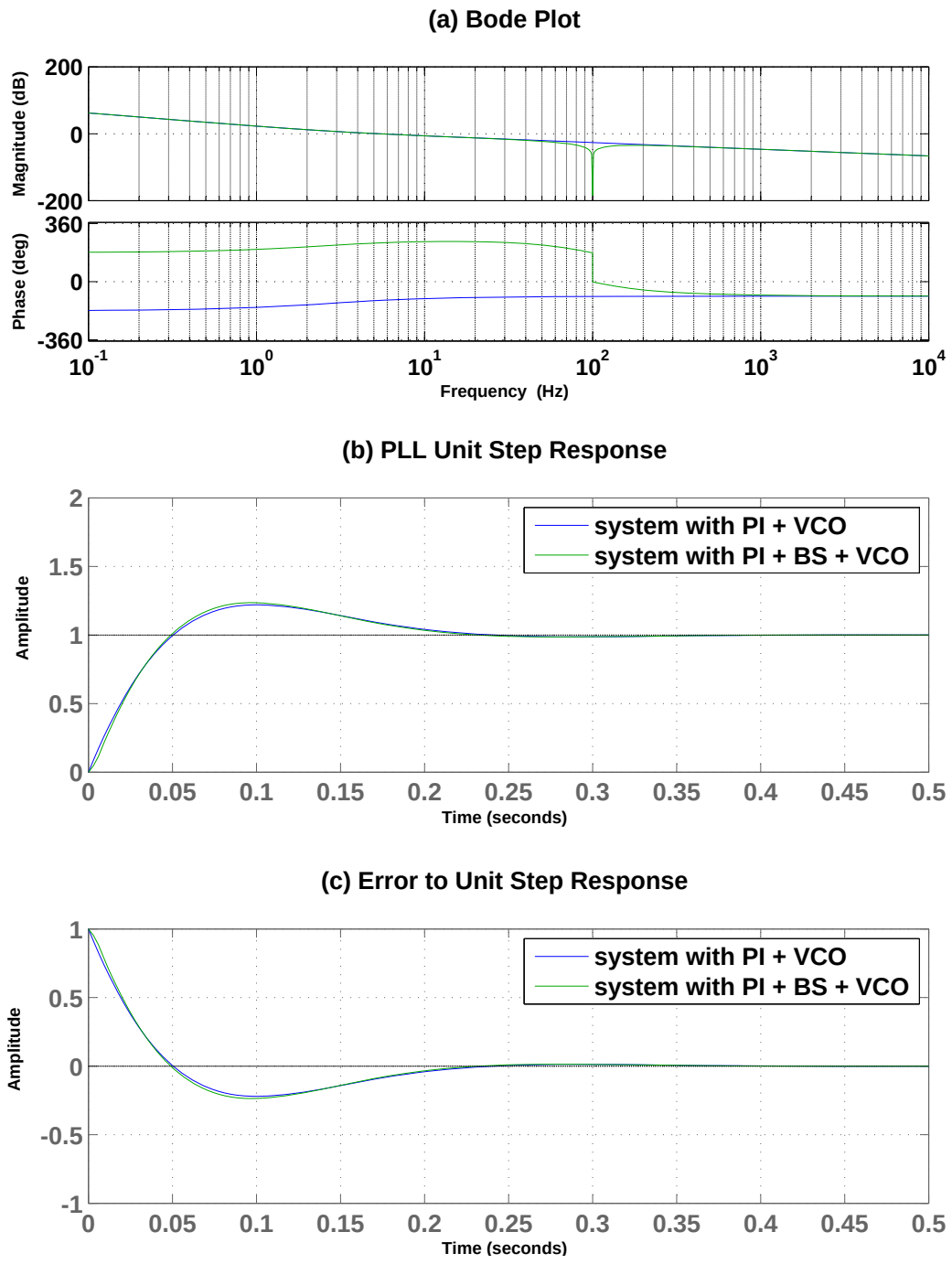

Figure 3.7: (a) Bode plot, (b) unit step response, (c) error response with unit step input of the system with (green) and without bandstop filter (blue)

the table that though the design was done without considering the bandstop filter, but it does not affect the essential parameters appreciably after the filter is used in the final model. In fact, it introduces a positive GM - a favourable index for a stable system. This validates our design theoretically. The settling time of 210 ms is sufficient as for a 50 Hz sinusoidal AC mains, to compensate for momentary sag, the allowable window, according to the corresponding IEEE standard, is 30 cycles i.e. 600 ms.

Input filter

Though not actually a part of the closed loop system, but a PLL for its proper functioning requires to reduce any broadband noise entering the system which influences on phase response. This can effectively be done if the input frequency range is known so that a bandpass filter may be introduced to attenuate any noise from the instrumentation system. The same is done by using a bandpass filter of TF

$$G_{BP}(s) = k_{bp}\frac{\omega_{bp}s}{(s^2 + \frac{\omega_{bp}}{Q_{bp}}s + \omega_{bp}^2)} \tag{3.35}$$

with the filter parameters as

gain (k_{bp}) = 1.0

centre frequency (ω_{bp}) = 2πx50

quality factor (Q_{bp}) = 0.8

Modelling with Park transformations

To utilize a PLL to lock the mains phase, the Park transformation method is employed. To illustrate the method it is assumed that the sag at the input mains is k_{sag} times the reference (nominal operating) voltage. So the sensed voltage (after corresponding scaling and conditioning) will be

$$V_{pn} = k_{sag} m_{equiv} v_{pref} = k_{sag} v_{pref} \qquad [\because m_{equiv} = 1] \tag{3.36}$$

After Park transformation using $(T_{3s2r}(\theta))$ and substitution of $\theta = \psi'$ we get,

$$v_{dq} = T_{3s2r}(\theta) V_{pn} = k_{sag} V_{ref} \begin{bmatrix} \cos(\omega t + \theta_m - \psi') \\ -\sin(\omega t + \theta_m - \psi') \end{bmatrix} \tag{3.37}$$

Normalizing the components w.r.t. V_{ref} gives

$$v_{dqn} = \frac{v_{dq}}{V_{ref}} = k_{sag} \begin{bmatrix} \cos(\omega t + \theta_m - \psi') \\ -\sin(\omega t + \theta_m - \psi') \end{bmatrix} = \begin{bmatrix} v_{dn} \\ v_{qn} \end{bmatrix} \tag{3.38}$$

v_{qn} is utilized as input to a SPLL algorithm that locks the input phase by bringing the phase difference and thus the normalised q component to 0 and in the process computes the sag. For this, an inversion of the signal is necessary and an inverter block is used for the purpose. The PD comprises of the $\alpha\beta$/dq block followed by the normalization and comparing the resultant v_{qn} with v_{qnref} $(= 0)$, finally passing it through the bandstop filter. The error is fed to a Proportional + Integrator (PI) block acting as the loop filter. The PI output is fed to a VCO that can be mathematically modelled as a summer that adds

the centre frequency (in this case the power line frequency, ω) followed by a resettable unity gain integrator (I)[79] that outputs the phase ψ', wrapped in the range of 0 to 2π. ψ' feeds to the $\alpha\beta$/dq transformation block thus completing the loop. The PI regulator maintains 0 input error at steady-state and will achieve phase lock condition for the $\alpha\beta$ and hence the abc components, this being achieved as $-\sin(\omega t + \theta_m - \psi') \approx -(\omega t + \theta_m - \psi')$ for small phase differences and $0 \leqslant k_{sag} \leqslant 1$. The control scheme is shown in Fig. 3.8. So for

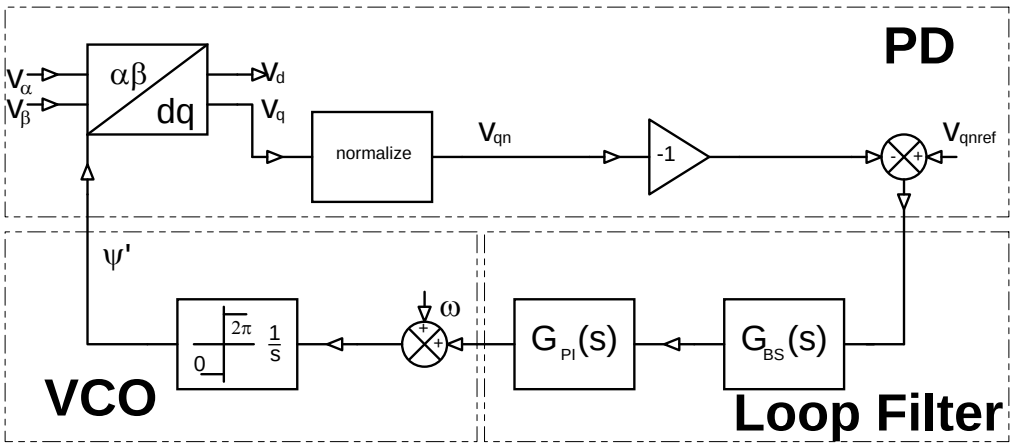

Figure 3.8: The control scheme for SPLL

$v_{qnref} = 0$ the output phase correctly tracks that of the input with a response dictated primarily by the PI controller. Once the phase is locked, v_{dn} will approach k_{sag} and v_{qn} will vanish as obvious from eq. (3.38).

3.3.2 Modelling the discrete control system

Discussion on the various transform methods available

To redesign the analog controller to its discrete equivalent, there are several methods available[30, 80]. A few popular methods are listed below.

- Backward difference
- Forward difference
- Impulse invariance
- Step invariance / Zero Order Hold (ZOH)
- Matched pole-zero
- Bilinear transform

The mapping methods for the above transforms are summarized in Table 3.3. Of these, the backward difference, the forward difference and the bilinear trans-

Transform	**Mapping**
Backward difference	$s \rightarrow \frac{1-z^{-1}}{T_s}$
Forward difference	$s \rightarrow \frac{1-z^{-1}}{T_s z^{-1}}$
Impulse invariance	$G_d(z) = T_s \mathcal{Z}[\mathcal{L}^{-1}[G_a(s)]]$
ZOH	$G_d(z) = \mathcal{Z}[\mathcal{L}^{-1}[\frac{1-e^{-T_s s}}{s} G_a(s)]]$
Matched pole-zero	a pole or zero at $s = -r$ is mapped to $z = e^{-rT}$, a pole or zero at infinity is placed at z=-1
Bilinear transform	$s \rightarrow \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$

Table 3.3: Transform methods and their s-domain to z-domain mapping

form are essentially numerical methods while the other methods are derived from various design perspectives. To understand how the left (stable) half of the s-plane appears in the z-plane under the three numerical methods, Fig. 3.9 may be referred whose shaded region shows the mapping in each case. Thus it may be seen that the forward difference method maps part of the left half

s-plane outside the unit circle (shown in dotted line) i.e., the stable region of the z-plane and thus is not recommended since a stable analog filter may result in an unstable discrete equivalent under this mapping. Bilinear transform, on the other hand, exactly maps the stable s-plane to the stable z-plane. Though the backward difference plane also maintains stability, but part of the region in the stable z-plane is never reached. This restricts the design to lowpass and bandpass filters having relatively small resonant frequencies and prevents transformations for cases like highpass filter based systems.

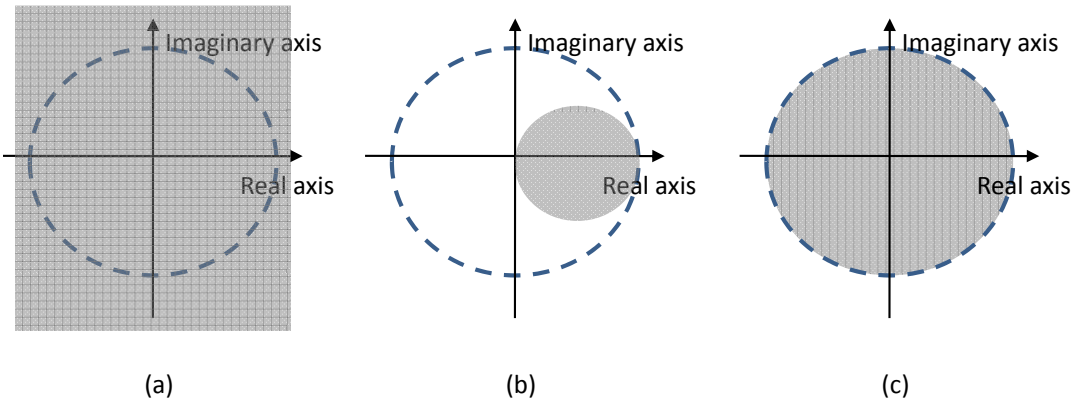

Figure 3.9: Mapping of left half of the s-plane by (a) forward difference, (b) backward difference and (c) bilinear transform into the z-plane

The impulse invariance method based filter is obtained by sampling the impulse response of the analog prototype. So, for an analog system, h(t), the corresponding discrete equivalent with impulse invariance will be

$$H(z) = \sum_{n=0}^{\infty} h(n) z^{-n} \tag{3.39}$$

Considering

$$z = e^{sT_s} \tag{3.40}$$

for every $s = \sigma + j\Omega$, the polar form of $z = re^{j\omega}$ may be expressed as

$$\begin{aligned} re^{j\omega} &= e^{(\sigma+j\Omega)T_s} \\ So, & \\ r &= e^{\sigma T_s} \\ \omega &= \Omega T_s \end{aligned} \tag{3.41}$$

Consequently, $\sigma \geqslant 0$ gives $r \geqslant 1$ and $\sigma < 0$ gives $0 < r < 1$. So the left hand s-plane is mapped inside the unit circle of the z-plane but a problem remains if it is observed that the mapping of $j\Omega$ into the unit circle is many to one. This is so as for any integral value of k, the interval $(2k-1)\pi \leqslant \Omega \leqslant (2k+1)\pi$ maps always to $-\pi \leqslant \omega \leqslant \pi$. This actually leads to aliasing in the frequency domain[25].

The same is true for matched pole-zero case where the poles and zeros on the left half s-plane is mapped into the interior of the z-plane unit circle. So in order to preserve the frequency response of the analog filter and to avoid aliasing, T_s must be carefully selected and must be sufficiently small.

The step-invariance method or the zero-order-hold (zoh) method is also another transformation used for analog to digital conversions. In this method, samples are blocked and held for the specified T_s thus retaining the values till the next samples come. This is shown schematically in Fig. 3.10. But it

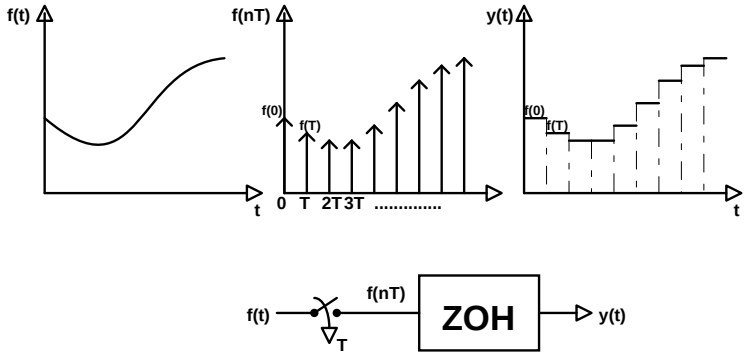

Figure 3.10: Scheme of the ZOH (step invariant) method

suffers from the fact that the frequency response is distorted[81].
Considering these, the bilinear transform method is selected for the present purpose which preserves stability and maps every point of the frequency response of the continuous-time system to a corresponding point in the frequency response of the discrete time equivalent although at a somewhat different frequency which only becomes appreciable nearer to the Nyquist frequency[30, 80].

SPLL using bilinear transform

Using bilinear transform of each of the TF blocks with sampling frequency of 5 kHz, the z transformed TF are evaluated and shown in Table 3.4. From this, the OLTF and the CLTF of both the systems are computed and are compared as in Fig. 3.11 and Fig. 3.12. From the Bode plot and the time responses, the comparison of the digital equivalent is summarised in Table 3.5. The comparison justifies that the design may be utilized for implementation in digital processor with the computed coefficients.

analog TF	**z transformed TF**
$G_{BS}(s) = \dfrac{s^2 + 3.948\text{x}10^5}{(s^2 + 785.4s + 3.948\text{x}10^5)}$	$G_{BS}(z) = \dfrac{0.9274 - 1.84z^{-1} + 0.9274z^{-2}}{1 - 1.84z^{-1} + 0.8549z^{-2}}$
$G_{PI}(s) = \dfrac{30s + 500}{s}$	$G_{PI}(z) = \dfrac{30.05 - 29.95z^{-1}}{1 - z^{-1}}$
$G_{VCO}(s) = \dfrac{1}{s}$	$G_{VCO}(z) = \dfrac{0.0001 + 0.0001z^{-1}}{1 - z^{-1}}$

Table 3.4: TF of the various blocks of the analog and software PLL

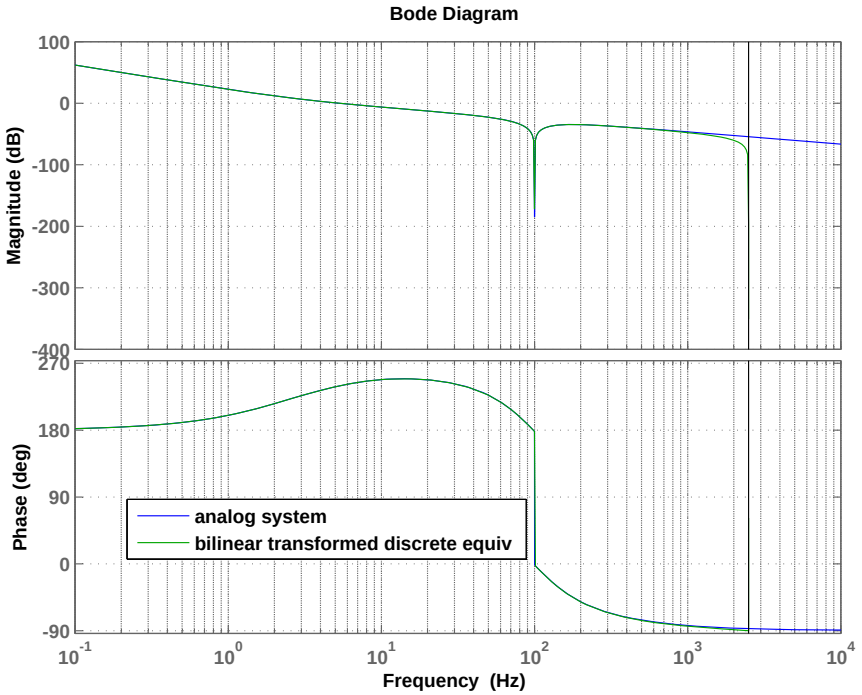

Figure 3.11: Comparing the bode plots of the analog PLL (blue) with the bilinear transformed discrete equivalent SPLL (green)

PLL type	**PM (^{0})**	**GCF (rad/s)**	**GM (dB)**	**PCF (rad/s)**	**2% settling time (ms)**
analog PLL	59.69	5.32	782.67	98.37	210.60
SPLL	59.69	5.32	746.58	98.17	210.60
error %	0.0	0.0	4.16	0.20	0.0

Table 3.5: Comparing frequency and time response parameters of analog PLL and SPLL

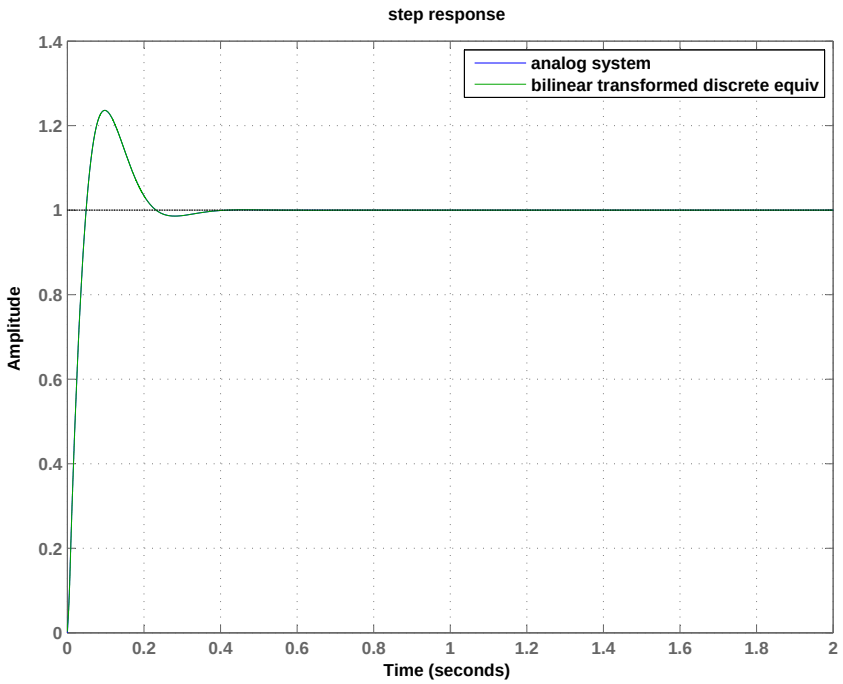

Figure 3.12: Comparing the step responses of the analog PLL (blue) with the bilinear transformed discrete equivalent SPLL (green)

Input filter using bilinear transform

The same transform is applied to the bandpass filter with sampling frequency of 5 kHz to yield the corresponding $G_{BP}(z)$ as

$$G_{BP}(z) = \frac{0.0302 - 0.0302z^{-2}}{1 - 1.921z^{-1} + 0.9245z^{-2}} \tag{3.42}$$

Simulations

Each of the blocks with TF, G(z) of the form

$$G(z) = \frac{R(z)}{U(z)} = \frac{(d_0 + d_1z^{-1} + d_2z^{-2})}{(1 + c_1z^{-1} + c_2z^{-2})} \tag{3.43}$$

corresponds to the difference equation

$$r_0 = d_0u_0 + d_1u_{-1} + d_2u_{-2} - c_1r_{-1} - c_2r_{-2} \tag{3.44}$$

where r_{-i} and u_{-j} respectively represents the output and input sequences for the i^{th} and j^{th} past samples. A code is developed using this form with

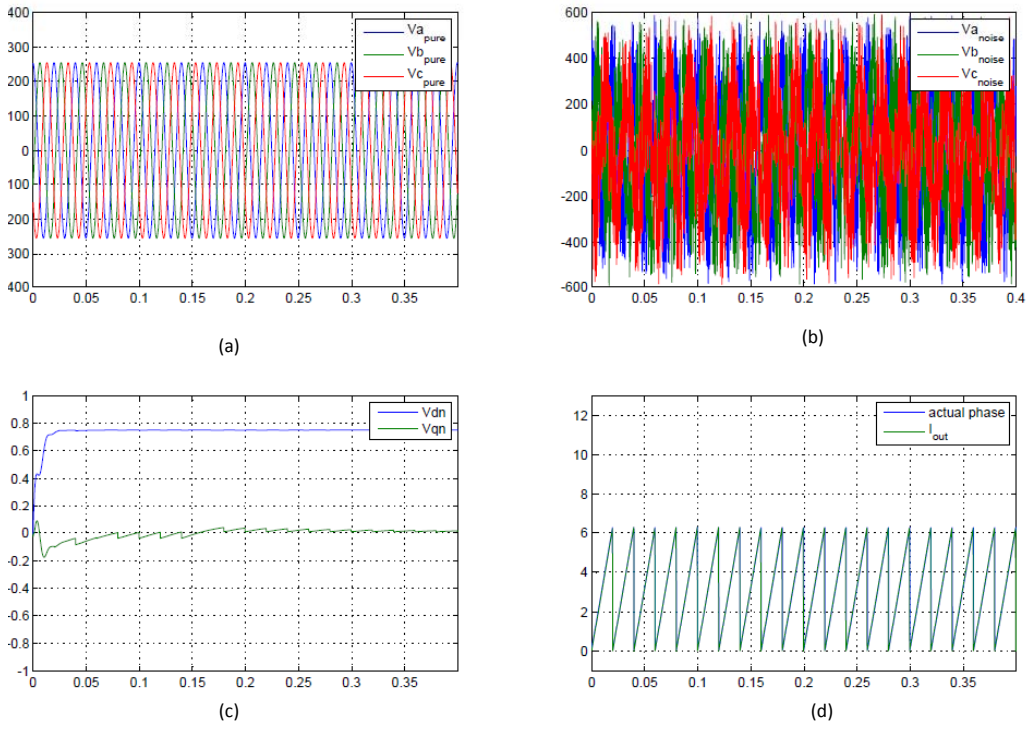

Figure 3.13: SPLL time domain characteristics corresponding to mains sag = 0.75, (a) the pure mains signal, (b) the signal buried in noise, (c) the normalized dq components, (d) comparison of the mains phase and the integrator output of the SPLL

variable sag values to test the SPLL algorithm. A random noise of maximum amplitude same as the signal peak-to-peak value is added to the ideal signal and a random input phase is assumed. Sags to 0.75, 0.5, 0.25 of the 240 V

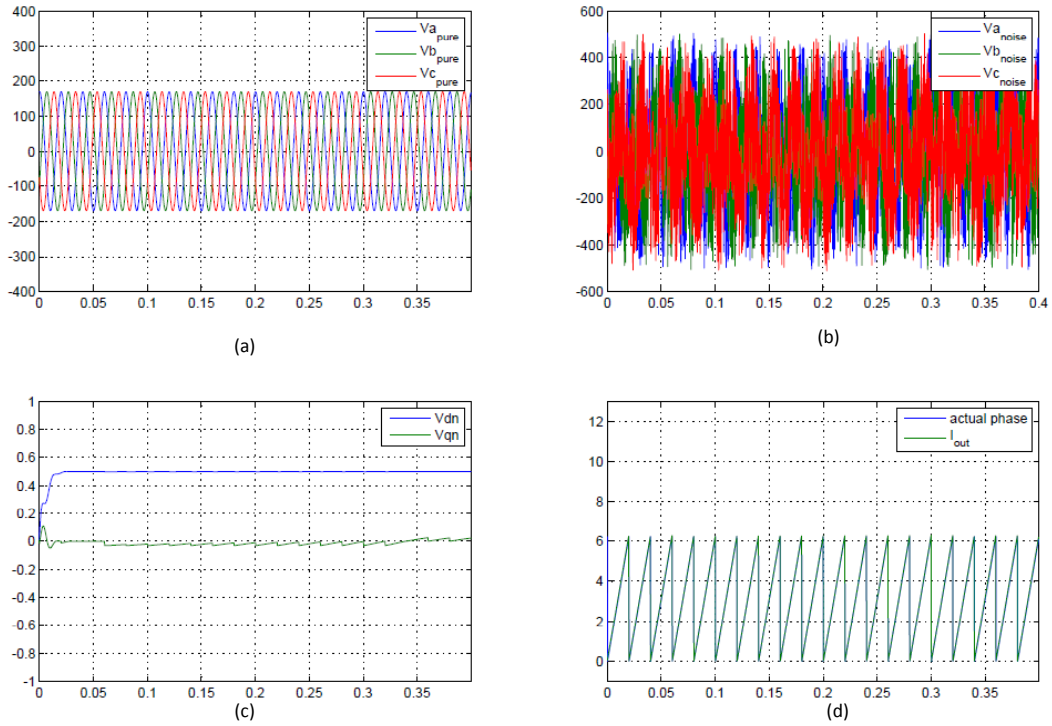

Figure 3.14: SPLL time domain characteristics corresponding to mains sag = 0.5, (a) the pure mains signal, (b) the signal buried in noise, (c) the normalized dq components, (d) comparison of the mains phase and the integrator output of the SPLL

mains is selected and the corresponding results are plotted. The plots in Fig. 3.13 - 3.15 shows that phase lock and sag detection (V_{dn}) are achieved in each case.

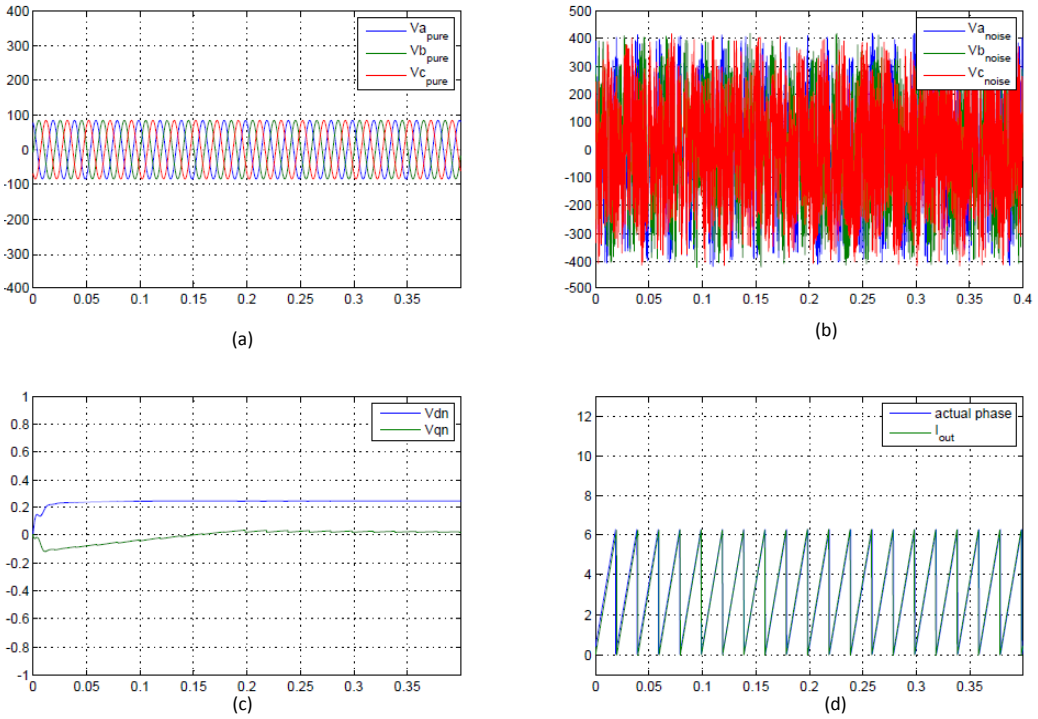

Figure 3.15: SPLL time domain characteristics corresponding to mains sag = 0.25, (a) the pure mains signal, (b) the signal buried in noise, (c) the normalized dq components, (d) comparison of the mains phase and the integrator output of the SPLL

Chapter 4

Power low pass filter

The control system based on the SPLL outputs the phase and the sag fraction of the mains. The information serves as the basis of the gate drive module that generates the necessary gate signal for the power electronics based full bridge that ultimately synthesizes the compensating voltage. This chapter deals with the design of the Low Pass Filter (LPF) system, an invariable constituent of a PWM based inverter. As the present discussion considers the design of the filter system only, the input mains are omitted and the three input phases in the model are shorted to the neutral which does not compromise generalization and is equally applicable when the VSI is used as a compensator in the DVR scheme. Actually the scheme represents the VSI operating for a full voltage sag.

4.1 Introduction to general VSI filter system

With a higher rating of the inverter, the volume and cost of the filter components increases. With time, the design has evolved from the simpler first

order L filter to second order LC filter and more recently the third order LCL filters. As has already been discussed in section 2.9.2, the improved efficiency in attenuating high frequency components, arising from the switching of the inverter bridge, had been achieved at the cost of complex controls for maintaining system stability. Several such methods and filter designs are reported in [42, 64–69, 71–74].

The present chapter introduces a new method to characterize a filter system by defining several performance indices. This offers a practical choice of the filter components and proposes a novel LC filter topology for a $3-\phi$ VSI system that reduces the volume of the filter and assures a satisfactory attenuation thus eliminating the control overhead required in higher order filters. The final configuration advantageously utilizes the injection transformer's turns ratio (n). It may here be noted, the phase sequences are referred as *abc* if $V_{lc} = V_{lb}e^{j\frac{2\pi}{3}} = V_{la}e^{-j\frac{2\pi}{3}}$ and *acb* if $V_{lb} = V_{lc}e^{j\frac{2\pi}{3}} = V_{la}e^{-j\frac{2\pi}{3}}$.

4.2 Load ratings

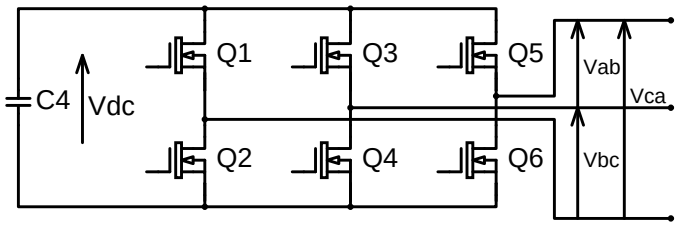

Figure 4.1: IGBT based full wave VSI system

The design could have assumed any load but it is normalized with respect to $3-\phi$ 240V, 50Hz system feeding a star connected resistive load 50Ω

(R_l) per phase. Thus the total load KVA (S_l) and current per phase ($I_{l,ph}$) are given as

$$S_l = 3\frac{V_{la}^2}{R_l} = 3.456KVA \quad \text{and} \quad I_{l,ph} = \frac{V_{la}}{R_l} = 4.8A \tag{4.1}$$

The drivers (Concept make 2SP0115T2Ax-FF450R12ME4) that were selected for the IGBT (Infineon make FF450R12ME4) based full bridge (Fig. 4.1) limits the choice of the maximum switching frequency (19 kHz in this case). As the output fundamental frequency, to be passed through the filter system, is same as that in the line (50 Hz), the gate triggering is selected two decades (100 times) above that at 5 kHz ($\equiv$ 3.14x10^{4}rad/s), well within the range of the selected IGBTs.

4.3 Conventional topologies and their improvisations

The conventional filter design, for attenuating switching frequency in an inverter system, lumps the filter components either in the primary (Fig. 4.2) or in the secondary (Fig. 4.3) side of the transformer (IT in this case), hereby referred to as L_pC_p and L_sC_s schemes respectively. The various parameters of the components that constitute the filter are then computed based on the load requirement and accordingly the design proceeds. In this regard, though the primary motivation is to design a filter system that will effectively reject all other frequency components barring the required one, another point needs to be addressed simultaneously for practical realization of the model, which is discussed next.

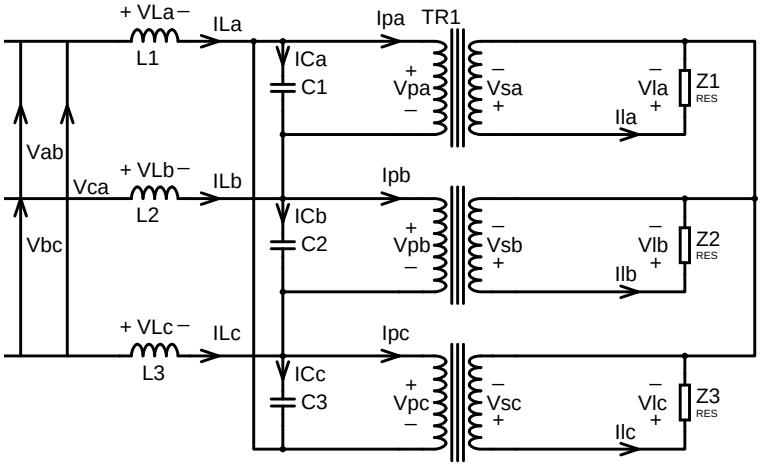

Figure 4.2: VSI with LC in transformer primary (L_pC_p)

4.3.1 Rating considerations for the filter components

For the inductor, a higher AC current flow means a higher power rating requiring an increase in the corresponding bulk of ferrite core that may not always be easily available. This results in stacking of available cores to increase the rating. Due to the brittleness of the core, the mounting pressure is to be carefully considered as less pressure may cause relative displacement of the cores during energization leading to a change of inductance during operation while higher pressure may cause damage of the material itself. Also, the problem of increased coil dimensions with increasing current may result in inadequate window space as offered by the geometry of the available core. CRGOS laminations could have solved the problem but its poorer frequency response at higher frequencies prevents its use as the inductor core material in the present case though when the high frequency is attenuated by the filter capacitor, the IT core will be CRGOS.

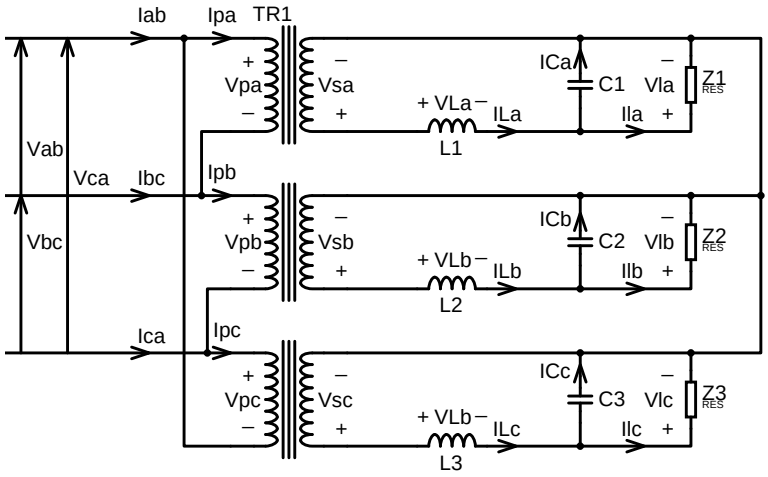

Figure 4.3: VSI with LC in transformer secondary (L_sC_s)

In the case of the capacitor, it may be noted that unlike the usual polarized capacitors used for DC power supplies, non-polarized capacitors are required to operate in both the cycles of the input sinusoid. It is also a practical problem of obtaining such a higher value of non-polarized capacitor that has a higher voltage rating and a high ripple current capability. One of the way-outs is the design of capacitor networks of series-parallel combinations to achieve the required capacitance and the voltage rating. But this will not be a general model and for a change in the requirement, a new network is to be designed to cater to the purpose. This makes the design voluminous as well.

Now, in the present case it may be observed, that the presence of a transformer, with turns-ratio (n) > 1, causes the secondary voltage to be stepped up while the secondary current is stepped down and just the reverse if the turns-ratio is less than one. This property may be utilized advantageously by placing the L and C strategically so that their ratings are favourably affected. As this will finally affect the cut-off and damping ratio, the reverse of the

scheme is also tested for completeness. These are illustrated in Figures 4.4 and 4.5 and referred to as C_pL_s and L_pC_s respectively.

In this regard, it may be pointed out, that the implementation of the C_pL_s configuration will cause overcurrent peaks in the IGBTs of the inverter. However, this configuration has been studied for the sake of completeness and for comparing its filtering performance with that of the other configurations.

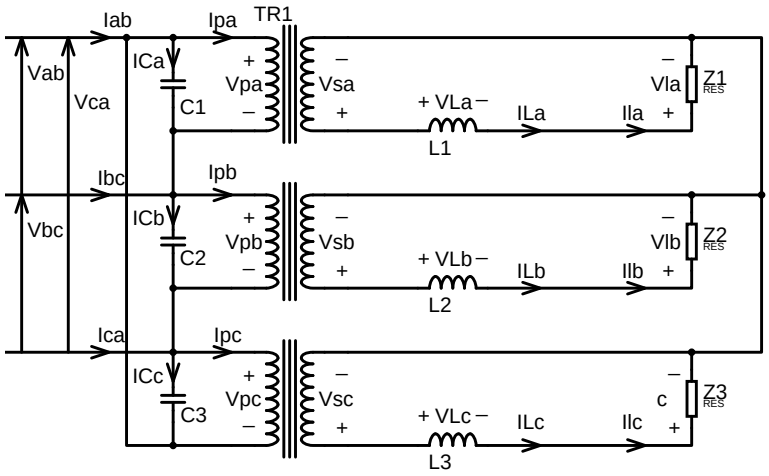

Figure 4.4: VSI with C in transformer primary and L in secondary (C_pL_s)

4.3.2 Indices of performance

From the previous arguments, it may be reasoned that the indices that may categorise a practical filter besides its capability to attenuate the unwanted harmonics are the ratings of the inductor current and the capacitor voltage. Thus it is proposed that the indicative parameters that will describe the performance of the filter are the capacitor voltage normalized to the load voltage (n_{Cl}) and the inductor current normalized to the load current (n_{Ll}). These, along with the filter transfer function (G_{LP}) with respect to the inverter

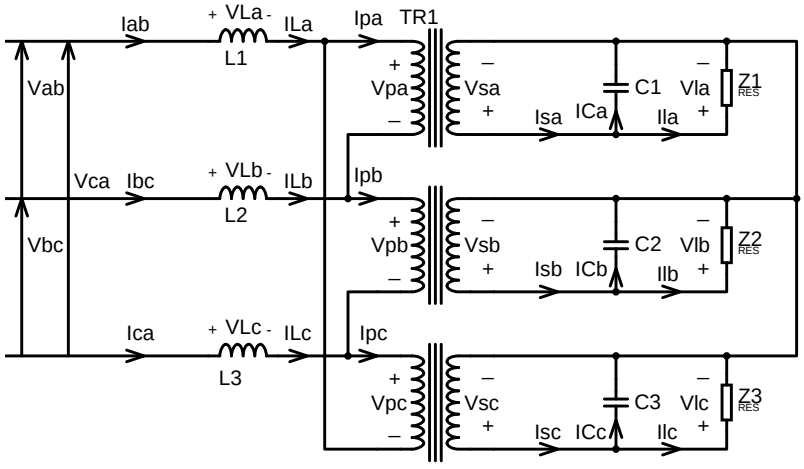

Figure 4.5: VSI with L in transformer primary and C in secondary (L_pC_s)

line to line voltage (V_{ab}, V_{bc}, V_{ca} as is the case) are thus formulated by

$$\left.\begin{aligned} G_{LP}(j\omega) &= \frac{V_{lx}(j\omega)}{V_{xy}(j\omega)} \\ n_{Cl}(j\omega) &= \frac{V_{Cpx}(j\omega)}{V_{lx}(j\omega)}\ or,\ \frac{V_{Csx}(j\omega)}{V_{lx}(j\omega)} \\ n_{Ll}(j\omega) &= \frac{I_{Lpx}(j\omega)}{I_{lx}(j\omega)}\ or,\ \frac{I_{Lsx}(j\omega)}{I_{lx}(j\omega)} \end{aligned}\right\} \tag{4.2}$$

where,

$$\begin{aligned} &x : \text{phase a, b or c} \\ &y : \text{next phase according to the sequence} \end{aligned} \tag{4.3}$$

The two formulations, each for n_{Cl} and n_{Ll}, corresponds to whether the capacitor or inductor is placed in the primary or secondary side of the transformer. It may be noted at this stage that further analyses, by decoupling a 3-ϕ system

to three 1-ϕ systems, will be restricted to phase a only, since in a balanced system, the results are similar for the rest of the phases.

The filter transfer functions and the corresponding indices for the circuits of Fig. 4.2 - 4.5 are listed as in Tables 4.1 and 4.2 [for detailed analysis see Appendix D]. The parameters of the filter transfer functions viz., the

Topology	$G_{LP}(j\omega)$
L_pC_p	$\dfrac{n/(3L_pC_p)}{\left(-\omega^2 + j\dfrac{n^2}{R_lC_p}\omega + \dfrac{1}{3L_pC_p}\right)}$
L_sC_s	$\dfrac{n/(L_sC_s)}{\left(-\omega^2 + j\dfrac{1}{R_lC_s}\omega + \dfrac{1}{L_sC_s}\right)}$
C_pL_s	$\dfrac{nR_l/L_s}{\left(\dfrac{R_l}{L_s} + j\omega\right)}$
L_pC_s	$\dfrac{1/(3nL_pC_s)}{\left(-\omega^2 + j\dfrac{1}{R_lC_s}\omega + \dfrac{1}{3n^2L_pC_s}\right)}$

Table 4.1: Load voltage normalized to VSI output line voltage

Topology	$n_{Ll}(j\omega)$	$n_{Cl}(j\omega)$
L_pC_p	$\sqrt{3}\left(n + \dfrac{j\omega R_lC_p}{n}\right)e^{j\frac{p\pi}{6}}$	$1/n$
L_sC_s	$\left(1 + j\omega R_lC_s\right)$	1
C_pL_s	1	$\dfrac{1}{n}\left(1 + j\dfrac{\omega L_s}{R_l}\right)$
L_pC_s	$\sqrt{3}n\left(1 + j\omega R_lC_s\right)e^{j\frac{p\pi}{6}}$	1

Table 4.2: $n_{Ll}(j\omega)$ and $n_{Cl}(j\omega)$, for both abc ($p = +1$) and acb ($p = -1$) phase sequences

cut-off frequency (ω_n), damping constant (ζ) and dc gain (K) for different

topologies are summarized for comparison in Table 4.3.

Topology	ω_n	ζ	K
L_pC_p	$\frac{1}{\sqrt{3L_pC_p}}$	$\frac{\sqrt{3}n^2}{2R_l}\sqrt{\frac{L_p}{C_p}}$	n
L_sC_s	$\frac{1}{\sqrt{L_sC_s}}$	$\frac{1}{2R_l}\sqrt{\frac{L_s}{C_s}}$	n
C_pL_s	$\frac{R_l}{L_s}$	-	n
L_pC_s	$\frac{1}{n\sqrt{3L_pC_s}}$	$\frac{\sqrt{3}n}{2R_l}\sqrt{\frac{L_p}{C_s}}$	n

Table 4.3: Comparison of parameters of the filter transfer functions for various LPF topologies

It is thus observed that not only do the magnitudes of L and C, but n also play an important role in determining the ratings of the filter components. But unfortunately, the indices and transfer function being coupled to each other, improving one may adversely affect one or both of the others. So three sets, each of n $\{0.1, 1.0, 10\}$, L$\{10\mu H, 100\mu H, 1000\mu H\}$ and C $\{10\mu F, 100\mu F, 1000\mu F\}$ are considered representing three different orders of magnitude to examine the effectiveness of each topology.

It may here be noted that being a first order system, C_pL_s configuration will provide poorer attenuation than the other three. Also, its configuration adversely affects the IGBT functioning. Considering these, further discussions regarding this particular configuration is omitted.

4.3.3 Selecting the condition to compare the performance

As n_{Cl} and n_{Ll} are also functions of frequency, we select a common frequency viz., the desired system (load) frequency i.e. 50Hz, for comparing

the parameters. Now, to choose the filter cut-off frequency, we may follow [71] which proposed the criteria $10f_s \leqslant f_r = \dfrac{1}{2\pi\sqrt{LC}} \leqslant Mf_{sw}$ (f_s, f_{sw} are respectively the system frequency and the PWM switching frequency) with M in the range [0.1, 0.5]. But considering the present case with system frequency of 50 Hz and PWM switching frequency of 5 kHz, the lower limit ($10f_s = 500Hz$) coincides with the lower range ($0.1f_{sw}$) of the upper limit. This happens as the difference of order between the system frequency and the switching frequency is not very high. For this reason, an additional constraint is included in the design viz., the settling time for the filter.

As the target design is a DVR system that is supposed to mitigate momentary voltage sags at the mains with a voltage tolerance of 10%, it is expected that the filter settling time is within a few cycles. Also, considering the presence of the electrical contactors which is supposedly the slowest device to respond (at least 2-4 cycles), the settling time (t_{settle}) is taken to be a quarter of a 50 Hz cycle, i.e., 5 ms and a 5% settling band is considered. From definition, this will correspond to

$$\zeta\omega_n = -\frac{\ln 0.05}{t_{settle}} = 599.15\ rad/s \tag{4.4}$$

With this, the damping constant and the attenuation at f_{sw} with respect to f_s for various f_n is tabulated in Table 4.4. From this table it is observed that if $3f_s \leqslant f_n \leqslant 5f_s$, then the attenuation is more than 50dB as well as the circuit is not very much underdamped. On this basis, the cut-off frequency is selected at 5 times the system frequency.

f_n	$20\log\lvert\frac{G_{LP}(jf_s)}{G_{LP}(jf_{sw})}\rvert$	ζ
50 Hz	68.38 dB	1.91
100 Hz	66.28 dB	0.95
150 Hz	61.05 dB	0.64
200 Hz	56.20 dB	0.48
250 Hz	52.27 dB	0.38
300 Hz	49.04 dB	0.32
350 Hz	46.31 dB	0.27
400 Hz	43.95 dB	0.24
450 Hz	41.86 dB	0.21
500 Hz	40.00 dB	0.19

Table 4.4: Comparison of attenuation and damping constant for various cut-off frequencies

4.3.4 Comparing the ratings of L and C based on the fixed cut-off frequency

From Table 4.3 it may be observed that the inductance will vary inversely as the capacitance for a constant cut-off frequency but the proportionality constant will depend on the particular topology. Thus, for a constant cut-off frequency and capacitance (inductance), the L_pC_p configuration, always gives a lower inductance (capacitance) than the L_sC_s ($\sqrt{3}$ times less) but it is higher (by a factor of n) than what is offered by L_pC_s if the transformer used is a step-up one.

The current rating of the inductor at the power frequency is reflected by the magnitude of n_{Ll}. Its variation as a function of n and capacitor value for each of the three topologies, viz., L_pC_p, L_sC_s and L_pC_s, is shown in Fig. 4.6. The family of graphs for each topology corresponds to the variation of n_{Ll} vs n for different capacitor values. Fig. 4.7 shows the variation of n_{Cl} with n for each of the topologies that reflects similarly the voltage rating of the filter

capacitors. From these, the following points are of significance for the present purpose.

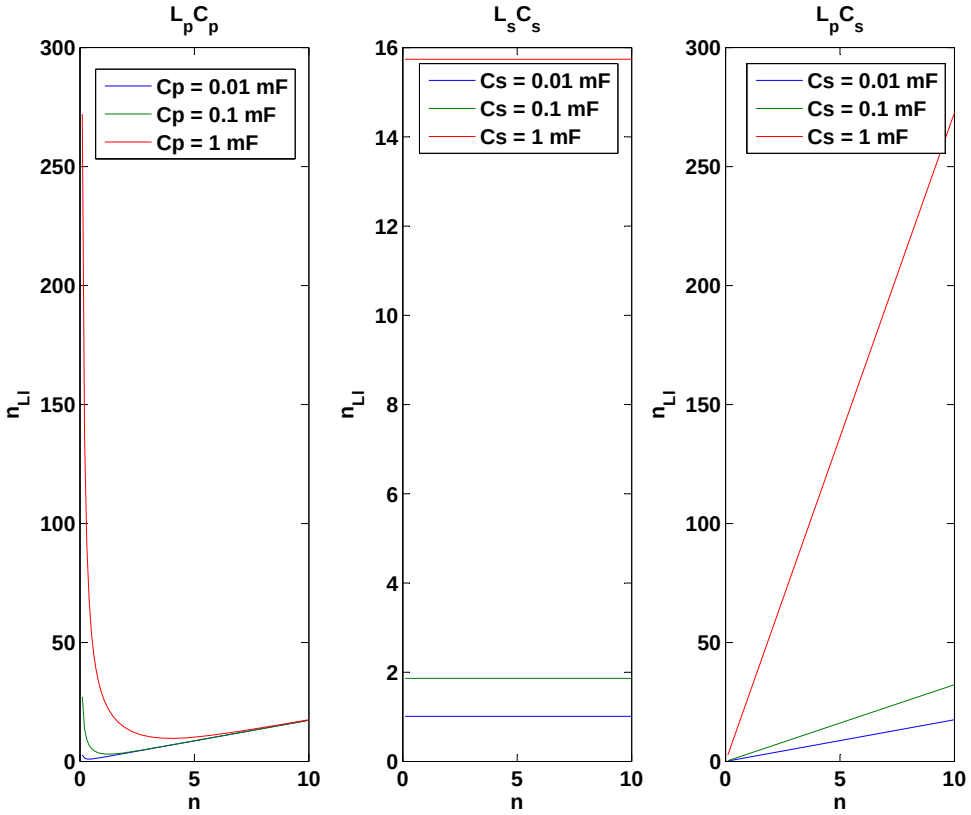

Figure 4.6: n_{Ll} vs n for different capacitor values for the L_pC_p, L_sC_s and L_pC_s configurations

1. For the same cut-off frequency and the capacitance (inductance) value, the inductance (capacitance) required is always lower in L_pC_p than in L_sC_s but for a step-up transformer, the lowest inductance (capacitance) is offered by the L_pC_s topology.

2. The current rating of the inductor in L_sC_s is the lowest for the complete

range of the turns-ratio and the load considered, while that in the L_pC_p configuration becomes more or less same for large n (> 10) that also matches the L_pC_s plot if C_s is of the order of $10\mu F$.

3. The voltage rating of the capacitors used in L_sC_s and L_pC_s are same and constant which is higher/equal/lower than that for the L_pC_p situation for a step-up/isolation/step-down transformer respectively.

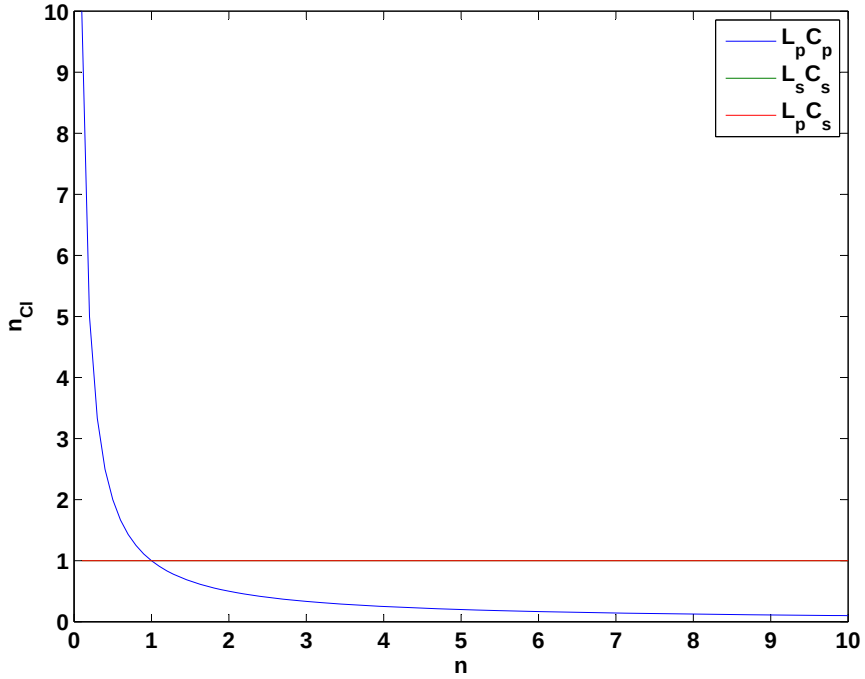

Figure 4.7: n_{Cl} vs n for configurations L_pC_p, L_sC_s and L_pC_s

4.3.5 Summarizing the observations

From the previous two subsections it is observed that lower ratings (voltage, current, inductance and capacitance values) of the filter component

are favoured if the transformer selected is a step-up one. It is also seen that with a step-up transformer, the inductance (capacitance) requirement is the lowest for the L_pC_s configuration for identical value of the capacitance (inductance). Thus the L_pC_s configuration would have been the best option but for the fact that the voltage rating of the capacitor in this case, or more generally in the case when it is placed in the secondary side, becomes same as the load voltage. The availability of such capacitors are poor and they are also very costly. To counter this limitation, a novel topology is proposed and discussed in the next section.

4.4 A novel topology

Considering the previous rationale, a step-up transformer with C distributed in both the primary and secondary ($L_pC_pC_s$) is proposed (Fig. 4.8) so that a better filtering is achieved with reduced volume of the filter.

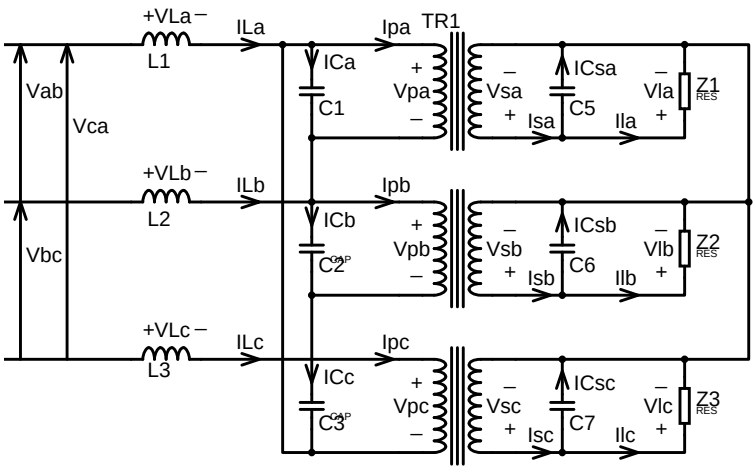

Figure 4.8: VSI with L in transformer primary and C distributed in both sides of transformer ($L_pC_pC_s$)

4.4.1 Transfer function and performance indices

Analysing the topology [see Appendix D], the indices will be

$$n_{Ll}(j\omega) = \sqrt{3}\left(n + j\omega R_l(\frac{C_p}{n} + nC_s)\right)e^{j\frac{p\pi}{6}}$$

[for both abc ($p = +1$) and acb ($p = -1$) phase sequences]

$$n_{Cpl}(j\omega) = 1/n$$

$$n_{Csl}(j\omega) = 1$$

$$G_{LP}(j\omega) = \frac{\frac{n}{3L_p(C_p+n^2C_s)}}{\left(-\omega^2 + j\frac{n^2}{R_l(C_p+n^2C_s)}\omega + \frac{1}{3L_p(C_p+n^2C_s)}\right)} \tag{4.5}$$

which gives

$$\begin{aligned} \omega_n &= \frac{1}{\sqrt{3L_p(C_p + n^2C_s)}} \\ \zeta &= \frac{\sqrt{3}n^2}{2R_l}\sqrt{\frac{L_p}{(C_p + n^2C_s)}} \\ k &= n \end{aligned} \tag{4.6}$$

Choosing the same sets of C_p and C_s and considering a 10:1 transformer, the current rating of the inductor normalized to the load current for various values of C_p and C_s is shown in Fig. 4.9. In the figure, n_{Ll} is plotted vs C_p for different values of C_s. It is thus obvious that for a given secondary capacitance, the increase in primary capacitance does not appreciably affect the inductor current rating. But due to the higher cost of the secondary capacitor with a high voltage rating, its value cannot be arbitrarily increased.

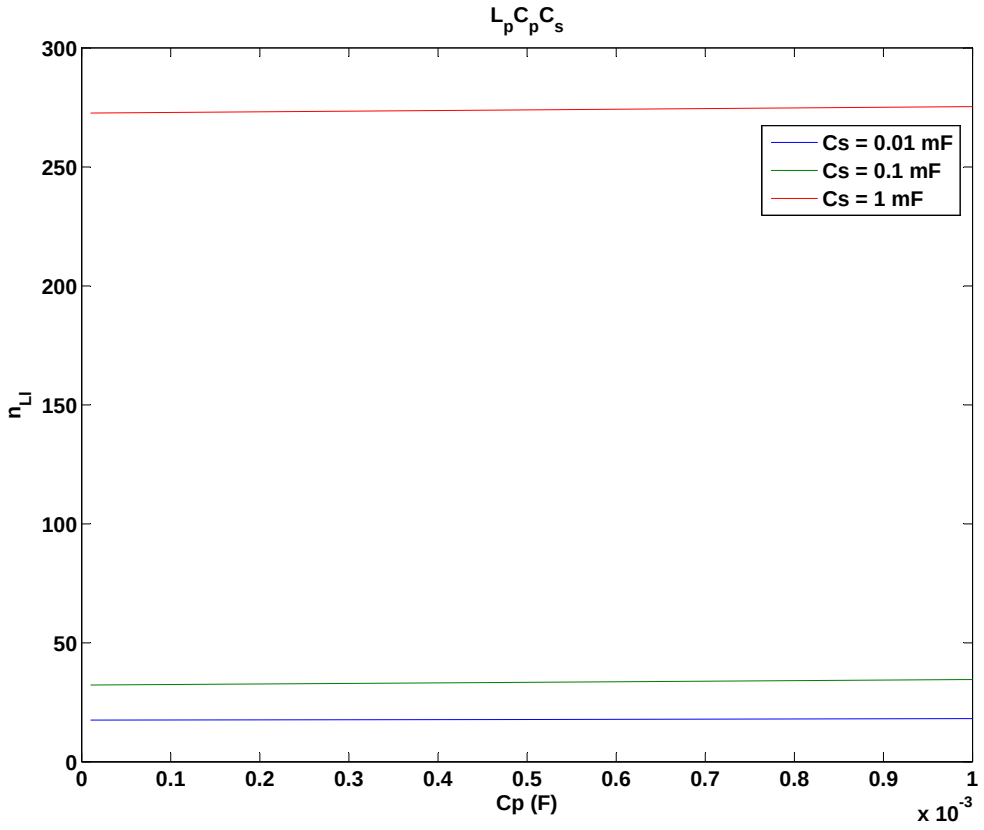

Figure 4.9: n_{Ll} vs C_p for different C_s for a 10:1 IT in $L_pC_pC_s$ configuration

Thus the primary capacitor, with a voltage rating one-tenth as compared to the secondary capacitor, may be very well used to fine tune the requirement of the cut-off frequency without a significant change of the inductor current rating.

4.4.2 Defining energy function based performance indices

At this stage, an additional performance index is defined for the inductor based on the stored energy requirement of the filter devices. Thus

defining

$$e_{Ll} = L_p n_{Ll}^2(j\omega) \text{ or } L_s n_{Ll}^2(j\omega) \text{ depending on whether the inductor is placed in the primary or secondary side} \quad (4.7)$$

it may be inferred that the figure will reflect both the inductance as well as the current it will be carrying and thus the higher the value of the product (e_{Ll}), the higher will be the cost of the inductor. This is obvious as the more is the energy stored, the greater will be the required volume of the filter and thus greater will be its cost.

Considering the same cut-off frequency and a constant turns-ratio, the plot of the energy function for various values of the filter capacitors is shown in Fig. 4.10 from which it may be concluded that if $10\ \mu F < C_s < 100\ \mu F$, the energy function is lowest in the case of $L_p C_p C_s$.

4.4.3 Implementation of the model

From Fig. 4.9 it is seen that the lowest n_{Ll} corresponds to $C_s = 10\ \mu F$ range i.e., the lowest of the range that was considered and Fig. 4.10 dictates $10\ \mu F < C_s < 100\ \mu F$ for lower energy function for the inductor. Additionally, the plot shows that if C_s is in the $10\mu F$ range, e_{Ll} is a decreasing function of C_p.

Considering these, the model was implemented with $C_s = 14.7\ \mu F$ (corresponding to a still lower value of e_{Ll} than $10\ \mu F$) and $C_p = 360.0\ \mu F$. With the conditions previously stated, the inductor value comes as $L_p = 73.82\ \mu H$. The implemented inductance had a final value of $80.0\ \mu H$. The designed trans-

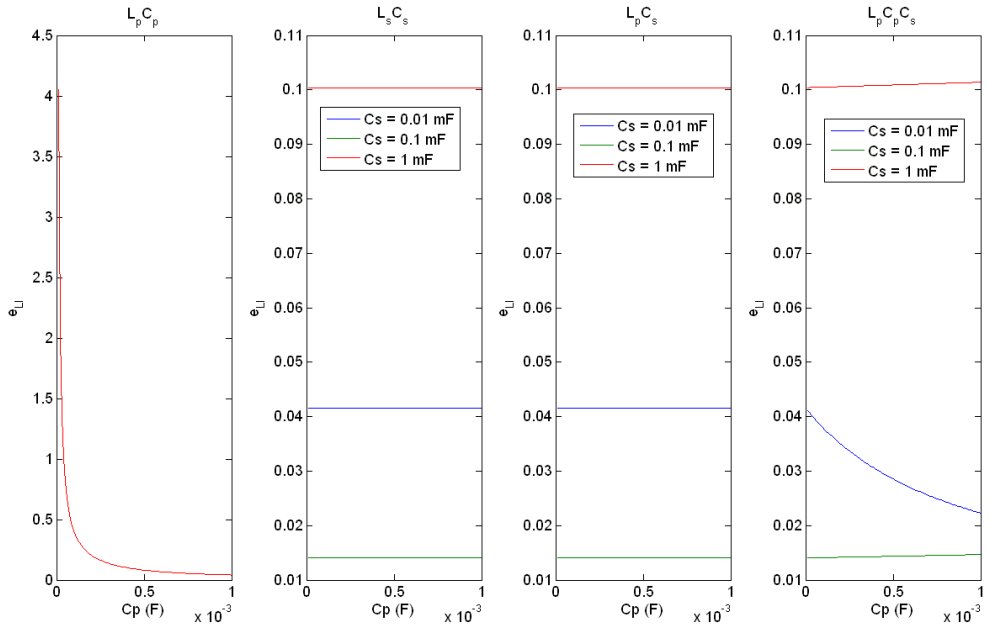

Figure 4.10: e_{Ll} vs C_p with different C_s for various filter configurations

former too deviated from the design condition and the final turns-ratio was measured as 11.53. The Bode plot of the implemented filter is shown in Fig. 4.11 which shows an attenuation at 5 kHz with respect to 50 Hz is coming as

$$\begin{aligned} \text{attenuation, } \Delta M &= \text{ dB at 50 Hz} - \text{ dB at 5 kHz} \\ &\sim 21.5\,dB - (-33.6)\,dB \\ &= 55.1\,dB \end{aligned} \tag{4.8}$$

From eq. (4.6), we get the cut-off frequency of the filter as 213.56 Hz.

The screenshot of the load voltages, the gate drive and their frequency spectrum, as obtained from the storage oscilloscope are shown in Fig. 4.12-4.14. The same may be compared with Fig. 4.15 that shows the plots of the recorded data and the calculated power spectrum as plotted in Fig. 4.16.

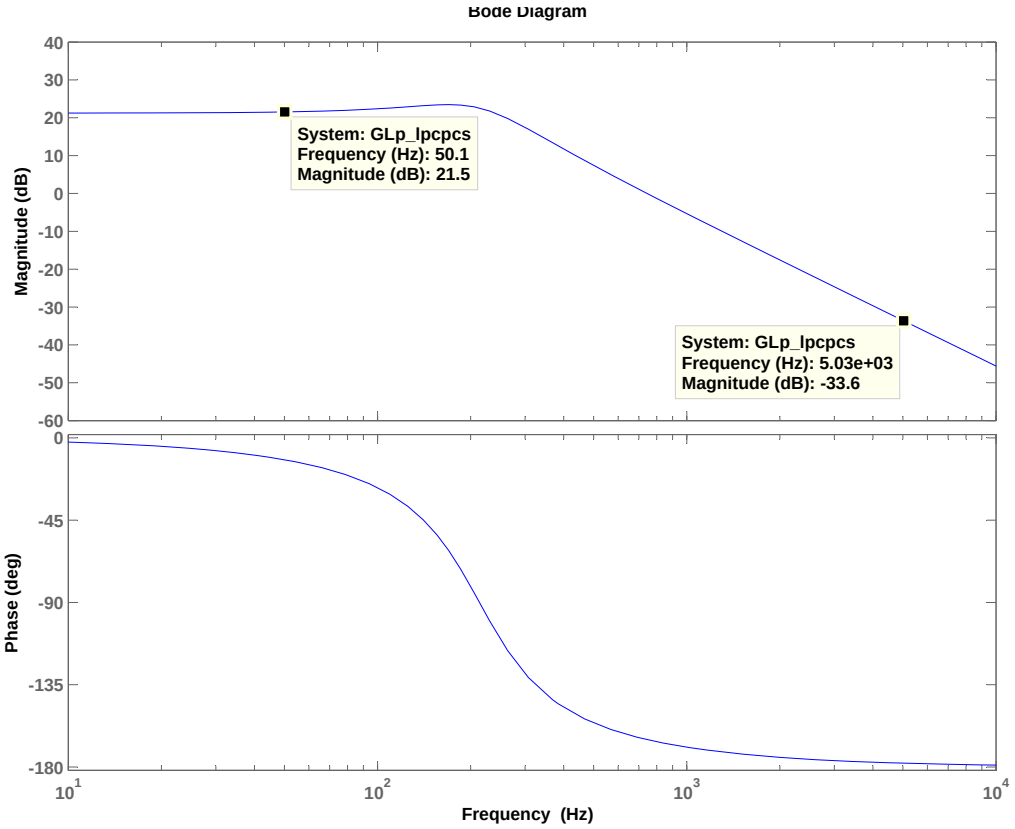

Figure 4.11: Bode plot for the implemented $L_pC_pC_s$

4.4.4 Discussions

From the analysis and the results it is seen that

1. With the utilization of the new topology, targeted to reduce the ratings of the filter components, the filtering itself was not compromised and the attenuation at the switching frequency with respect to the system frequency is $\sim 110\ dB - 50\ dB = 60\ dB$ that matches the design [see eq. (4.8)] and is slightly better than that. This also justifies the choice of the cut-off frequency. Thus without the use of a higher order filter, the attenuation offered had been sufficient. Since the filtering is inde-

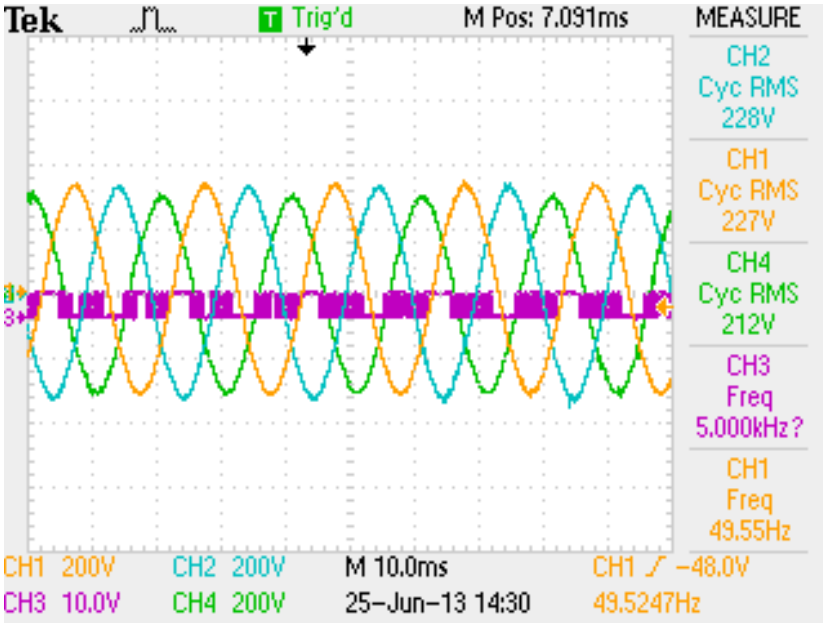

Figure 4.12: Oscilloscope screenshot of the $3-\phi$ load voltages along with one of the switching sequences

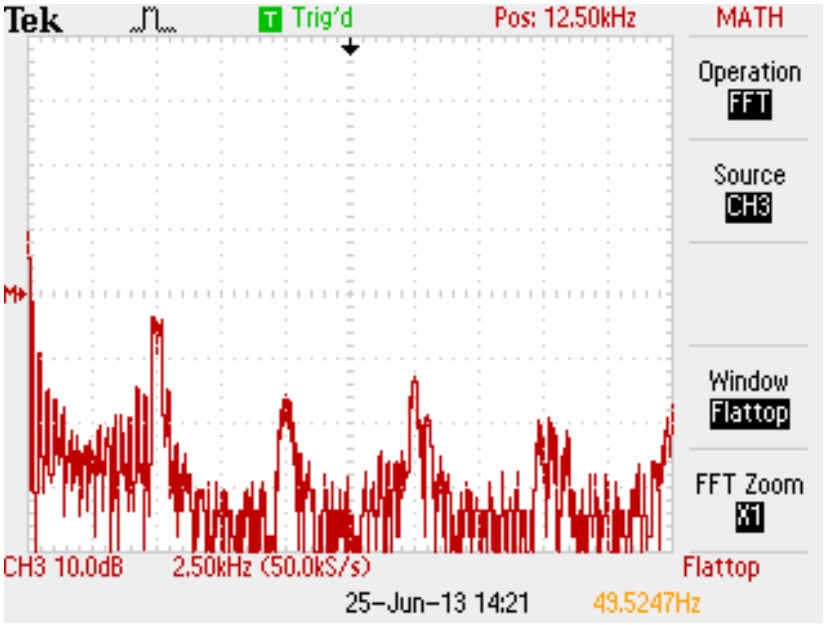

Figure 4.13: Oscilloscope screenshot of the frequency spectrum of the PWM gate drive

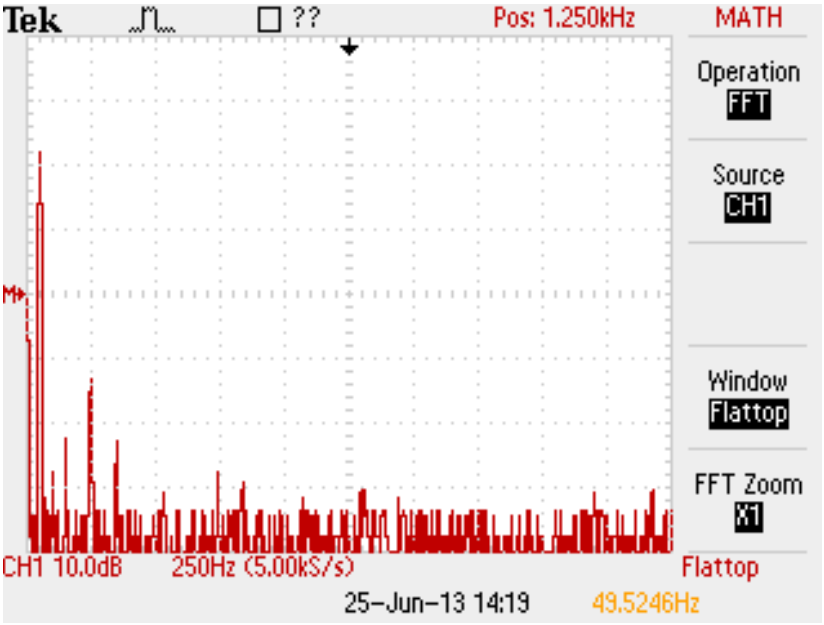

Figure 4.14: Oscilloscope screensshot of the frequency spectrum of one of the load phase voltages with the $L_pC_pC_s$ topology

pendent of the mode of operation, the VSI is also likely to offer the same attenuation during sag mitigation if utilized in DVR mode.

2. Due to the inherent stability of a second order filter system, there is no extra control system requirement as required for a filter system of order three or more.

3. An automatic spin-off for using a step-up transformer is its effect in reducing the rating of the DC bus voltage at the input of the VSI. This allows lesser insulation at the bus and the capacitor, and reduces the voltage rating of the corresponding power electronic switches which may be favourable from their operational point of view.

4. The system was applied in the DVR assembly and there too the per-

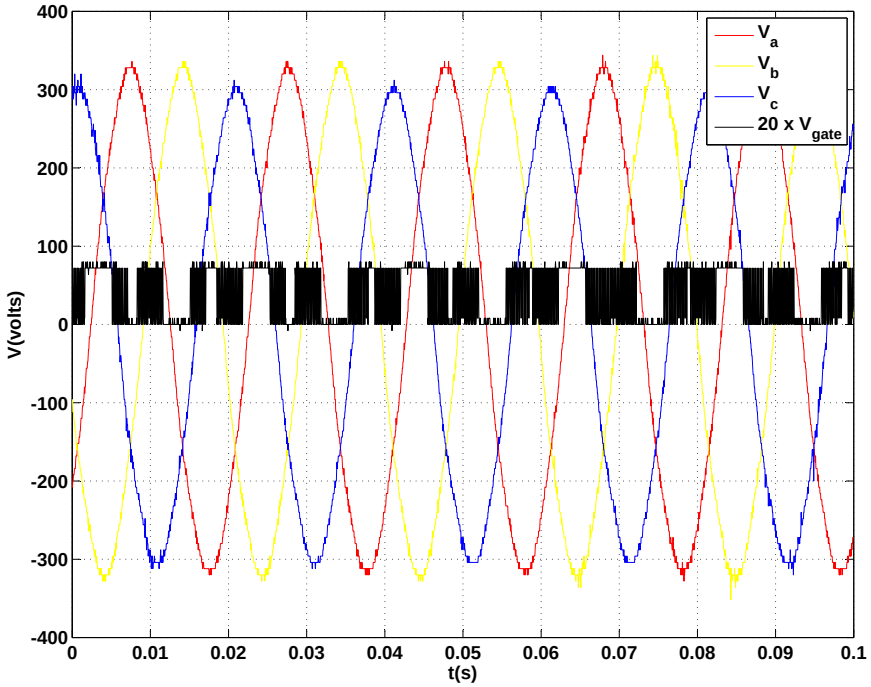

Figure 4.15: Readings of the $3-\phi$ load voltages along with one of the switching sequences (amplified 20 times), plotted from oscilloscope data

formance was according to the requirement as will be detailed in the subsequent chapter.

4.4.5 Features

A significant point to observe here is the voltage rating of the secondary capacitor which is equal to the load voltage (240 V AC in this case) while that of the primary will be roughly 11 (415/36) times less than that. This makes the design practical as regards availability of components, their volume and cost. If capacitors were deployed in a single side of the IT, it would require either more numbers of primary capacitors (making the design voluminous) or the requirement of a higher value of the secondary capacitors that are scarce

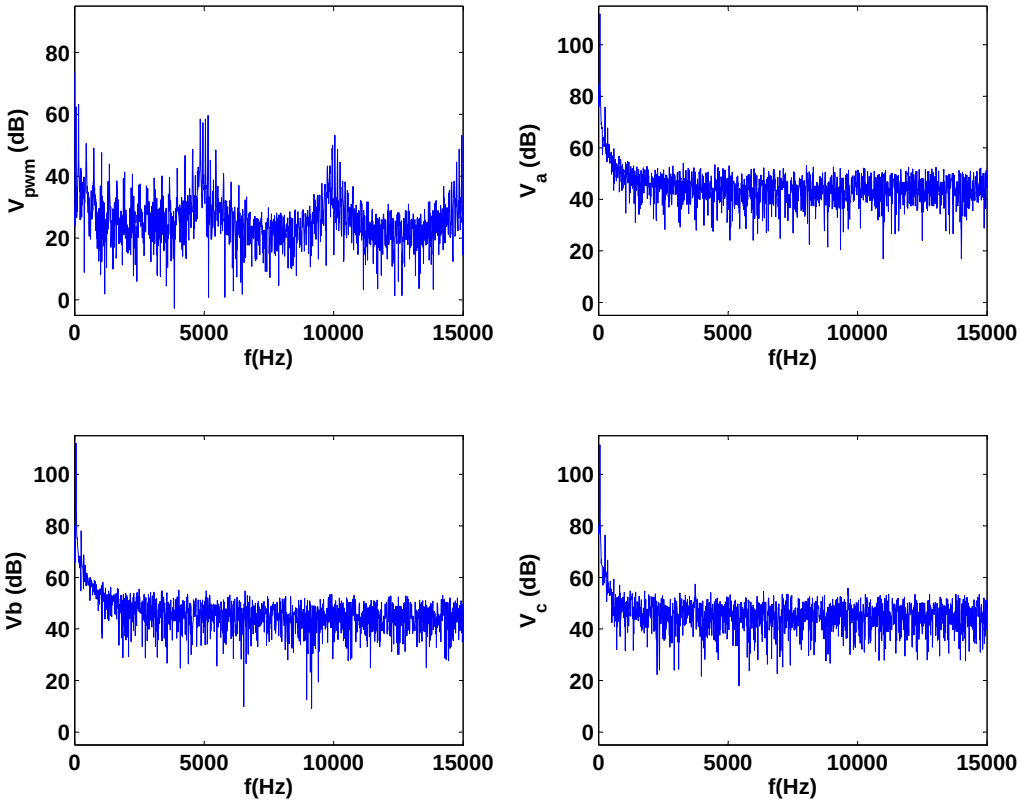

Figure 4.16: (a), (b), (c), Power spectrum of the $3-\phi$ output waveforms and (d) the PWM gate drive (top left) with the $L_pC_pC_s$ topology computed from the time series data recorded in oscilloscope

and costly in market. Also, by considering the effects of other parameters in the inductor current, the core size and the conductor diameter can be easily estimated over a wide range of values for the filter capacitor(s) and the IT ratio.

The chapter decouples a 3-ϕ system for analysis to 3 single phase systems and explores the low pass filtering techniques that may be applied to extract the power frequency output at the load. In this regard, the basic topologies for low pass filter systems have been discussed. Taking advantage of the electrical

property of the step-up transformer viz., the voltage and impedance amplifications, the design for the filter was improvised. This method is particularly relevant in cases where the space constraint of ferrite core inductors and unavailability of high capacitor values call for compromising in the attenuation of the filter or makes the design more voluminous. The inherent stability of a second-order system justifies no requirement of extra control system due to the inclusion of the filter. In the process, the attenuation of more than 40 dB has been achieved at the switching frequency. The implemented system further corroborates the design values. Though targeted for a specific load, it was tried to keep the formulations generalized so as to allow further evolution of the design in future.

Chapter 5

Utilization of the SPLL and LPF scheme

5.1 Scheme of the SMES based DVR

The novel LPF scheme has been utilized in the VSI stage of the SMES based DVR for testing its applicability in voltage sag mitigation. The SPLL code has been employed for locking the input phase and computing voltage sag. The three major subsystems of the DVR had been schematically presented in Fig. 2.11 which is again reproduced here in Fig. 5.1. It shows the distributed LC filter system and the breakers introduced with the Injection Transformer (IT). The DVR consists of

1. Superconducting magnet
2. 2-Quadrant DC-DC chopper
3. Digital controlled VSI with IT

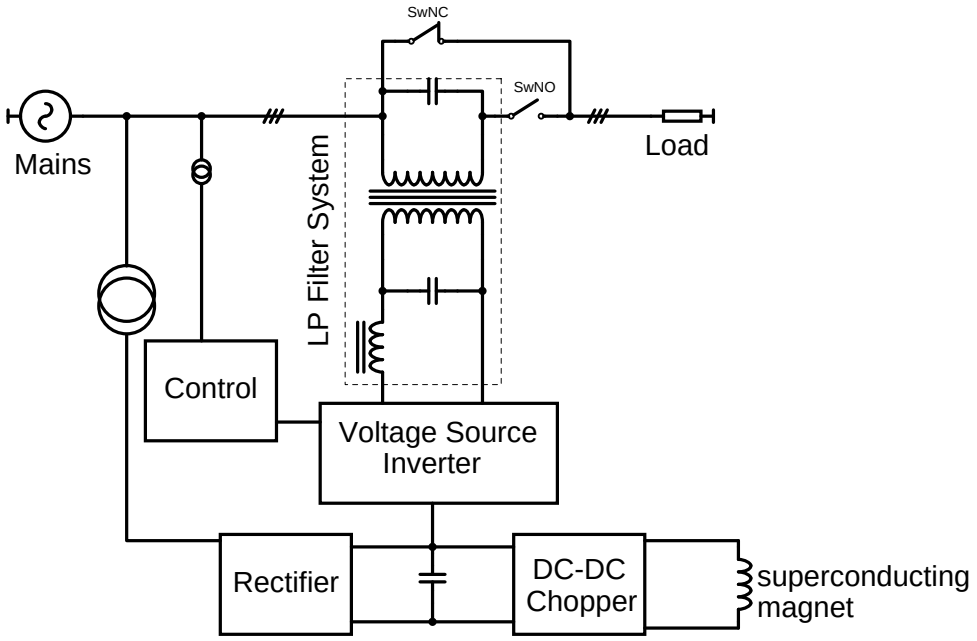

Figure 5.1: The scheme of the DVR based SMES system

A brief description of each of the subsystems follows.

5.1.1 Superconducting magnet

A solenoid type cryostable pool-boiling helium-cooled coil (Fig. 5.2) was designed with passive shielding arrangement. The coil parameters have been optimized in order to maximize the stored energy considering the constraints like coil outer diameter (OD) to contain inside existing magnetic dewar, the maximum current limit, hoop stress at inside layer (in median plane), etc. for a given length and type of conductor. A critical current margin of 30% has been kept corresponding to a temperature margin of 0.7 K for the coil operating at maximum field level upto 7 T. The margin allows flexibility of operating temperature from 4.2 K to 4.4 K, ensures superconducting oper-

Parameters	**values**
Material	NbTi/Cu
Conductor dimension	2.97 mm x 4.79 mm
No. of strands	1
Strand diameter	1.29 mm
No. of filaments	500
Filament diameter	40 μm
Overall Cu to superconductor ratio	20
Critical current at 5.5 T	1080 A

Table 5.1: Specifications of the superconductor

Parameters	**values**
Coil type	solenoid
Maximum operating current	800 A
Inductance	1.87 H
Maximum stored energy	0.6 MJ
Peak coil field	6.6 T
Coil dimension	790 mm (H)/132.5 mm (ID)/416 mm (OD)
Winding	36 layers x 154 turns/layer
Cable length	5 km

Table 5.2: Specifications of the superconducting coil

ation of the magnet when fully charged and any other small disturbances that might occur in the coil. A mylar tape of dimension 100 μm (thick) and 3 mm (width) has been used for insulation between turns. The gap between consecutive layers has been maintained with glass epoxy spacer of 1 mm thickness. This serves as a cooling channel as well as provides insulation between layers. Detailed parameters [82] are listed in Tables 5.1 and 5.2.

5.1.2 2-quadrant DC-DC chopper

A high current IGBT based DC-DC chopper (Fig. 5.3) has been designed and developed that dynamically configured itself to charge and discharge the coil according to the sag/no-sag signal as available from the VSI

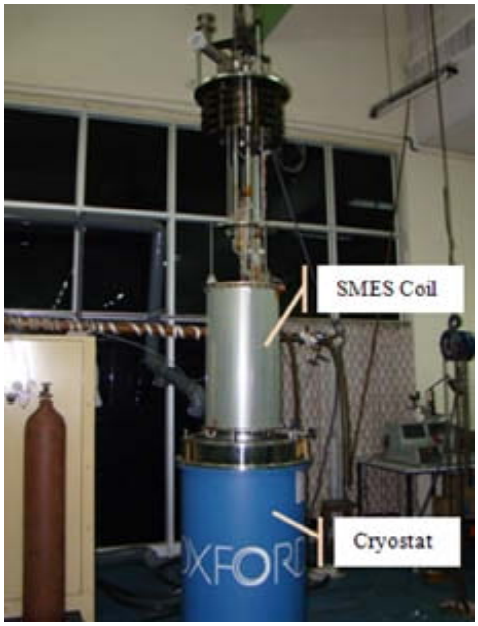

Figure 5.2: The SMES coil and its cryostat

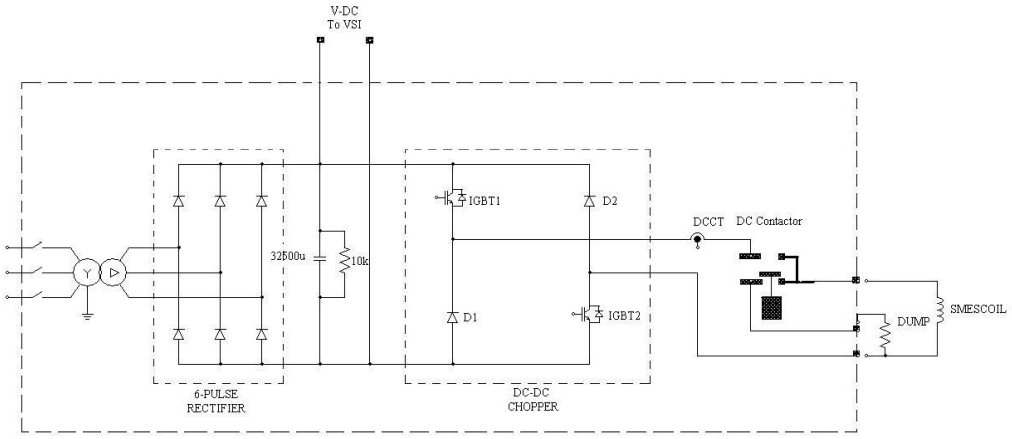

Figure 5.3: Schematic of the DC-DC chopper

that monitors the utility mains. A hysteresis band controller scheme has been adopted for the chopper to perform in the two quadrants according to the sys-

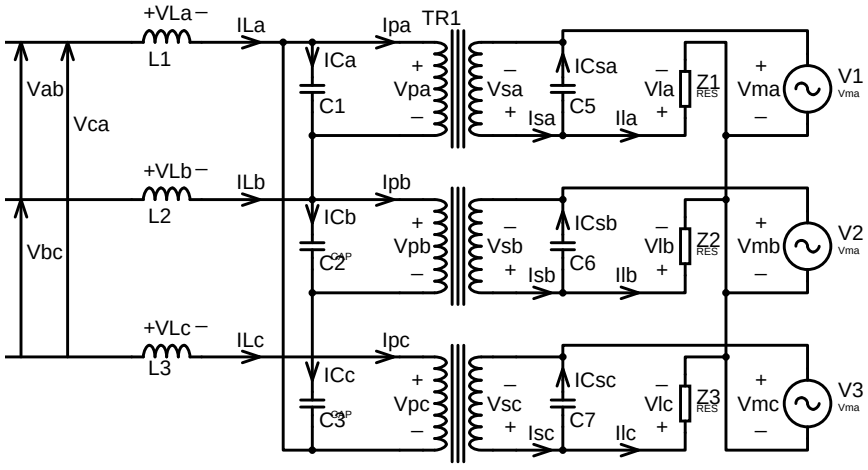

Figure 5.4: The power scheme of the DVR from the VSI perspective

tem demand. During normal mains, the chopper charged the coil to its steady state value within its tolerable limit and during a sag condition, it boosted the voltage across the capacitor, keeping it constant for the VSI, sourcing power from the stored energy in the coil.

It may be pointed out that the apparatus is aimed for utilities subjected to voltage sag only. So the rectifier system is only a diode rectifier in the present case. In case of applications demanding voltage swell compensation, a major change in the topology will include replacement of the diode rectifier by a controlled (active) rectifier system as the swell mitigation will result in dumping a good amount of active power across the DC bus.

5.1.3 The VSI based system

The VSI is utilized at the output stage of the SMES based DVR system. Its power scheme is a slight variation of Fig. 4.8 with the IT secondary connected in series between mains and load. The load and the VSI ratings and

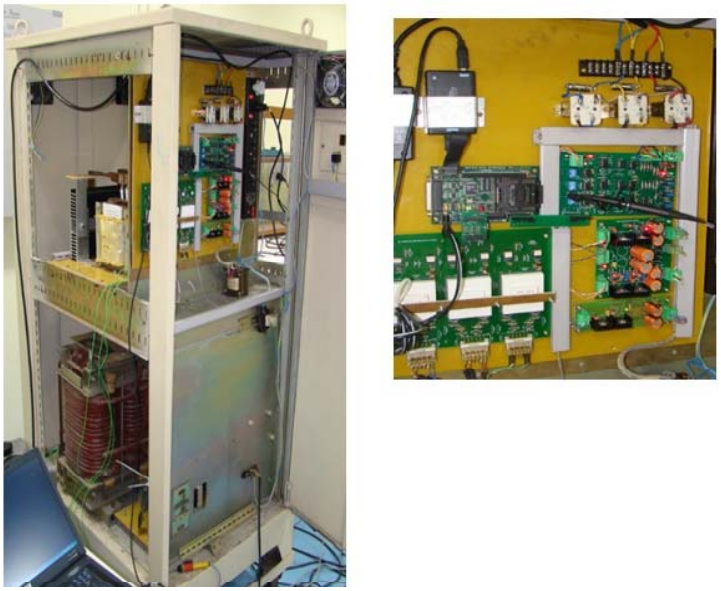

Figure 5.5: (a) VSI during assembly with the control PCBs and the power components, (b) the control PCBs zoomed

its components are the same as discussed in previous chapter. A simplified schematic diagram (with the breakers omitted) is shown in Fig. 5.4 and Fig. 5.5 shows the implemented hardware during the assembly. The switching voltages are filtered out at the LPF stage and added in series, via the secondary of the 3-ϕ Δ/open IT, with the mains voltage (V_m) to keep the load voltage (V_l) constant. The inverter voltage requirement at phase lock for a sag of depth k_{sag} is detailed in Appendix E and is given by

$$V_{invll} = \left[\left(1 - k_{sag}\right)\left\{\frac{1}{n} - 3\omega^2 L_p\left(\frac{C_p}{n} + nC_s\right)\right\} + j\frac{3n\omega L_p}{R_l}\right]v_{pref} \qquad (5.1)$$

The expression may be compared with (3.1) that was used while analysing the SPLL based control system. The interface system is as detailed in Fig. 3.2 and consists of a PT based low voltage electronics (LVE) that isolates, scales

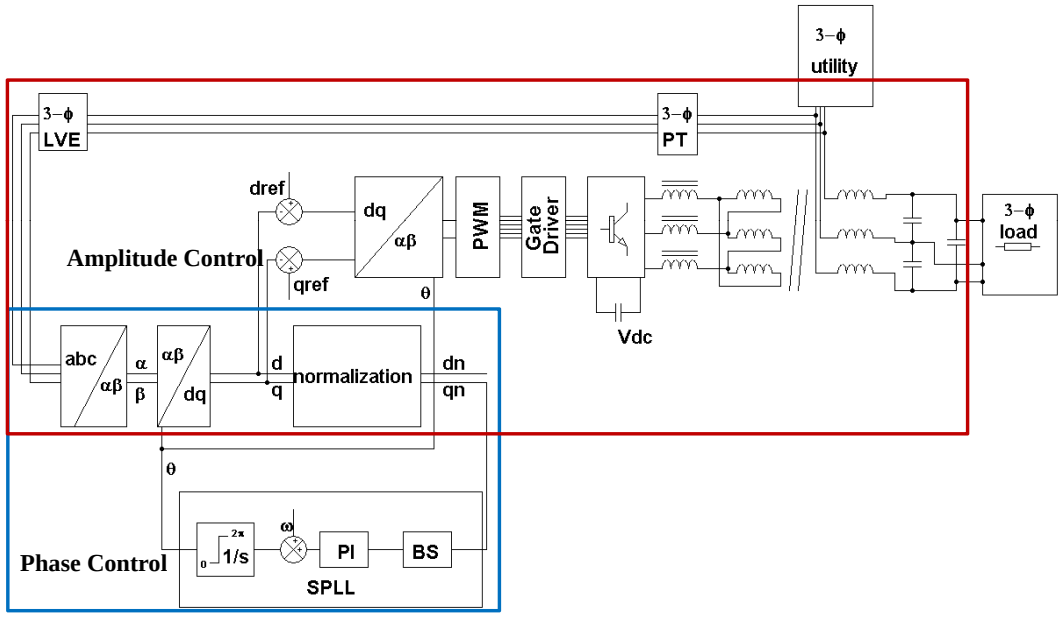

Figure 5.6: The control scheme of the VSI customized for sag mitigation

and conditions the mains voltage signals for interfacing a multi-channel ADC frontend of the DSP based controller core (Fig. 5.6). The SPLL locks the input phase and evaluates the amplitude error to generate the gate signals following SVPWM. Texas Instruments make TMS320F2812 fixed point DSP was used that features an inbuilt SVPWM state machine and a 12 bit 16 channel 12.5 MSPS ADC, alongwith other peripherals. The code utilized TI's IQ Math Library, a virtual floating point engine, to enable floating point computational precision. The SVPWM state machine was dynamically configured according to the computed sag and the phase information (as discussed in section 3.1) and the gate signals were applied to the IGBTs constituting the full bridge. The sampling frequency was selected as 5 kHz.

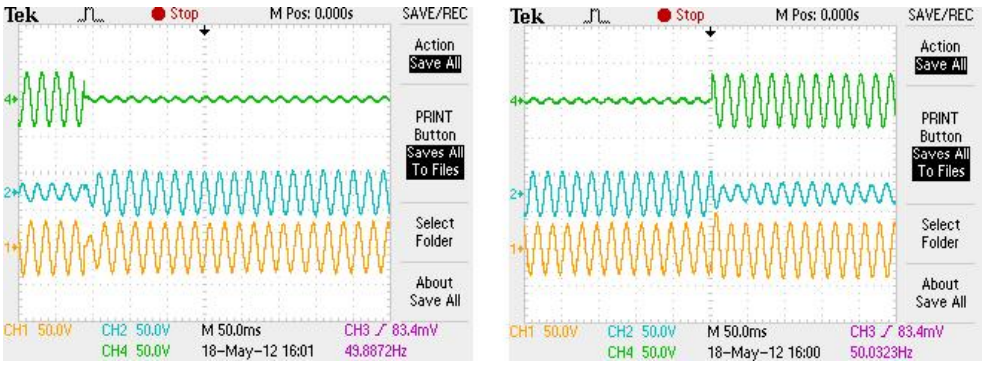

Figure 5.7: Oscilloscope screenshots of voltage sag and restoration at load (orange) by series injection (blue) for a (a): 100% to 10% step change of mains (green) followed by (b): 10% to 100% step

5.2 Testing

5.2.1 Functionality testing at reduced load

Prior to its integration to the SMES based DVR, a functional testing of the scheme was carried out for a $3-\phi$ 50 Hz, 25 V, 1 A 4-wire output. As the current was well within the short-circuit limit of the IT, the circuit breakers were removed from the system thus keeping the IT secondary continuously in series with the load. This was specfically done to understand the response from sag detection to correction. A programmable power source (California Instrument make $3-\phi$ 16-819 Hz, 45 KVA power converter) was used for simulating the utility mains. A DC power source was used as the dc bus. Sags of different depths were generated and output displayed in oscilloscope. One such screenshot is shown in Fig. 5.7 and the recorded data is plotted in Fig. 5.8. DSP registers were used for storing the digital instrumentation and control parameters. Fig. 5.9 shows an instance of phase tracking for 40 ms.

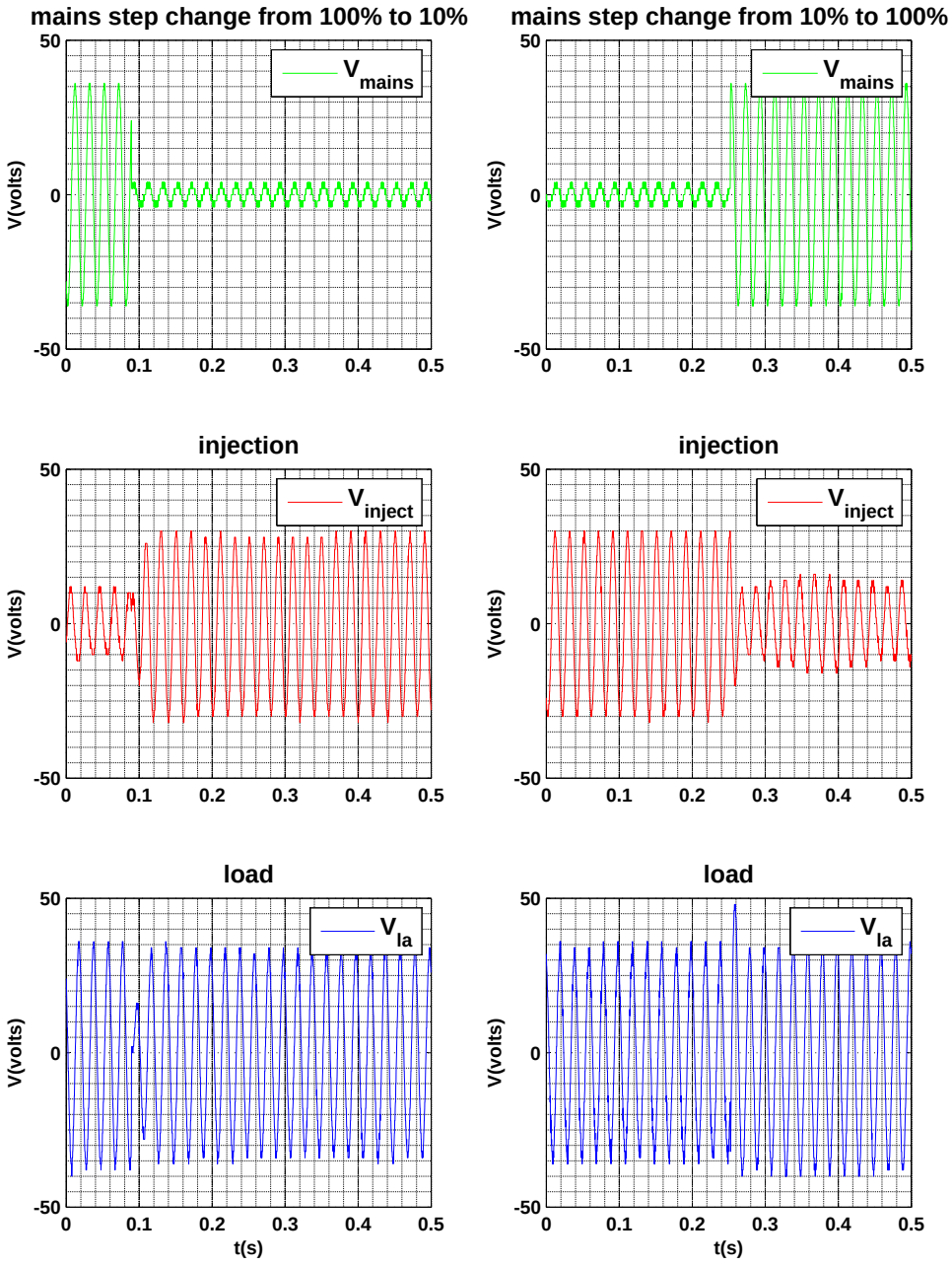

Figure 5.8: Plots showing the voltage sag and restoration at load (blue) by series injection (red) for a 100% to 10% step change of mains (green) followed by 10% to 100% step

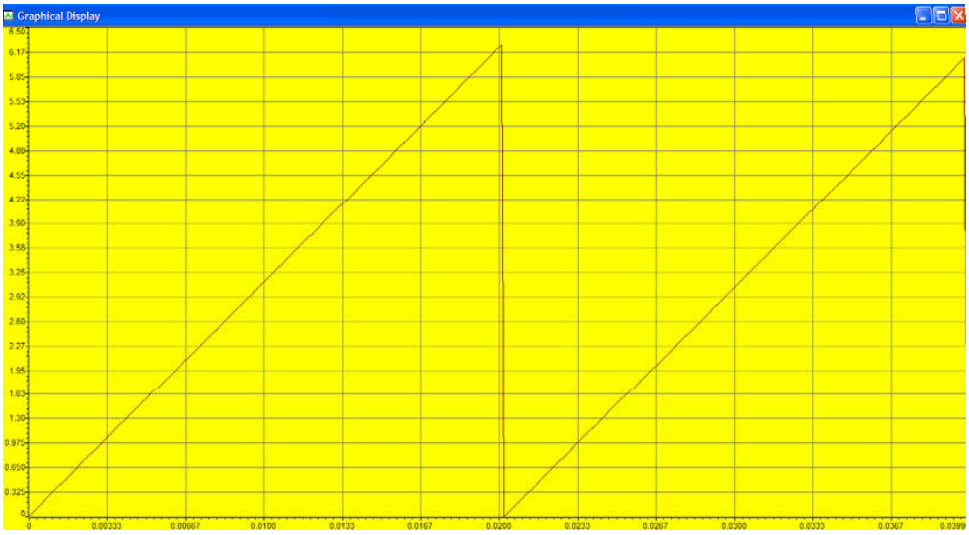

Figure 5.9: DSP register values showing phase tracking of mains voltage

The plots show phase tracking from 0 to 2π within 20 ms and sag mitigation within a cycle.

5.2.2 Testing of the integrated system

Subsequent to standalone testing of the VSI system, it was integrated to the chopper (connected to the SMES coil) and tested with the programmable source. An additional signal from the VSI control was used to initiate charge / discharge mode of the chopper-coil assembly. Again, varied sags were generated by the source and data recorded in oscilloscope and DSP registers.

Figures 5.10 - 5.12 are the screenshots of the DSP register values that demonstrate the control system functionality as regards the input bandpass filter that conditions the ADC samples, the transformed $2-\phi$ signals, the SPLL output and the normalized computed voltage amplitude.

The DSC acquires the phase voltage signals through its ADC channels and

scales them in the range of the mains voltage. These are then filtered by the bandpass block to eliminate the unwanted distortions and the conditioned signals (Figures 5.11 (a), (c), (e)) are transformed to their corresponding $\alpha\beta$ components. The Fig. 5.11 (b) shows the α component in phase with the a phase (Fig. 5.11 (a)) of the mains and Fig. 5.11 (d) shows the β phase in phase quadrature. Based on these transformations, the sag magnitude as shown in Fig. 5.11 (f) is computed and stored instantaneously.

The $\alpha\beta$ components and its corresponding sag for another instant is shown in Figures 5.12 (a) - (c). The computed sag is again filtered to make its value constant (Fig. 5.12 (e)). The $\alpha\beta$ components are simultaneously fed to the SPLL block that utilizes its elements to drive the VCO (Fig. 5.12 (d)) and lock the phase (Fig. 5.12 (f)).

Fig. 5.13[1] captures two instances of voltage sag mitigation as recorded in the oscilloscope screens. The (a) and (b) plots are the VSI outputs and the (c) and (d) are the corresponding chopper outputs. It is seen that during the normal mains (pink in (a) and (b)) the VSI maintains the SMES coil current (blue in (c) and (d)) within its hysteresis band. Once there is a sag, as sensed by the VSI, it signals the chopper to configure itself to the discharge mode and boosts the voltage (pink in (c) and (d)) across the DC bus capacitor. The VSI, simultaneously, generates the gate signals (one of the six gate signals, magnified 20x, is shown in green in (a) and (b)) to the inverter bridge and the

[1]It may be observed in Fig. 5.13 (a) and (b), that part of the screen near the middle portion is blank. This is due to the relatively longer time scale of 1.0 s and the horizontal wrapping up of data once the plot reaches the rightmost extreme in the time scale. The selection of a larger time scale to display the data causes its storage buffer to completely fill up and so it erases part of the data (oldest first) and stores and plot the new data continuously from left to right.

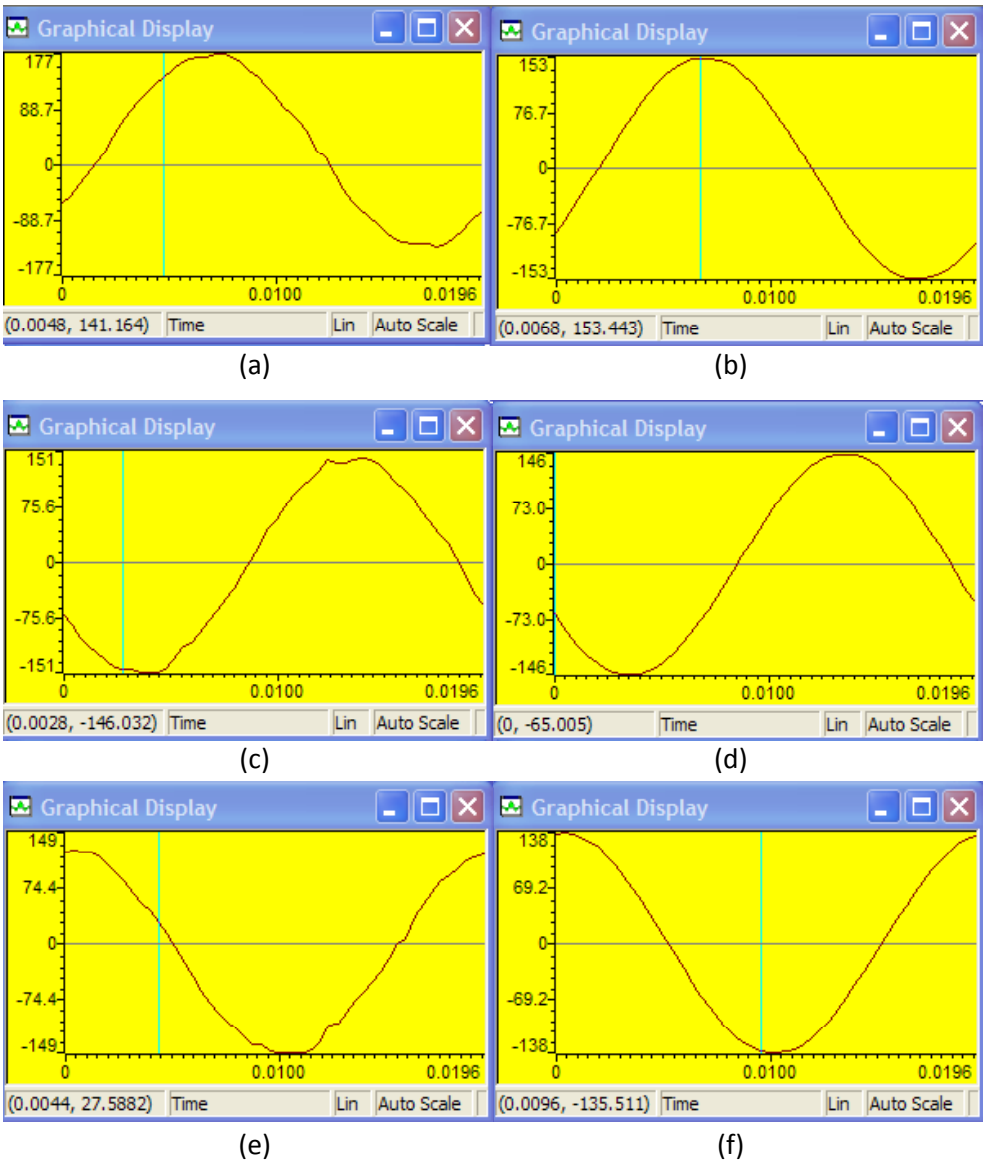

Figure 5.10: Screenshot of DSP register values showing phase signals before ((a), (c), (e)) and after bandpassed ((b), (d), (f))

resulting injection keeps the load voltage (two of the phases shown by blue and yellow in (a) and (b)) constant. In this mode, the SMES coil current droops as energy is drawn out of it. As soon as the sag vanishes, the gate signal is

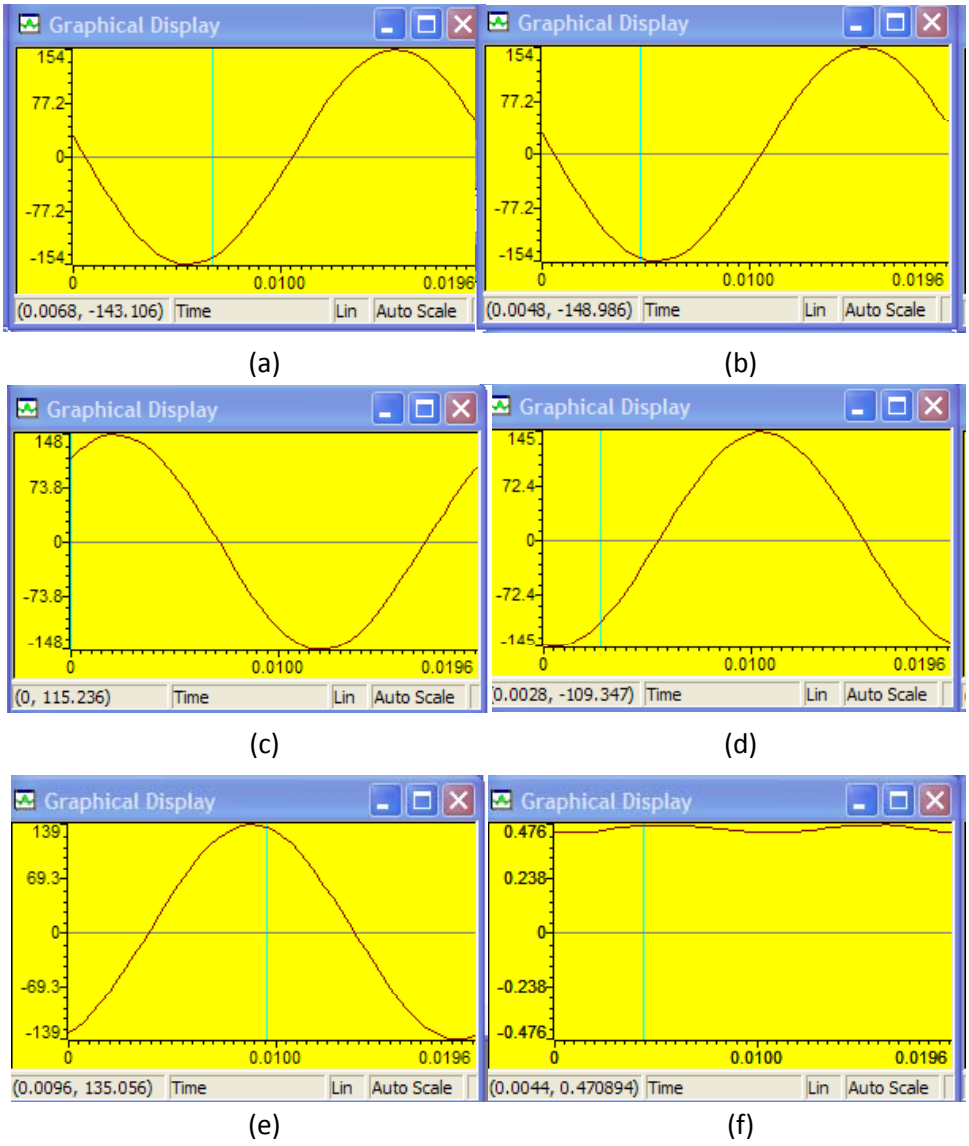

Figure 5.11: Screenshot of DSP register values showing (a), (c), (e): abc phase voltages filtered by bandpass filter, (b), (d): the corresponding $\alpha\beta$ transformed components and (f): the computed unfiltered sag signals

withdrawn and the chopper is automatically configured to its charging mode.

To observe the time response more critically, part of the recorded data of

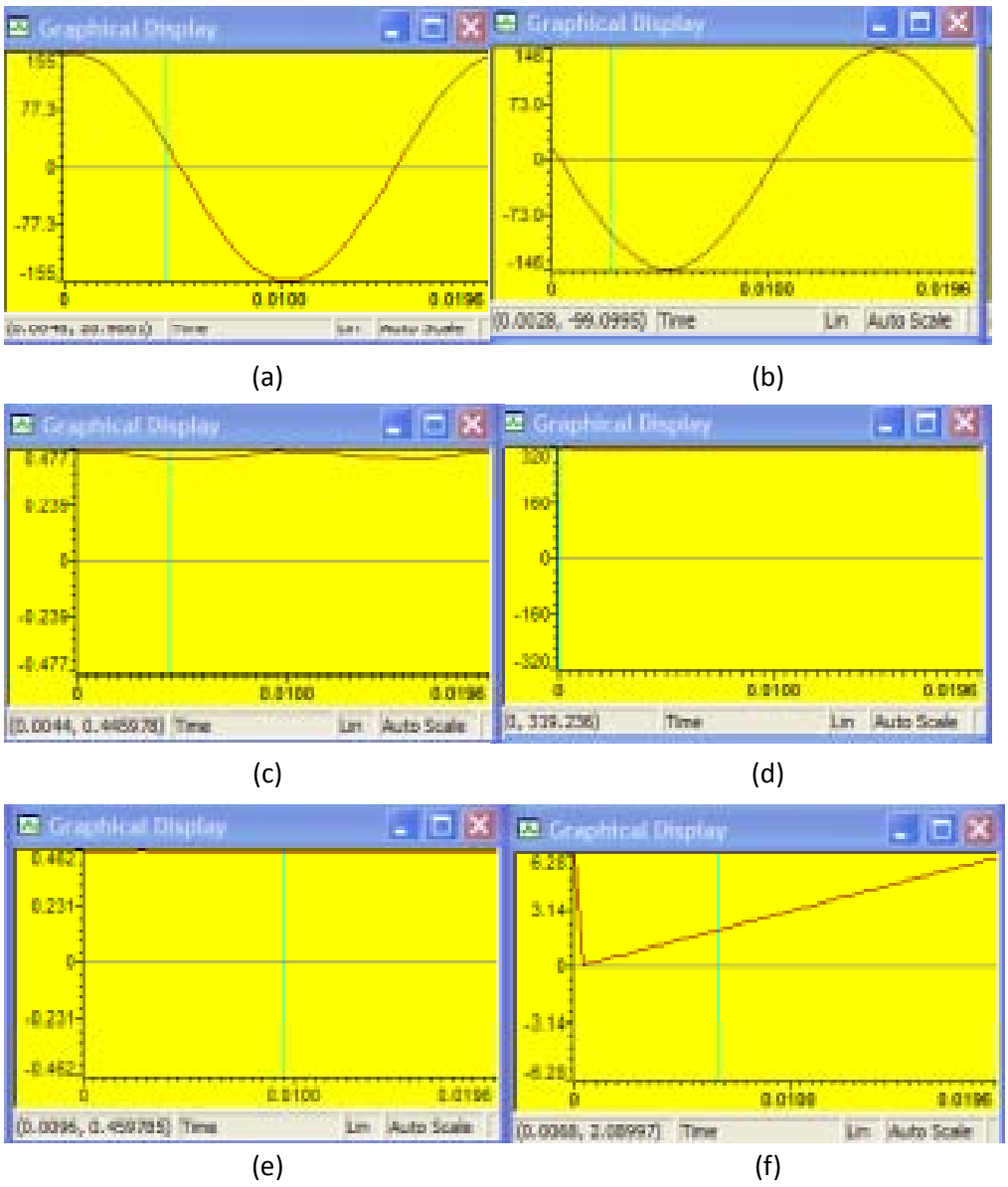

Figure 5.12: Screenshot of DSP register values showing (a), (b): $\alpha\beta$ components, (c): computed unfiltered sag, (d): VCO input, (e): corresponding filtered sag and (f): phase tracking

the VSI is plotted in Fig. 5.14 demonstrating voltage restoration by the VSI during a sag. Here it is observed that though the gate (b) is operating almost

instantaneously as the sag occurs (b) at the mains, the load (two phases are shown in (c) and (d)) takes around two cycles to be fully compensated. This is due to the delayed response of the electrical contacts that takes around two cycles to be completely closed. The response was similar when the mains voltage was restored to the normal value. Fig. 5.15 is a screenshot of the oscilloscope display of magnitude spectrum of one of the load phases at steady state during sag. It can be seen that the attenuation is $\sim 60\,dB$ as predicted in the previous section.

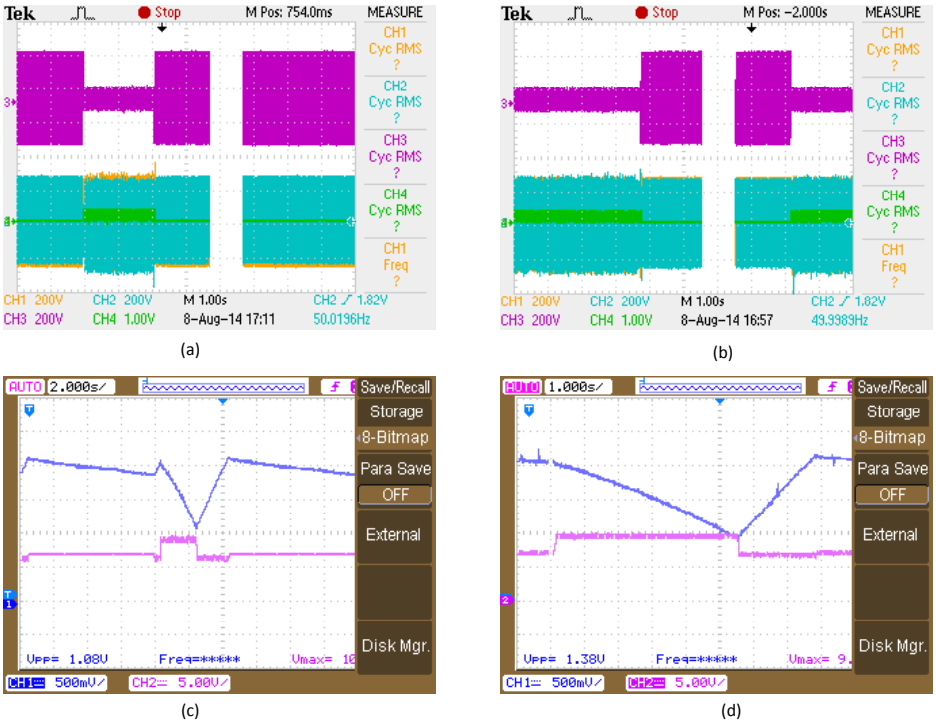

Figure 5.13: Oscilloscope screenshot of (a), (b): mains (pink), a VSI gate trigger (green) from control, two of the load phases (blue and yellow) during voltage sag, (c), (d): chopper voltage (pink) and current (blue) during sag

It may be debated here that the contact switches viz. SwNO (normally open)

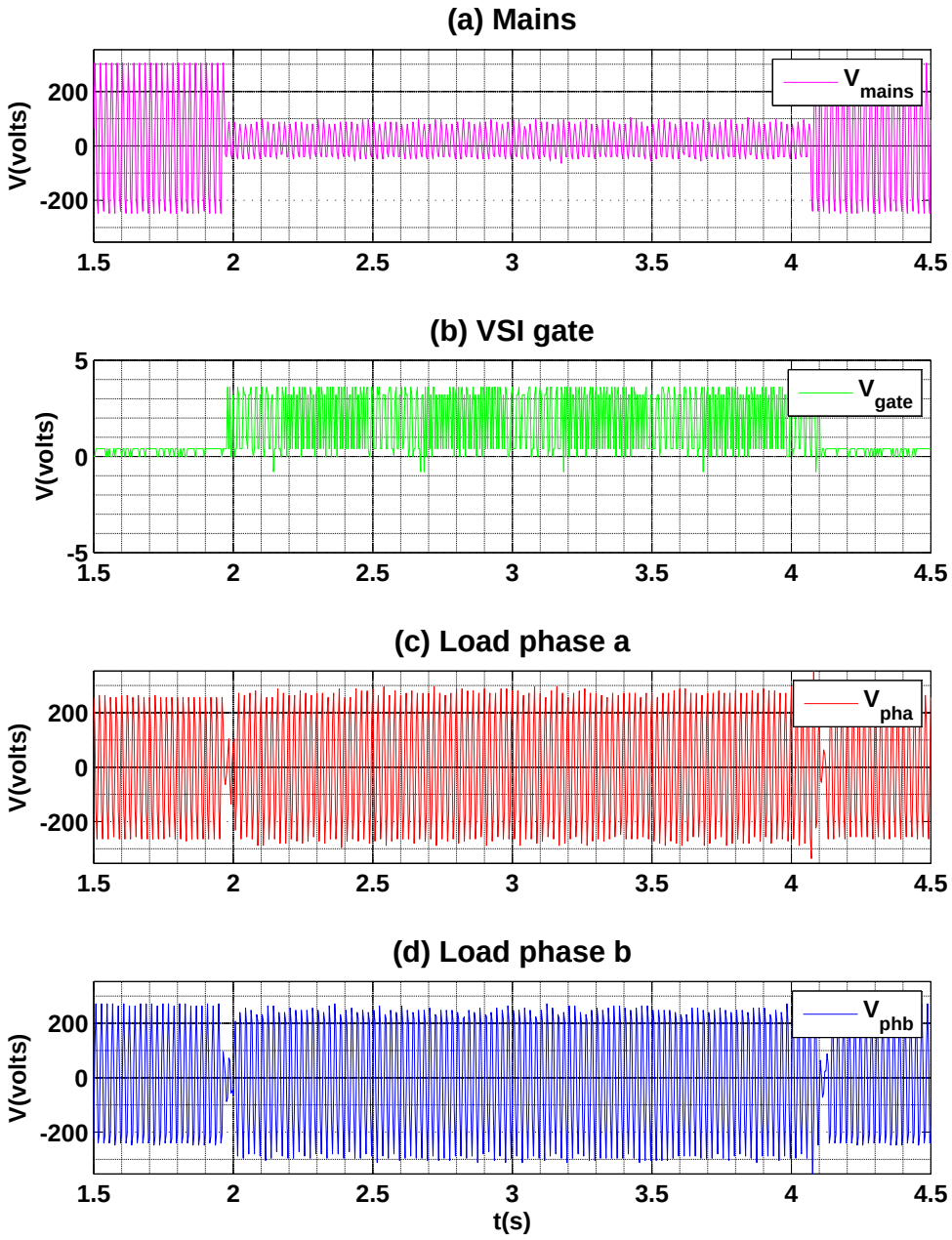

Figure 5.14: Part of the oscilloscope data plotted to show (a): the voltage at the mains, (b): the gate driver response and (c), (d): output voltages of two of the load phases

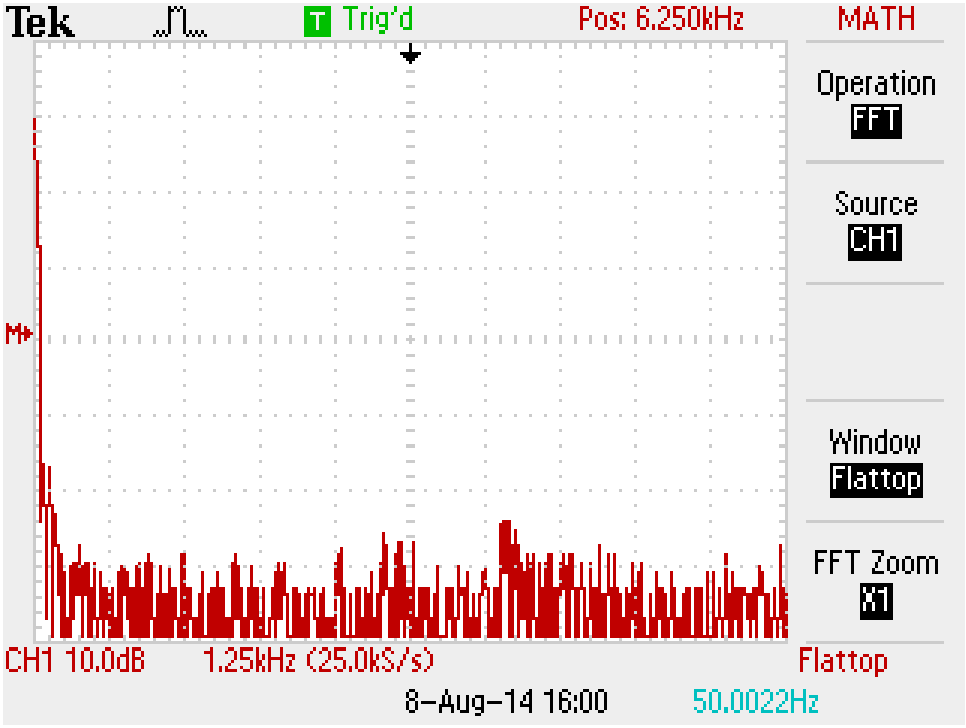

Figure 5.15: Oscilloscope screenshot of frequency spectrum of the restored load voltage during sag

and SwNC (normally close) in the Fig. 5.1 may be interchanged in order to avoid the delay so that the DVR will remain functional, continuously feeding the load and the mains may take over in case it fails. But this will have two problems. First of all, in the situation when the DVR fails and there is a voltage sag at the grid, either at the same time or during the period when the DVR is disconnected, then the basic aim of sag mitigation at load during an actual voltage sag event at the grid is not satisfied. Secondly, the VSI based DVR, as envisaged, is a voltage sag mitigation device, drawing the required energy from the SMES coil-chopper module and is not meant for continuous

operation. So the swapping of the switch positions will actually dictate a change in the functionality of the sub-systems which requires an elaborate change in its basic philosophy.

Chapter 6

Conclusion

A novel scheme of low pass filter system applied to a digital controlled VSI and utilized in SMES based DVR system to mitigate voltage sags in the utility mains is presented. A set of performance indices has been defined reflecting the quality of the filter and also the ratings of the filter components. An additional energy function based performance index for the inductor of the filter system was also put forward. It thus considered both the attenuation and the practicability of implementation of the filter system as regards the volume and availability of components. The way to utilize transformer turns-ratio advantageously was indicated in the final scheme. In the process, an attenuation of 60 dB has been achieved at the switching frequency. The design was implemented in actual hardware. Tests were carried out configuring it both as a standalone inverter and a VSI employed in DVR. The test results corroborated the design values. The design was kept generalized so that it may be applied on any VSI system. The general formulations open scope for evolution of the model by designers and developers. Detailed analysis of the

model for a balanced $3-\phi$ system was also presented that decoupled it for $1-\phi$ analysis. However, in case the load in non-linear or draws a constant power, then the leakage inductance of the transformer, neglected for the present case, will have to be considered as the added resonant modes may be excited in such a way that may not be damped by the present controller. This may be pursued in future research related to this work.

Also, methods may be devised to improve on the currently achieved response time of 2 cycles. An option might be to use series power electronic switches in the primary (inverter) side of the IT and removing the contact switches (SwNO and SwNC in Fig. 5.1) from the circuit altogether. During the condition of healthy mains, the switches will remain off and will be simultaneously switched on along with the gate pulses whenever a sag is detected. Being faster than the electrical contactors, the system will definitely improve on the response time and may be used if the case of instantaneous sag is considered which allows a maximum of 0.5 cycles only to mitigate voltage sags.

A digital control system was designed for the VSI that utilized an SPLL for phase locking and sag detection. The origin of the PLL system was discussed and its linearization explained. The need of a prefilter to condition the signal for eliminating unwanted frequencies and the requirement for the controller loop filter to eliminate double frequency component were indicated. The SPLL was designed to incorporate a bandpass prefilter for allowing only the preferred frequency in the system. The loop filter employed a bandstop filter cascaded to a PI controller to selectively eliminate the inherent high frequency component and the steady-state error simultaneously. So in effect it made provisions for a practically implementable PLL system. The analog design was translated to its

bilinear transformed discrete equivalent and stability was checked theoretically. Difference equations were derived from the discrete model. A fixed point DSP based controller was used to implement the code for the SPLL with all its components. It was utilized for online phase locking, sag computations and SVPWM based switching generator for the VSI bridge besides handshaking signals between the subsystems of the integrated DVR. The VSI was configured for SMES based DVR for a $3-\phi$ 240 V, 50 Hz, 3.45 kW load for voltage sag mitigation according to IEEE 1159-1995. Voltage sags of varying depths were mitigated for 40 ms to 6 sec with phase locking. This demonstrated the system's performance for satisfactory phase locking and voltage compensations for momentary sags and partly for instantaneous and temporary sags.

Here, it may be observed that the present scheme had assumed the condition of balanced phase voltages. The case of unbalanced voltage sag detection with mitigation may also be considered in future. One of the options in this regard might be to use three single phase VSI systems for separate control of each of the phases. This and other methods may be explored in future.

Appendix A

Clarke Transformation

The peak invariant Clarke transformation (T_{3s2s}) from a $3-\phi$ system to a $2-\phi$ system is given by

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = T_{3s2s} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{A.1}$$

A.1 Illustration

If

$$V_{3s} = V_m \begin{bmatrix} \cos\omega t \\ \cos(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t - \frac{2\pi}{3}) \end{bmatrix} \tag{A.2}$$

the Clarke transformed amplitude invariant $2-\phi$ system will be

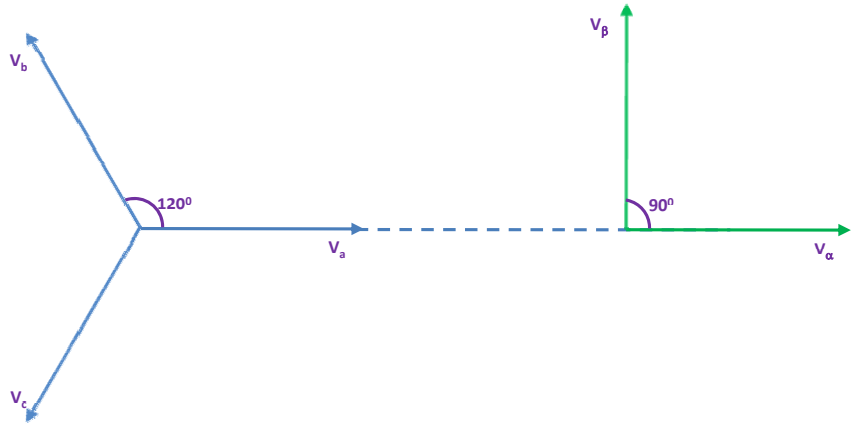

Figure A.1: Clarke transformation

$$
\begin{aligned}
V_{2s} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} V_{3s} \\
&= \frac{2}{3} V_m \begin{bmatrix} \frac{3}{2}\cos\omega t \\ -2\frac{\sqrt{3}}{2}\sin\omega t \sin\frac{2\pi}{3} \end{bmatrix} \\
&= V_m \begin{bmatrix} \cos\omega t \\ -\sin\omega t \end{bmatrix} \\
&= V_m \begin{bmatrix} \cos\omega t \\ \cos(\omega t + \frac{\pi}{2}) \end{bmatrix}
\end{aligned} \tag{A.3}
$$

Thus as shown in Fig. A.1, the transformed vector in the $\alpha - axis$ will be aligned with the $a - axis$ of the abc system while the $\beta - axis$ will lead it by $\frac{\pi}{2}$. As the amplitude of the transformed vectors remain the same, it justifies the naming of the transformation matrix.

Appendix B

Park Transformation

The transformation from a $3-\phi$ system to a rotating $2-\phi$ system is called Park transformation and is given by

$$\begin{aligned}
\begin{bmatrix} V_d \\ V_q \end{bmatrix} &= \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \\
&= \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \\
&= \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta+\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta+\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \\
&= T_{3s2r}(\theta) \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}
\end{aligned} \tag{B.1}$$

B.1 Illustration

When applied to a balanced $3-\phi$ system, the resultant rotating system will be

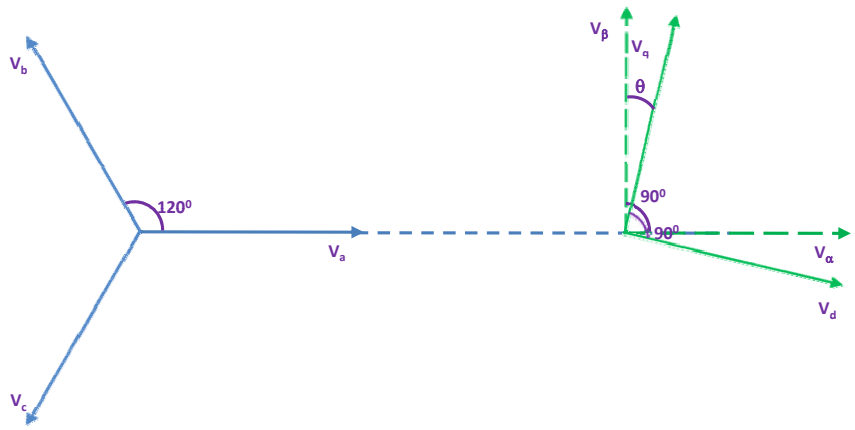

Figure B.1: Park transformation

$$V_{2r} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta+\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) \\ \sin\theta & \sin(\theta+\frac{2\pi}{3}) & \sin(\theta-\frac{2\pi}{3}) \end{bmatrix} V_m \begin{bmatrix} \cos\omega t \\ \cos(\omega t+\frac{2\pi}{3}) \\ \cos(\omega t-\frac{2\pi}{3}) \end{bmatrix}$$

$$= \frac{1}{3}V_m \begin{bmatrix} 3\cos(\theta-\omega t) \\ 3\sin(\theta-\omega t) \end{bmatrix}$$

$$= V_m \begin{bmatrix} \cos(\theta-\omega t) \\ \sin(\theta-\omega t) \end{bmatrix}$$

$$= V_m \begin{bmatrix} \cos(\omega t - \theta) \\ \cos(\omega t - \theta + \frac{\pi}{2}) \end{bmatrix} \tag{B.2}$$

As shown in Fig. B.1, the transformed vector set, being orthogonal to each other lags the corresponding Clarke Transform (shown in dotted green lines) by θ.

Appendix C

Space Vector Pulse Width Modulation (SVPWM)

An application of SVPWM for estimating the switching time[48] for a full wave $3-\phi$ inverter may be understood from Fig. C.1.

C.1 Description of the system

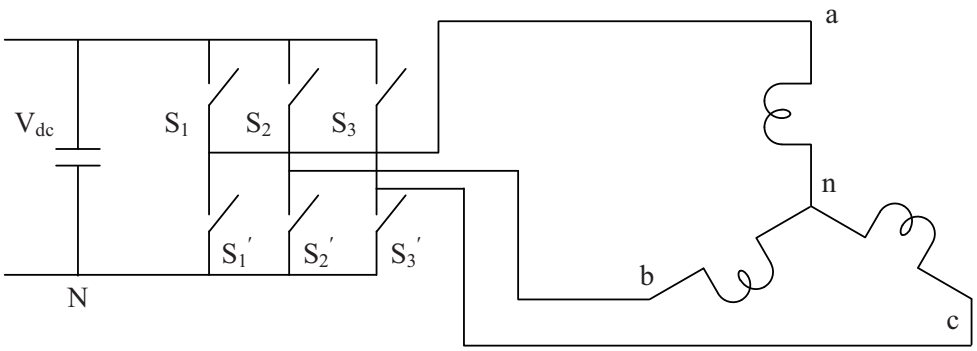

Figure C.1: A $3-\phi$ VSI system with load

The power electronic switches $(S_1, S_1', S_2, S_2', S_3, S_3')$ are used to convert

the DC bus voltage (V_{dc}) to alternating voltages for the load. The switches are configured from complementary function such that when one switch is ON, the other switch in the same leg remains OFF and vice versa.

C.2 Analysis

Applying KVL to the system we get,

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} + V_{Nn} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{C.1}$$

Now, for a balanced $3-\phi$ system,

$$V_{an} + V_{bn} + V_{cn} = 0 \tag{C.2}$$

Using (C.1) and (C.2) it may be shown that

$$V_{Nn} = -\frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) \tag{C.3}$$

and

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} \tag{C.4}$$

Now, if we consider (S_1, S_2, S_3) to represent the binary states (0, 1) of the switches in the three legs of the VSI, the switching voltages may be represented

as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \tag{C.5}$$

Thus, (C.4) may be rewritten as

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \tag{C.6}$$

Applying Clarke Transformation, we may write using eq. (A.1)

$$\begin{aligned} \begin{bmatrix} V_{\alpha n} \\ V_{\beta n} \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \\ &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \\ &= \frac{2}{9} \begin{bmatrix} 3 & -\frac{3}{2} & -\frac{3}{2} \\ 0 & 3\frac{\sqrt{3}}{2} & -3\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} V_{dc} \\ &= \frac{2}{3} \begin{bmatrix} S_1 - \frac{1}{2}(S_2 + S_3) \\ \frac{\sqrt{3}}{2}(S_2 - S_3) \end{bmatrix} V_{dc} \end{aligned} \tag{C.7}$$

Now, as each switch is either ON or OFF, the total number of unique combinations of the switches are $2^3 = 8$. So the voltage phasors in the transformed system will be as tabulated in Table C.1 The vectors thus formed is depicted

S_3	S_2	S_1	$V_{\alpha n}$	$V_{\beta n}$	$V_{S_1S_2S_3} = V_{\alpha n} + jV_{\beta n}$
0	0	0	0	0	0
0	0	1	$\frac{2}{3}V_{dc}$	0	$\frac{2}{3}V_{dc}$
0	1	0	$-\frac{1}{3}V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}e^{j\frac{2\pi}{3}}$
0	1	1	$\frac{1}{3}V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}e^{j\frac{\pi}{3}}$
1	0	0	$-\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}e^{-j\frac{2\pi}{3}}$
1	0	1	$\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}e^{-j\frac{\pi}{3}}$
1	1	0	$-\frac{2}{3}V_{dc}$	0	$\frac{2}{3}V_{dc}e^{j\pi}$
1	1	1	0	0	0

Table C.1: Clarke transformed vectors for the various switching states

in Fig. C.2. It can be seen that these forms the diagonal of a regular hexagon with each side of length $\frac{2}{3}V_{dc}$. The six sectors so formed are marked as I - VI. Now, to synthesize any vector $(V_s'\angle\theta)$ lying inside the n^{th} sector of the hexagon [as shown in Fig. C.3] with the weighted algebraic sum of the two space vectors making the sector , the expression for the same in matrix form will be

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}V_{dc} \begin{bmatrix} \cos\frac{(n-1)\pi}{3} & \cos\frac{n\pi}{3} \\ \sin\frac{(n-1)\pi}{3} & \sin\frac{n\pi}{3} \end{bmatrix} \begin{bmatrix} t_x \\ t_y \end{bmatrix} \tag{C.8}$$

where t_x and t_y are the weights applied to the space vector making up the n^{th} sector, respectively in the anticlockwise direction. The correct expression for

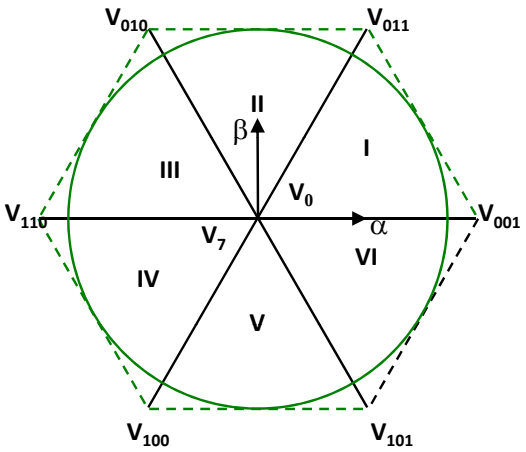

Figure C.2: The space vectors for the various switching states

the weighted sum will be [23]

$$t_x V_x + t_y V_y + t_z/2(V_{000} + V_{111}) = V_s' \tag{C.9}$$

with the constraint

$$t_x + t_y + t_z = 1 \tag{C.10}$$

V_x, V_y being the corresponding space vectors of magnitude $\frac{V_{dc}}{2}$ but with an angle of $\frac{\pi}{3}$ between them.

Now the angle of the vector may be expressed as

$$\theta = (n-1)\frac{\pi}{3} + \gamma \tag{C.11}$$

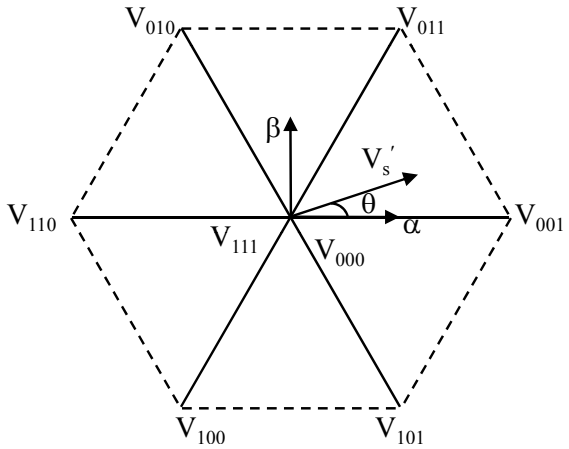

Figure C.3: Synthesis of any vector by the space vectors

where $0 \leqslant \gamma < \frac{\pi}{3}$. The weights may be obtained as

$$\begin{aligned}
\begin{bmatrix} t_x \\ t_y \end{bmatrix} &= \frac{\sqrt{3}}{V_{dc}} \begin{bmatrix} \sin\frac{n\pi}{3} & -\cos\frac{n\pi}{3} \\ -\sin\frac{(n-1)\pi}{3} & \cos\frac{(n-1)\pi}{3} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \\
&= \frac{\sqrt{3}V_s'}{V_{dc}} \begin{bmatrix} \sin\frac{n\pi}{3} & -\cos\frac{n\pi}{3} \\ -\sin\frac{(n-1)\pi}{3} & \cos\frac{(n-1)\pi}{3} \end{bmatrix} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \\
&= \frac{\sqrt{3}V_s'}{V_{dc}} \begin{bmatrix} \sin(\frac{n\pi}{3} - \theta) \\ -\sin(\frac{(n-1)\pi}{3} - \theta) \end{bmatrix} \\
&= \frac{\sqrt{3}V_s'}{V_{dc}} \begin{bmatrix} \sin(\frac{\pi}{3} + \gamma) \\ \sin(\gamma) \end{bmatrix} \qquad [\text{from } (C.11)] \qquad \text{(C.12)}
\end{aligned}$$

Once these two are computed the rest is computed from (C.10) as

$$t_z = 1 - (t_x + t_y)) \tag{C.13}$$

Now, if the weights are to relate to the switching times

$$t_x \geqslant 0$$

$$t_y \geqslant 0$$

Also, these being proper fractions as the application cannot use the space vectors exceeding their value,

$$t_x \leqslant 1$$

$$t_y \leqslant 1$$

So we get the inequation

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} \leqslant \frac{\sqrt{3}V_s'}{V_{dc}} \begin{bmatrix} \sin(\frac{\pi}{3} + \gamma) \\ \sin(\gamma) \end{bmatrix} \leqslant \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{C.14}$$

From (C.11) and (C.14) we thus may say

$$\frac{V_{dc}}{\sqrt{3}} \leqslant V_s' \leqslant 0 \tag{C.15}$$

This may be compared with SPWM given in Fig. C.4 that indicates that the square wave peak is only $0.5V_{dc}$. So compared to SVPWM the DC bus

utilization is poor for SPWM. Moreover, SPWM contains more harmonics [48].

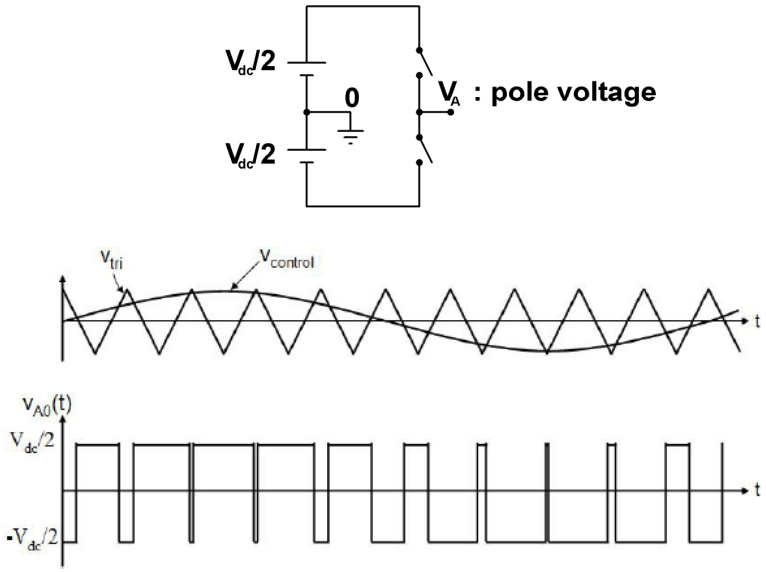

Figure C.4: Application of SPWM for inverters

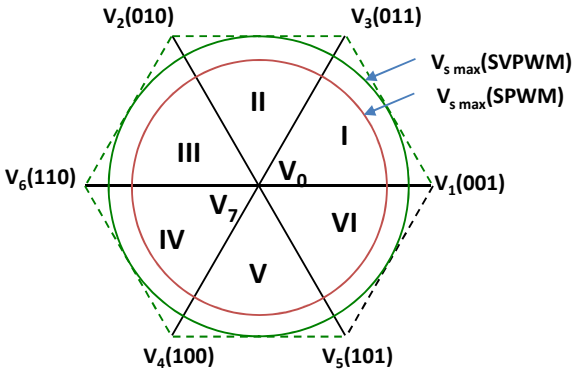

Figure C.5: Comparing the utilization of SPWM and SVPWM

Appendix D

Analysing LPF configurations for VSI

D.1 Derivations with T_1 and T_2

During the circuit analysis of the Δ-Y $3-\phi$ network in this appendix, there are several instances of analysing loops and nodes shared by two phases. Often, these involve difference operations between voltages and currents of the phases. To represent these operations, two matrices are used viz., T_1 and T_2. As the analysis is carried out for both phase sequences, two more matrices viz. S_{+1} and S_{-1} representing the positive and negative sequences respectively are used. Using the above four operators (defined in Operators section of Nomenclature) and remembering $a^3 = 1$, the following four relations

are derived that are extensively used in the subsequent sections.

$$
\begin{aligned}
T_1 S_{+1} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} &= \begin{bmatrix} (1-a^2) \\ (a-1) \\ (a^2-a) \end{bmatrix} \\
&= (1-a^2) \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} \\
&= (1-a^2) S_{+1} \\
&= \left(1 - (\cos\frac{2\pi}{3} - j\sin\frac{2\pi}{3})\right) S_{+1} \\
&= \sqrt{3} e^{j\frac{\pi}{6}} S_{+1} \qquad \text{(D.1)}
\end{aligned}
$$

$$
\begin{aligned}
T_1 S_{-1} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} &= \begin{bmatrix} (1-a) \\ (a^2-1) \\ (a-a^2) \end{bmatrix} \\
&= (1-a) \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} \\
&= (1-a) S_{-1} \\
&= \left(1 - (\cos\frac{2\pi}{3} + j\sin\frac{2\pi}{3})\right) S_{-1} \\
&= \sqrt{3} e^{-j\frac{\pi}{6}} S_{-1} \qquad \text{(D.2)}
\end{aligned}
$$

$$T_2 S_{+1} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} = \begin{bmatrix} (1-a) \\ (a-a^2) \\ (a^2-1) \end{bmatrix}$$

$$= (1-a) \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix}$$

$$= (1-a) S_{+1}$$

$$= \sqrt{3} e^{-j\frac{\pi}{6}} S_{+1} \tag{D.3}$$

$$T_2 S_{-1} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} = \begin{bmatrix} (1-a^2) \\ (a^2-a) \\ (a-1) \end{bmatrix}$$

$$= (1-a^2) \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix}$$

$$= (1-a^2) S_{-1}$$

$$= \sqrt{3} e^{j\frac{\pi}{6}} S_{-1} \tag{D.4}$$

D.2 Analysis of the L_pC_p topology

The L_pC_p topology is shown in Fig. D.1. The secondaries of the IT

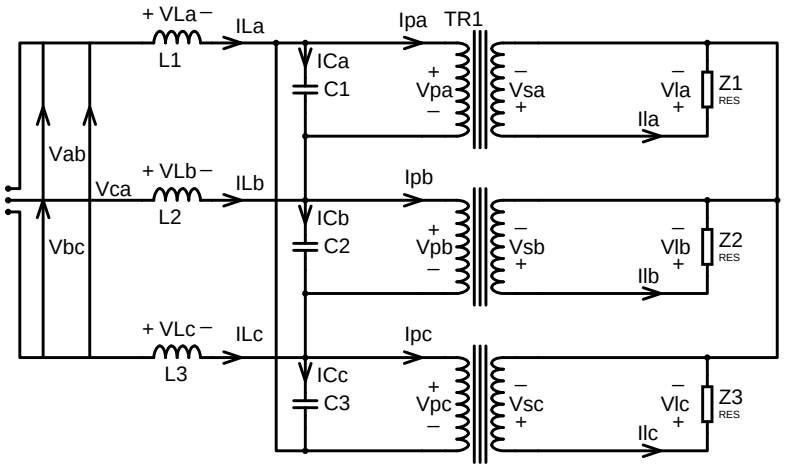

Figure D.1: Inverter with LC in IT primary

are across the load. So the winding voltages will be

$$V_s = V_l = S_p V_{la} [\text{for both abc } (p = +1) \text{ and acb } (p = -1) \text{ phase sequences}] \tag{D.5}$$

and

$$V_p = \frac{1}{n} V_s = \frac{1}{n} V_l \tag{D.6}$$

Again, the secondary currents are same as the load currents. So the IT currents are given by

$$I_s = I_l = \frac{1}{R_l} V_l \tag{D.7}$$

and

$$I_p = nI_s = \frac{n}{R_l}V_l \tag{D.8}$$

From eq. (D.6), the voltages across the primary capacitors (same as that in the IT primaries) will be

$$V_{Cp} = V_p = \frac{1}{n}V_l \tag{D.9}$$

and the corresponding current matrix is

$$I_{Cp} = j\omega C_p V_{Cp} = \frac{j\omega C_p}{n}V_l \tag{D.10}$$

From eq. (D.9), we may write

$$n_{Cl}(j\omega) = \frac{V_{Cpx}}{V_{lx}} = \frac{1}{n} \qquad [x = a, b, c] \tag{D.11}$$

Now, the current flowing through a filter inductor is derived by applying KCL in the node common to the inductor, the corresponding primary capacitors and the corresponding IT primaries. These node operations are represented by matrix T_1 whose expression is listed in Section D.1.

$$\begin{aligned}
\therefore I_L = T_1(I_p + I_{Cp}) &= \left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right) T_1 V_l \\
&= \left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right) T_1 S_p V_{la} \\
&= \left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right) \sqrt{3} e^{j\frac{p\pi}{6}} S_p V_{la}
\end{aligned}$$

$$= \sqrt{3}\left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right)e^{j\frac{p\pi}{6}}V_l$$
$$= \sqrt{3}\left(n + \frac{j\omega R_l C_p}{n}\right)e^{j\frac{p\pi}{6}}I_l \tag{D.12}$$

This gives

$$n_{Ll}(j\omega) = \frac{I_{Lpx}}{I_{lx}} \qquad \text{[same for any phase x]}$$
$$= \sqrt{3}\left(n + \frac{j\omega R_l C_p}{n}\right)e^{j\frac{p\pi}{6}} \tag{D.13}$$

The voltages across the inductors are given by,

$$V_L = j\omega L_p I_L = j\omega L_p \sqrt{3}\left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right)e^{j\frac{p\pi}{6}}V_l$$
$$= \sqrt{3}\omega\left(\frac{nL_p}{R_l} + \frac{j\omega L_p C_p}{n}\right)e^{j(\frac{\pi}{2}+\frac{p\pi}{3})}V_l \tag{D.14}$$

Now, for each of the inverter output line voltages KVL is used for the loop containing the line voltage terminals, the inductor drops and the drop across the corresponding primary capacitor. This is again notated as T_2, listed in Section D.1.

$$\therefore V_{invll} = T_2 V_L + V_p = T_2\sqrt{3}\omega\left(\frac{nL_p}{R_l} + \frac{j\omega L_p C_p}{n}\right)e^{j(\frac{\pi}{2}+\frac{p\pi}{6})}V_l + \frac{1}{n}V_l$$
$$= \sqrt{3}\omega\left(\frac{nL_p}{R_l} + \frac{j\omega L_p C_p}{n}\right)e^{j(\frac{\pi}{2}+\frac{p\pi}{6})}T_2 S_p V_{la} + \frac{1}{n}V_l$$
$$= \sqrt{3}\omega\left(\frac{nL_p}{R_l} + \frac{j\omega L_p C_p}{n}\right)e^{j(\frac{\pi}{2}+\frac{p\pi}{6})}\sqrt{3}e^{-j\frac{p\pi}{6}}S_p V_{la} + \frac{1}{n}V_l$$

$$= 3\omega\left(\frac{nL_p}{R_l} + \frac{j\omega L_p C_p}{n}\right)e^{j\frac{\pi}{2}}V_l + \frac{1}{n}V_l$$
$$= \left(\frac{1}{n}(1 - 3\omega^2 L_p C_p) + j(\frac{3n\omega L_p}{R_l})\right)V_l \quad \text{(D.15)}$$

From eq. (D.15), the index $G_{LP}(j\omega)$ for each phase can be computed by finding the ratio of each element of V_l to the corresponding element of V_{invll}. As obvious from the expression, the ratio will be the same in each case and will be

$$G_{LP}(j\omega) = \frac{1}{\left(\frac{1}{n}(1 - 3\omega^2 L_p C_p) + j(\frac{3n\omega L_p}{R_l})\right)} = \frac{\frac{n}{3L_p C_p}}{\left(-\omega^2 + j\frac{n^2}{R_l C_p}\omega + \frac{1}{3L_p C_p}\right)} \quad \text{(D.16)}$$

The line currents at the inverter output are same as the inductor currents and are given by

$$I_{invll} = I_L = \sqrt{3}\left(\frac{n}{R_l} + \frac{j\omega C_p}{n}\right)e^{j\frac{p\pi}{6}}V_l \quad \text{(D.17)}$$

D.3 Analysis of the L_sC_s topology

The L_sC_s topology is shown in Fig. D.2. The voltages across the secondary capacitors are same as the load voltages. So,

$$V_{Cs} = V_l \quad \text{(D.18)}$$

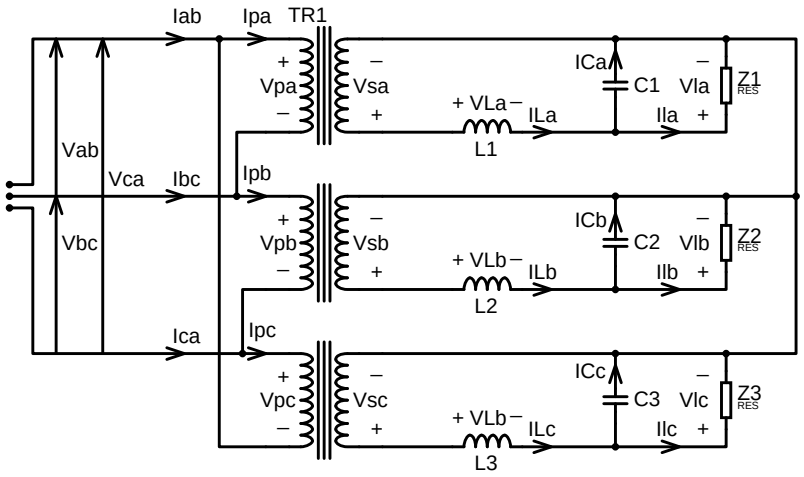

Figure D.2: Inverter with LC in IT secondary

Thus,

$$n_{Cl}(j\omega) = 1 \tag{D.19}$$

and

$$I_{Cs} = j\omega C_s V_l \tag{D.20}$$

The current in each inductor is the sum of the current through the capacitor and the load current.

$$\therefore I_L = I_{Cs} + I_l = \left(\frac{1}{R_l} + j\omega C_s\right) V_l = \left(1 + j\omega R_l C_s\right) I_l \tag{D.21}$$

This gives,

$$n_{Ll}(j\omega) = (1 + j\omega R_l C_s) \tag{D.22}$$

Again,

$$V_L = j\omega L_s I_L = j\omega L_s \left(\frac{1}{R_l} + j\omega C_s\right) V_l \tag{D.23}$$

Thus IT secondary voltages will be given by

$$V_s = V_l + V_L = \left(1 - \omega^2 L_s C_s + j\frac{\omega L_s}{R_l}\right) V_l \tag{D.24}$$

and correspondingly the voltage across the primary of the IT will be

$$V_p = \frac{1}{n} V_s = \frac{1}{n}\left(1 - \omega^2 L_s C_s + j\frac{\omega L_s}{R_l}\right) V_l \tag{D.25}$$

As each IT secondary current flows through the corresponding secondary inductor,

$$I_s = I_L = \left(\frac{1}{R_l} + j\omega C_s\right) V_l \tag{D.26}$$

and

$$I_p = n I_s = n\left(\frac{1}{R_l} + j\omega C_s\right) V_l \tag{D.27}$$

The inverter output line voltages will be

$$V_{invll} = V_p = \frac{1}{n}\left(1 - \omega^2 L_s C_s + j\frac{\omega L_s}{R_l}\right) V_l \tag{D.28}$$

which gives,

$$G_{LP}(j\omega) = \frac{1}{\frac{1}{n}\left(1 - \omega^2 L_s C_s + j\frac{\omega L_s}{R_l}\right)} = \frac{\frac{n}{L_s C_s}}{\left(-\omega^2 + j\frac{1}{R_l C_s}\omega + \frac{1}{L_s C_s}\right)} \quad \text{(D.29)}$$

The line currents from the inverter leads can be computed as

$$\begin{aligned} I_{invll} = T_1 I_p &= n\left(\frac{1}{R_l} + j\omega C_s\right) T_1 V_l \\ &= n\left(\frac{1}{R_l} + j\omega C_s\right) T_1 S_p V_{la} \\ &= n\left(\frac{1}{R_l} + j\omega C_s\right) \sqrt{3} e^{j\frac{p\pi}{6}} S_p V_{la} \\ &= \sqrt{3} n\left(\frac{1}{R_l} + j\omega C_s\right) e^{j\frac{p\pi}{6}} V_l \end{aligned} \quad \text{(D.30)}$$

D.4 Analysis of the $C_p L_s$ topology

The $C_p L_s$ topology is shown in Fig. D.3. The load currents are flowing through the corresponding secondary inductors. So,

$$I_L = I_l = \frac{V_l}{R_l} \quad \text{(D.31)}$$

which gives,

$$n_{Ll}(j\omega) = 1 \quad \text{(D.32)}$$

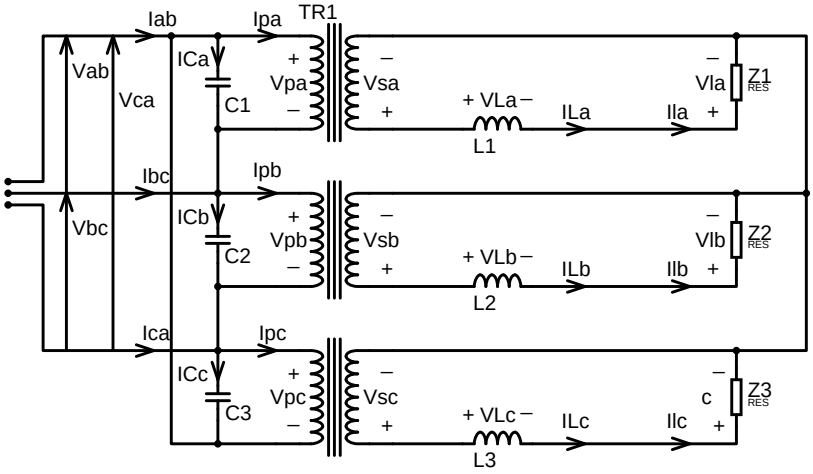

Figure D.3: Inverter with C in IT primary secondary and L in IT primary

and

$$V_L = j\omega L_s I_L = j\frac{\omega L_s}{R_l} V_l \tag{D.33}$$

The IT secondary voltages will be the vector sum of the load and the inductor drops in the corresponding phases.

$$V_s = V_l + V_L = (1 + j\frac{\omega L_s}{R_l})V_l \tag{D.34}$$

$$\therefore V_p = \frac{1}{n}V_s = \frac{1}{n}(1 + j\frac{\omega L_s}{R_l})V_l \tag{D.35}$$

The secondary currents will be the same as the inductor currents given by,

$$I_s = I_L = \frac{V_l}{R_l} \tag{D.36}$$

that corresponds to

$$I_p = nI_s = \frac{n}{R_l}V_l \tag{D.37}$$

The capacitor voltages are the same as the IT primary voltages

$$\therefore V_{Cp} = V_p = \frac{1}{n}\left(1 + j\frac{\omega L_s}{R_l}\right)V_l \tag{D.38}$$

and

$$I_{Cp} = j\omega C_p V_{Cp} = \frac{\omega C_p}{n}(-\frac{\omega L_s}{R_l} + j)V_l \tag{D.39}$$

So,

$$n_{Cl} = \frac{1}{n}(1 + j\frac{\omega L_s}{R_l}) \tag{D.40}$$

The inverter output line voltages will thus be

$$V_{invll} = V_{Cp} = \frac{1}{n}(1 + j\frac{\omega L_s}{R_l})V_l \tag{D.41}$$

which gives

$$G_{LP}(j\omega) = \frac{1}{\frac{1}{n}(1 + j\frac{\omega L_s}{R_l})} = \frac{\frac{nR_l}{L_s}}{\left(\frac{R_l}{L_s} + j\omega\right)} \tag{D.42}$$

The inverter output line currents are

$$\begin{aligned} I_{invll} = T_1(I_{Cp} + I_p) &= \left(\frac{\omega C_p}{n}(-\frac{\omega L_s}{R_l} + j) + \frac{n}{R_l}\right) T_1 V_l \\ &= \left(\frac{1}{R_l}(n - \frac{\omega^2 L_s C_p}{n}) + j\frac{\omega C_p}{n}\right) T_1 V_l \\ &= \left(\frac{1}{R_l}(n - \frac{\omega^2 L_s C_p}{n}) + j\frac{\omega C_p}{n}\right) T_1 S_p V_{la} \\ &= \sqrt{3}\left(\frac{1}{R_l}(n - \frac{\omega^2 L_s C_p}{n}) + j\frac{\omega C_p}{n}\right) e^{j\frac{p\pi}{6}} V_l \end{aligned} \tag{D.43}$$

D.5 Analysis of the L_pC_s topology

The L_pC_s topology is shown in Fig. D.4. The secondary capacitors are

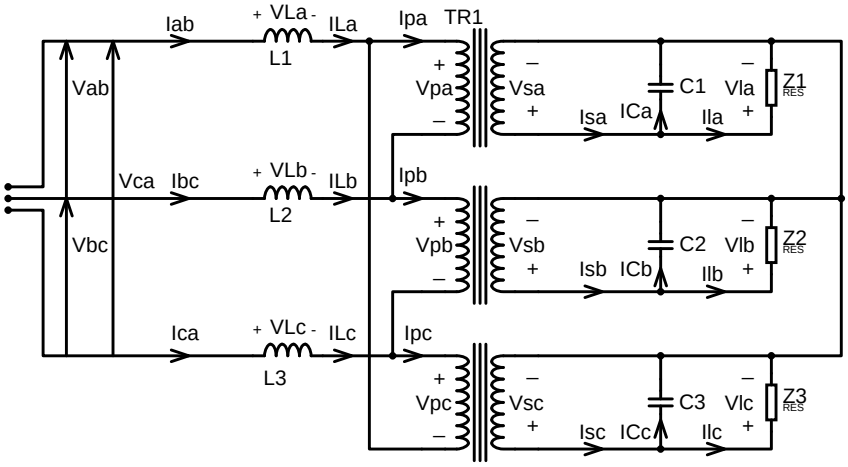

Figure D.4: Inverter with L in IT and C in IT secondary

placed across the load.

$$\therefore V_{Cs} = V_l \tag{D.44}$$

and

$$n_{Cl}(j\omega) = 1 \tag{D.45}$$

Also,

$$I_{Cs} = j\omega C_s V_{Cs} = j\omega C_s V_l \tag{D.46}$$

The load voltages are the same as IT secondary voltages. So,

$$V_s = V_l \tag{D.47}$$

and correspondingly,

$$V_p = \frac{1}{n} V_s = \frac{1}{n} V_l \tag{D.48}$$

The currents in the IT are computed as

$$I_s = I_l + I_{Cs} = (\frac{1}{R_l} + j\omega C_s) V_l \tag{D.49}$$

and

$$I_p = nI_s = n(\frac{1}{R_l} + j\omega C_s) V_l \tag{D.50}$$

The inductor currents are computed from KCL using the common node between them and the corresponding primary windings.

$$\begin{aligned} I_L = T_1 I_p &= n(\frac{1}{R_l} + j\omega C_s) T_1 S_p V_{la} \\ &= \sqrt{3}n(\frac{1}{R_l} + j\omega C_s) e^{j\frac{p\pi}{6}} S_p V_{la} \\ &= \sqrt{3}n\left(\frac{1}{R_l} + j\omega C_s\right) e^{j\frac{p\pi}{6}} V_l \\ &= \sqrt{3}n\left(1 + j\omega R_l C_s\right) e^{j\frac{p\pi}{6}} I_l \end{aligned} \tag{D.51}$$

$$\therefore n_{Ll}(j\omega) = \sqrt{3}n\left(1 + j\omega R_l C_s\right) e^{j\frac{p\pi}{6}} \tag{D.52}$$

Also,

$$V_L = j\omega L_p I_L = \sqrt{3}n\omega L_p(-\omega C_s + j\frac{1}{R_l}) e^{j\frac{p\pi}{6}} V_l \tag{D.53}$$

$$\begin{aligned} \therefore V_{invll} = T_2 V_L + V_p &= \sqrt{3}n\omega L_p(-\omega C_s + j\frac{1}{R_l}) e^{j\frac{p\pi}{6}} T_2 S_p V_{la} + \frac{1}{n} V_l \\ &= \sqrt{3}n\omega L_p(-\omega C_s + j\frac{1}{R_l}) e^{j\frac{p\pi}{6}} \sqrt{3} e^{-j\frac{p\pi}{6}} S_p V_{la} + \frac{1}{n} V_l \\ &= 3n\omega L_p(-\omega C_s + j\frac{1}{R_l}) S_p V_{la} + \frac{1}{n} V_l \\ &= 3n\omega L_p(-\omega C_s + j\frac{1}{R_l}) V_l + \frac{1}{n} V_l \\ &= \left((\frac{1}{n} - 3n\omega^2 L_p C_s) + j\frac{3n\omega L_p}{R_l}\right) V_l \end{aligned} \tag{D.54}$$

which gives

$$G_{LP}(j\omega) = \frac{1}{\left((\frac{1}{n} - 3n\omega^2 L_p C_s) + j\frac{3n\omega L_p}{R_l}\right)} = \frac{\frac{1}{3nL_pC_s}}{\left(-\omega^2 + j\frac{1}{R_l C_s} + \frac{1}{3n^2 L_p C_s}\right)} \tag{D.55}$$

The current will be

$$I_{invll} = I_L = \sqrt{3}n(\frac{1}{R_l} + j\omega C_s)e^{j\frac{p\pi}{6}} V_l \tag{D.56}$$

D.6 Analysis of the $L_pC_pC_s$ topology

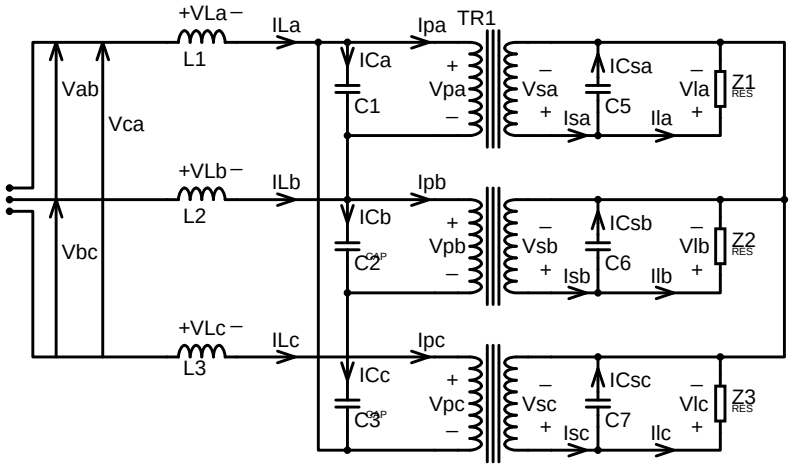

Figure D.5: Inverter with LC in IT primary and C in IT secondary

The secondary capacitor voltages will be

$$V_{Cs} = V_l \tag{D.57}$$

$$\therefore n_{Csl} = 1 \tag{D.58}$$

and the current flowing through them are

$$I_{Cs} = j\omega C_s V_{Cs} = j\omega C_s V_l \tag{D.59}$$

The IT secondary voltages will be the same as the load voltages.

$$\therefore V_s = V_l \tag{D.60}$$

So,

$$V_p = \frac{1}{n} V_s = \frac{1}{n} V_l \tag{D.61}$$

The IT currents are computed as

$$I_s = I_{Cs} + I_l = \left(\frac{1}{R_l} + j\omega C_s \right) V_l \tag{D.62}$$

and

$$I_p = n I_s = n \left(\frac{1}{R_l} + j\omega C_s \right) V_l \tag{D.63}$$

Now, the voltages across the primary capacitors are

$$V_{Cp} = V_p = \frac{1}{n} V_l \tag{D.64}$$

$$\therefore n_{Cpl} = \frac{1}{n} \tag{D.65}$$

and

$$I_{Cp} = j\omega C_p V_{Cp} = j\frac{\omega C_p}{n} V_l \tag{D.66}$$

Now,

$$\begin{aligned} I_{Lp} = T_1(I_p + I_{Cp}) &= \left(\frac{n}{R_l} + jn\omega C_s + j\frac{\omega C_p}{n}\right) T_1 V_l \\ &= \left(\frac{n}{R_l} + j\omega(\frac{C_p}{n} + nC_s)\right) T_1 V_l \\ &= \left(\frac{n}{R_l} + j\omega(\frac{C_p}{n} + nC_s)\right) T_1 S_p V_{la} \\ &= \sqrt{3}\left(\frac{n}{R_l} + j\omega(\frac{C_p}{n} + nC_s)\right) e^{j\frac{p\pi}{6}} S_p V_{la} \\ &= \sqrt{3}\left(\frac{n}{R_l} + j\omega(\frac{C_p}{n} + nC_s)\right) e^{j\frac{p\pi}{6}} V_l \\ &= \sqrt{3}\left(n + j\omega R_l(\frac{C_p}{n} + nC_s)\right) e^{j\frac{p\pi}{6}} I_l \end{aligned} \tag{D.67}$$

$$\therefore n_{Ll}(j\omega) = \sqrt{3}\left(n + j\omega R_l(\frac{C_p}{n} + nC_s)\right) e^{j\frac{p\pi}{6}} \tag{D.68}$$

The voltages across the inductors are

$$V_{Lp} = j\omega L_p I_{Lp} = \sqrt{3}\omega L_p\left(-\omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\right) e^{j\frac{p\pi}{6}} V_l \tag{D.69}$$

The inverter outputs are

$$\begin{aligned} V_{invll} = T_2 V_{Lp} + V_p &= \sqrt{3}\omega L_p\bigg(- \omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\bigg)e^{j\frac{p\pi}{6}}\, T_2 S_p V_{la} + \frac{1}{n}V_l \\ &= 3\omega L_p\bigg(- \omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\bigg)V_l + \frac{1}{n}V_l \\ &= \bigg((\frac{1}{n} - 3\omega^2 L_p(\frac{C_p}{n} + nC_s)) + j\frac{3n\omega L_p}{R_l}\bigg)V_l \end{aligned} \tag{D.70}$$

$$\therefore G_{LP}(j\omega) = \frac{\frac{n}{3L_p(C_p+n^2C_s)}}{\bigg(- \omega^2 + j\frac{n^2}{R_l(C_p+n^2C_s)}\omega + \frac{1}{3L_p(C_p+n^2C_s)}\bigg)} \tag{D.71}$$

Also,

$$I_{invll} = I_{Lp} = \sqrt{3}\bigg(\frac{n}{R_l} + j\omega(\frac{C_p}{n} + nC_s)\bigg)e^{j\frac{p\pi}{6}}\, V_l \tag{D.72}$$

Appendix E

Inverter parameters for DVR

The VSI with the low pass filter in $L_pC_pC_s$ configuration is shown in Fig. E.1. Applying KVL to the load circuit of any phase,

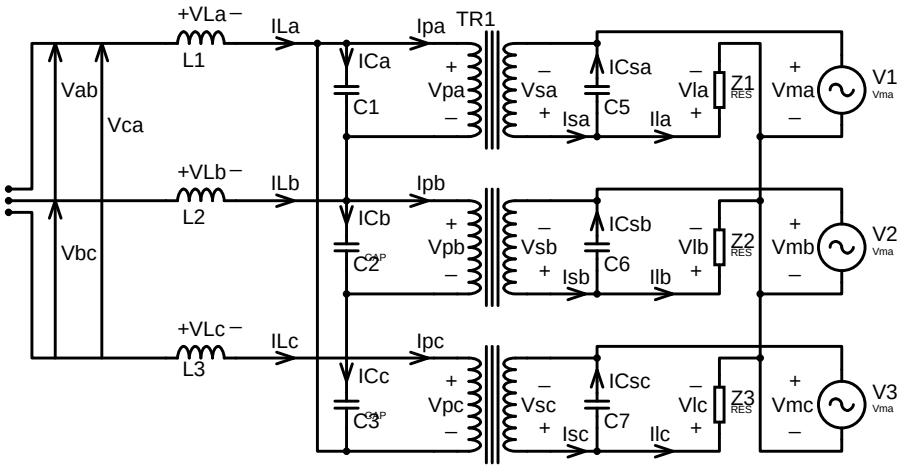

Figure E.1: VSI configured for DVR with $L_pC_pC_s$ type low pass filter

$$V_l = V_{mp} + V_{Cs} \tag{E.1}$$

So, for a sag of k_{sag} at the mains, once phase is locked,

$$V_{Cs} = V_l - V_{mp} = V_{pref} - k_{sag}v_{pref} = (1 - k_{sag})v_{pref} \tag{E.2}$$

and the current flowing through it is

$$I_{Cs} = j\omega C_s V_{Cs} = j(1 - k_{sag})\omega C_s v_{pref} \tag{E.3}$$

The IT secondary voltages will be the same as the capacitor voltage.

$$\therefore V_s = (1 - k_{sag})v_{pref} \tag{E.4}$$

So,

$$V_p = \frac{1}{n}V_s = \frac{(1 - k_{sag})}{n}v_{pref} \tag{E.5}$$

The IT currents are computed as

$$I_s = I_{Cs} + I_l = \left(\frac{1}{R_l} + j(1 - k_{sag})\omega C_s\right)v_{pref} \tag{E.6}$$

and

$$I_p = nI_s = n\left(\frac{1}{R_l} + j(1 - k_{sag})\omega C_s\right)v_{pref} \tag{E.7}$$

Now, the voltage across the primary capacitor is

$$V_{Cp} = V_p = \frac{(1 - k_{sag})}{n}v_{pref} \tag{E.8}$$

$$\therefore I_{Cp} = j\omega C_p V_{Cp} = j\frac{(1-k_{sag})\omega C_p}{n} v_{pref} \tag{E.9}$$

Now,

$$\begin{aligned} I_{Lp} = T_1(I_p + I_{Cp}) &= \left(\frac{n}{R_l} + jn(1-k_{sag})\omega C_s + j\frac{(1-k_{sag})\omega C_p}{n}\right) T_1 v_{pref} \\ &= \sqrt{3}\left(\frac{n}{R_l} + j(1-k_{sag})\omega(nC_s + \frac{C_p}{n})\right) e^{j\frac{p\pi}{6}} v_{pref} \end{aligned} \tag{E.10}$$

The voltage across the inductor is

$$V_{Lp} = j\omega L_p I_{Lp} = \sqrt{3}\omega L_p\left(-(1-k_{sag})\omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\right) e^{j\frac{p\pi}{6}} v_{pref} \tag{E.11}$$

The inverter output is

$$\begin{aligned} V_{invll} &= T_2 V_{Lp} + V_p \\ &= \sqrt{3}\omega L_p\left(-(1-k_{sag})\omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\right) e^{j\frac{p\pi}{6}} T_2 S_p V_{apref} \\ &\quad + \frac{(1-k_{sag})v_{pref}}{n} \\ &= 3\omega L_p\left(-(1-k_{sag})\omega(\frac{C_p}{n} + nC_s) + j\frac{n}{R_l}\right) v_{pref} + \frac{(1-k_{sag})v_{pref}}{n} \\ &= \left((1-k_{sag})(\frac{1}{n} - 3\omega^2 L_p(\frac{C_p}{n} + nC_s)) + j\frac{3n\omega L_p}{R_l}\right) v_{pref} \end{aligned} \tag{E.12}$$

$$I_{invll} = I_{Lp} = \sqrt{3}\left(\frac{n}{R_l} + j(1-k_{sag})\omega(nC_s + \frac{C_p}{n})\right) e^{j\frac{p\pi}{6}} v_{pref} \tag{E.13}$$

References

[1] A. de Almeida, L. Moreira, and J. Delgado, "Power quality problems and new solutions," in *Proceedings of the International Conference on Renewable Energy and Power Quality*, Vigo (Espanha), April 2003, pp. 150–158.

[2] M. H. Ali, B. Wu, and R. A. Dougal, "An overview of SMES applications in power and energy systems," *Sustainable Energy, IEEE Transactions on*, vol. 1, no. 1, pp. 38–47, April 2010.

[3] R. Carnegi, D. Gotham, D. Nderitu, and P. V. Preckel, "Utility scale energy storage systems benefits, applications, and technologies," p. 95, June 2013, State Utility Forecasting Group, Purdue University.

[4] D. Connolly, "An investigation into the energy storage technologies available, for the integration of alternative generation techniques," University of Limerick, Energy Storage Report, November 2007.

[5] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy, and Y. Liu, "Energy storage systems for advanced power applications," *Proceedings of the IEEE*, vol. 89, no. 12, pp. 1744–1756, Dec 2001.

[6] P. Tixador, "SMES," European Summer School on Supernoductivity, Turku, Finland, June 2011, Lecture.

[7] A. De, S. Srivastava, V. K. Khare, S. Bandyopadhyay, T. P. Tiwari, B. Sarkar, S. K. Thakur, M. Das, and S. Saha, "Superconducting magnet for cyclotrons and its application for energy storage systems at VECC," in *Workshop on Cyclotrons: Rising Expectations & Mounting Challenges*, VECC, Kolkata, June 2008, pp. 33–41.

[8] "Superconducting magnetic energy storage," Factsheet to accompany the report "Pathways for energy storage in the UK", [Online; accessed 12-August-2014]. [Online]. Available: http://www.lowcarbonfutures.org/sites/default/files/superconductingmagneticenergystorage_final.pdf

[9] P. Tixador, "Superconducting magnetic energy storage; status and perspective," in *IEEE/CSC&ESAS European Superconductivity news forum*, no. 3, January 2008.

[10] M. Kavitha, N. Ratnakar, and M. Reddy, "Integration of FACTS into energy storage systems for future power systems applications," *Advanced Research in Electrical, Electronics and Instrumentation Engineering, International Journal of*, vol. 2, no. 2, pp. 800–810, February 2013.

[11] K. E. Nielsen, "Superconducting magnetic energy storage in power systems with renewable energy sources," Master's thesis, Norwegian University of Science and Technology, Trondheim, Jun 2010.

[12] L. R. Lawrence (Jr), C. Cox, and D. Broman, "High temperature superconductivity: The products and their benefits," Oak Ridge National

Lab., TN (United States), Tech. Rep., July 1998, prepared for the U.S. DOE, ORNL/Sub/97-SX339V/2.

[13] W. Hasenzahl, "A comparison of the conductor requirements for energy storage devices made with ideal coil geometries," *IEEE Transactions on Magnetics*, vol. 25, no. 2, pp. 1799–1802, March 1989.

[14] A. Badel, "Superconducting magnetic energy storage using high temperature superconductor for pulse power supply," Ph.D. dissertation, l'Institut polytechnique de Grenoble, Universite de Grenoble, Sep 2010.

[15] X. D. Xue, K. W. E. Cheng, and D. Sutanto, "Power system applications of superconducting magnetic energy storage systems," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 2, Oct 2005, pp. 1524–1529.

[16] M. G. Molina and P. E. Mercado, "Primary frequency control of multimachine power systems with STATCOM-SMES: a case study," *International Journal of Electrical Power & Energy Systems*, vol. 44, no. 1, pp. 388–402, January 2013.

[17] M. G. Molina, P. E. Mercado, and E. H. Watanabe, "Improved superconducting magnetic energy storage (SMES) controller for high-power utility applications," *Energy Conversion, IEEE Transactions on*, vol. 26, no. 2, pp. 444–456, June 2011.

[18] J. B. X. Devotta and M. G. Rabbani, "Application of superconducting magnetic energy storage unit in multi-machine power systems," *Energy conversion and management*, vol. 41, no. 5, pp. 493–504, March 2000.

[19] F. C. Beach and I. R. McNab, "Present and future naval applications for pulsed power," in *Pulsed Power Conference, 2005 IEEE*, June 2005, pp. 1–7.

[20] P. I. James and G. Stejic, "Advanced naval energy storage - revisiting SMES," in *Proceedings of the ASNE Day 2008: The Road to CG(X): Future Cruiser & Sea-Based Missile Defence*, Virginia, June 2008.

[21] K. P. Juengst, R. Gehring, A. Kudymow, G. Kuperman, and E. Suess, "SMES based power modulator," Status, August 2001, Scientific Report, FZKA 6568.

[22] A. Sannino, J. Svensson, and T. Larsson, "Power-electronic solutions to power quality problems," *Electric Power Systems Research*, vol. 66, no. 1, pp. 71 – 82, July 2003.

[23] A. De, S. Kumari, V. K. Khare, S. S. Pal, A. Sadhukhan, V. K. Meshram, S. K. Thakur, and S. Saha, "Design, development and testing of a DSP based dynamic voltage restorer," in *Electronic System Design (ISED), 2012 International Symposium on*, Dec 2012, pp. 157–161.

[24] "IEEE recommended practice for monitoring electric power quality," *IEEE Std. 1159-1995*, 1995.

[25] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 3rd ed. Prentice-Hall, ISBN 0-13-373762-4, October 1995.

[26] I. A. Brezovich, "Digital vs. analogue control systems," May 2011, presented at the 2011 Annual Meeting of the American College of Medical Physics, Chattanooga, TN.

[27] P. Murphy, M. Xie, Y. Li, M. Ferdowsi, N. Patel, F. Fatehi, A. Homaifar, and F. Lee, "Study of digital vs analog control," in *Power Electronics Seminar Proceedings (CPES Center for Power Electronics Systems)*, 2002, pp. 203–206.

[28] M. Heqitson, "Digital vs. Analogue control," GEO ISC Meeting, Hannover, Feb, 2010, Lecture.

[29] R. M. Mathur and R. K. Varma, *Thyristor-based FACTS Controllers for Electrical Transmission Systems*. Wiley India Private Limited, August 2011.

[30] B. C. Kuo, *Digital Control Systems*, 2nd ed. Oxford University Press, ISBN 978-0-19-568620-3, 2007.

[31] N. G. Hingorani and L. Gyugyi, *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*. Wiley India Private Limited, ISBN 9788126530403, 2011.

[32] "Flexible AC transmission systems," [Online; accessed 24-February-2014]. [Online]. Available: http://shodhganga.inflibnet.ac.in/bitstream/10603/2438/11/11_chapter\%203.pdf

[33] J. Dixon, L. Moran, J. Rodriguez, and R. Domke, "Reactive power com-

pensation technologies, state-of-the-art review," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2144–2164, Dec 2005.

[34] "Modelling of distribution system, power electronics devices with respect to their load flow and short circuit behavour," Phase to Phase BV, Arnhem, May 2004.

[35] Y. Zhang, Y. Zhang, and C. Chen, "A novel power injection model of IPFC for power flow analysis inclusive of practical constraints," *Power Systems, IEEE Transactions on*, vol. 21, no. 4, pp. 1550–1556, Nov 2006.

[36] A. Lashkar Ara and S. A. Nabavi Niaki, "Comparison of the FACTS equipment operation in transmission and distribution systems," in *17th International Conference on Electricity Distribution (CIRED)*, Barcelona, May 2003, session 2, paper no 44.

[37] J. J. Paserba, "How FACTS controllers benefit AC transmission systems," in *Transmission and Distribution Conference and Exposition, 2003 IEEE PES*, vol. 3, September 2003, pp. 991–998.

[38] L. Gyugyi, C. D. Schauder, C. W. Edwards, and M. Sarkozi, "Apparatus and method for dynamic voltage restoration of utility distribution networks," Jul. 12 1994, US Patent 5,329,222.

[39] C. Benachaiba and F. Brahim, "Voltage quality improvement using DVR," *Electrical Power Quality and Utilisation, Journal*, vol. XIV, no. 1, pp. 39–46, 2008.

[40] A. M. Shazly, A. G. Cerrada, M. A. Abdel-Moamen, and B. Hasanin,

"Dynamic voltage restorer (DVR) system for compensation of voltage sags, state-of-the-art review," *International Journal Of Computational Engineering Research*, vol. 3, no. 1, pp. 177–183, Jan 2013.

[41] H. Amaris, M. Alonso, and C. Ortega, *Reactive Power Management of Power Networks with Wind Generation (Lecture Notes in Energy)*. Springerm, ISBN 9781447146667, November 2012.

[42] T. I. El-Shennawy, A. M. Moussa, M. A. El-Gammal, and A. Y. Abou-Ghazala, "A dynamic voltage restorer for voltage sag mitigation in a refinery with induction motors loads," *Americal Journal of Engineering and Applied Sciences*, vol. 3, no. 1, pp. 144–151, 2010.

[43] H. Ezoji, A. R. Sheikhaleslami, A. Ghatresamani, M. Shahverdi, and M. H. Alborzi, "Hysteresis voltage control of dvr based on unipolar pwm." in *Applications of MATLAB in Science and Engineering*, T. Michalowski, Ed. INTECH Open Access Publisher, 2011, ch. 14, pp. 83–96.

[44] W. C. Duesterhoeft, M. W. Schulz, and E. Clarke, "Determination of instantaneous currents and voltages by means of alpha, beta, and zero components," *Transactions of the American Institute of Electrical Engineers*, vol. 70, no. 2, pp. 1248–1255, July 1951.

[45] R. H. Park, "Two-reaction theory of synchronous machines generalized method of analysis-part i," *Transactions of the American Institute of Electrical Engineers*, vol. 48, no. 3, pp. 716–727, July 1929.

[46] Z. G. Wang, J. X. Jin, Y. G. Guo, and J. G. Zhu, "SVPWM techniques

and applications in HTS PMSM machines control," *Journal of Electronic Science and Technology of China*, vol. 6, no. 2, pp. 191–197, June 2008.

[47] J. P. i Felix, "Modulation and control of three-phase PWM multilevel converters," Ph.D. dissertation, Technical University of Catalonia, Spain, November 2002.

[48] N. Mohan, W. Sulkowski, P. Jose, and T. Brekken, "Including voltage space vector PWM in undergraduate courses," accessed Jul 09, 2012. [Online]. Available: {http://et.upt.ro/admin/tmpfile/fileE1224952113file490349319450a.pdf}

[49] S. de Pablo, A. B. Rey, L. C. Herrero, and J. M. Ruiz, "A simpler and faster method for svm implementation," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–9.

[50] K. Nagar, A. K. Sharma, D. K. Palwalia, and S. Amit, "Harmonic analysis of three phase spwm and svpwm converters," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 3, no. 11, pp. 12 977–12 985, November 2014.

[51] X. Kestelyn, E. Semail, and J.-P. Hautier, "Multi-phase system supplied by svm vsi: A new fast algorithm to compute duty cycles," *EPE Journal*, vol. 14, no. 3, pp. 25–31, 2004.

[52] V. K. Ramachandaramurthy, C. Fitzer, A. Arulampalam, C. Zhan, M. Barnes, and N. Jenkins, "Control of a battery supported dynamic voltage restorer," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 149, no. 5, pp. 533–542, Sep 2002.

[53] C. Zhan, V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, S. Kromlidis, M. Barnes, and N. Jenkins, "Dynamic voltage restorer based on voltage space vector PWM control," in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, vol. 2, 2001, pp. 1301–1307.

[54] G.-C. Hsieh and J. Hung, "Phase-locked loop techniques. a survey," *Industrial Electronics, IEEE Transactions on*, vol. 43, no. 6, pp. 609–615, Dec 1996.

[55] D. Abramovitch, "Phase-locked loops: a control centric tutorial," in *American Control Conference, 2002. Proceedings of the 2002*, vol. 1, 2002, pp. 1–15.

[56] F. D. Freijedo, A. G. Yepes, O. Lopez, P. Fernandez-Comesana, and J. Doval-Gandoy, "An optimized implementation of phase locked loops for grid applications," *Instrumentation and Measurement, IEEE Transactions on*, vol. 60, no. 9, pp. 3110–3119, Sept 2011.

[57] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 8, pp. 2923–2932, Aug 2008.

[58] C. Zhan, C. Fitzer, V. K. Ramachandaramurthy, A. Arulampalam, M. Barnes, and N. Jenkins, "Software phase-locked loop applied to dynamic voltage restorer (DVR)," in *Power Engineering Society Winter Meeting, 2001. IEEE*, vol. 3, 2001, pp. 1033–1038.

[59] M. M. Mehta and V. Chandrasekhar, "A hybrid analog-digital phase-locked loop for frequency mode non-contact scanning probe microscopy," *Review of Scientific Instruments*, vol. 85, no. 1, 2014, eid. 013707.

[60] A. A. Ahmad, M. Pichan, and A. Abrishamifar, "A new simple structure PLL for both single and three phase applications," *International Journal of Electrical Power & Energy Systems*, vol. 74, pp. 118–125, January 2016.

[61] S. M. Shahruz, "Low-noise and fast-locking phase-locked loop," *Review of Scientific Instruments*, vol. 73, no. 12, 2002.

[62] S. Gautam, P. Yunqing, M. Kashif, Y. R. Kafle, Z. Z. Hua, and L. Bo, "Study on software phase locked loop for single phase active power filter," in *Communication and Computing (ARTCom 2013), Fifth International Conference on Advances in Recent Technologies in*, Sept 2013, pp. 319–327.

[63] K. M. Rolfes, "The automated software phase-locked loop and the exploration of an adaptive algorithm for the adjustment of PLL parameters," Master's thesis, University of Wisconsin - Madison, 1994.

[64] A. Papavasiliou, S. A. Papathanassiou, S. N. Manias, and G. Demetriadis, "Current control of a voltage source inverter connected to the grid via LCL filter," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, June 2007, pp. 2379–2384.

[65] A. Houari, H. Renaudineau, B. Nahid-Mobarakeh, J. P. Martin, S. Pierfederici, and F. Meibody-Tabar, "Large signal stability analysis

and stabilization of converters connected to grid through LCL filters," *Industrial Electronics, IEEE Transactions on*, vol. 61, no. 12, pp. 6507–6516, Dec 2014.

[66] S. Eren, M. Pahlevaninezhad, A. Bakhshai, and P. Jain, "Composite nonlinear feedback control and stability analysis of a grid-connected voltage source inverter with LCL filter," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 11, pp. 5059–5074, Nov 2013.

[67] J. Scoltock, T. Geyer, and U. Madawala, "Model predictive direct current control for a grid-connected converter: LCL-filter versus L-filter," in *Industrial Technology (ICIT), 2013 IEEE International Conference on*, Feb 2013, pp. 576–581.

[68] M. Hanif, V. Khadkikar, W. Xiao, and J. L. Kirtley, "Two degrees of freedom active damping technique for LCL filter-based grid connected PV systems," *Industrial Electronics, IEEE Transactions on*, vol. 61, no. 6, pp. 2795–2803, June 2014.

[69] J. Xu, J. Yang, J. Ye, Z. Zhang, and A. Shen, "An LTCL filter for three-phase grid-connected converters," *Power Electronics, IEEE Transactions on*, vol. 29, no. 8, pp. 4322–4338, Aug 2014.

[70] K. R. Padiyar, *FACTS Controllers in Power Transmission and Distribution.* New Agw International (P) Limited, Publishers, 2007.

[71] S. J. Yao, Z. G. Zhu, H. Y. Zhang, J. W. Cao, and G. Y. Zhang, "The design of filter parameters of dynamic voltage restorer in medium voltage network," *Applied Mechanics and Materials*, vol. 64, pp. 133–141, 2014.

[72] H. Kim, J.-H. Kim, and S.-K. Sul, "A design consideration of output filters for dynamic voltage restorers," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 6, June 2004, pp. 4268–4272.

[73] S. Guo and D. Liu, "Analysis and design of output LC filter system for dynamic voltage restorer," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, March 2011, pp. 1599–1605.

[74] G. Chen, M. Zhu, and C. Xu, "Parameter optimization of the LC filters based on multiple impact factors for cascaded H-bridge dynamic voltage restorers," *Journal of Power Electronics*, vol. 14, pp. 165–174, January 2014.

[75] S. A. O. da Silva, E. Tomizaki, R. Novochadlo, and E. A. A. Coelho, "PLL structures for utility connected systems under distorted utility conditions," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, Nov 2006, pp. 2636–2641.

[76] S. Gautam, P. Yunqing, M. Kashif, Y. Kafle, Z. Z. Hua, and L. Bo, "Study on software phase locked loop for single phase active power filter," in *Communication and Computing (ARTCom 2013), Fifth International Conference on Advances in Recent Technologies in*, Sept 2013, pp. 319–327.

[77] M. O. Sonnaillon, R. Urteaga, and F. J. Bonetto, "Software PLL based

on random sampling," *Instrumentation and Measurement, IEEE Transactions on*, vol. 59, no. 10, pp. 2621–2629, Oct 2010.

[78] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *Industry Applications, IEEE Transactions on*, vol. 45, no. 6, pp. 2039–2047, Nov 2009.

[79] B. P. Lathi, *Modern Digital and Analog Communication Systems*, 3rd ed., ser. The Oxford series in electrical and computer engineering. Oxford University Press, ISBN 0-19-511009-9, March 1998.

[80] M. S. Santina, A. R. Stubberud, and G. H. Hostetter, "Discrete-time equivalents to continuous-time systems," in *The Control Handbook*, 1st ed., ser. Electrical Engineering Handbook, W. S. Levine, Ed. CRC Press, ISBN 0-8493-8570-9, February 1996, ch. 13, pp. 265–279.

[81] T. Adam, S. Dadvandipour, and F. Jozsef, "Influence of discretization method on the digital control system performance," *Acta Montanistica Slovaca*, vol. 8, no. 4, pp. 197–200, 2003.

[82] U. Bhunia, J. Pradhan, A. Roy, V. Khare, U. Panda, A. De, S. Bandopadhaya, T. Bhattacharyya, S. Thakur, M. Das, S. Saha, C. Mallik, and R. K. Bhandari, "Design, fabrication and cryogenic testing of 0.6 MJ SMES coil," *Cryogenics*, vol. 52, no. 12, pp. 719 – 724, 2012, Special Issue: ACASC 2011.