TRANSITION METAL OXIDE-BASED DEVICES FOR MEMORY APPLICATIONS

By

Abhishek Rakshit

PHYS05201504012

Surface Physics and Materials Science Division

Saha Institute of Nuclear Physics, Kolkata

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---------- **Date :**
Guide : Prof. Supratic Chakraborty

---------- **Date :**
Member : Prof. Tapas Kumar Chini

---------- **Date :**
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DECLARATION

I, hereby, declare that the investigation presented in the thesis has been carried out by me. The work is original and the work has not been submitted earlier as a whole or in part for a degree/diploma at this or any other Institution or University.

Abhishek Rakshit
11/11/2020

Abhishek Rakshit

List of Publications

a. Published journal articles included in PhD thesis

1. *Control of interfacial layer growth during deposition of high-κ oxide thin films in reactive RF-sputtering system*,

Abhishek Rakshit, Arijit Bose, Debaleen Biswas, Radhaballav Bhar, and Supratic Chakraborty, **Applied Surface Science 423**, 957 (2017).

2. *Effect of oxygen content on the electrical properties of sputter deposited vanadium oxide thin-films*,

Abhishek Rakshit, Manabendra Mukherjee, and Supratic Chakraborty, **Materials Science in Semiconductor Processing 88**, 127 (2018).

3. *Insulator-to-metal transition of vanadium oxide-based metal-oxide-semiconductor devices at discrete measuring temperatures*,

Abhishek Rakshit, Karimul Islam, Anil Kumar Sinha, and Supratic Chakraborty, **Semiconductor Science and Technology 34**, 055001 (2019).

4. *Effect of oxygen content and crystallization temperature on the insulator-to-metal transition properties of vanadium oxide thin-films*,

Abhishek Rakshit, Karimul Islam, Rezwana Sultana, and Supratic Chakraborty, **Vacuum 180**, 109633 (2020).

b. Conference papers/presentations included in PhD thesis

1. *A novel instrumental modification of an existing reactive RF–sputtering system for reducing the interfacial layer formation during deposition of high–κ oxide thin film*, Abhishek Rakshit, Debaleen Biswas, and Supratic Chakraborty presented at Young Scientists' Colloquium (YSC) - 2017.

2. *Deposition and characterization of vanadium oxide based thin films for MOS device applications*, Abhishek Rakshit, Debaleen Biswas and Supratic Chakraborty, **AIP Conference Proceedings 1942**, 120024 (2018), presented at DAE Solid State Physics Symposium (SSPS) - 2017.

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2. *Effect of Zr doping and lattice oxygen release on the resistive switching properties of $Zr_xHf_{1-x}O_2$-based metal-oxide-semiconductor devices*,

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3. *X-ray reflectivity and X-ray photoelectron spectroscopy studies on reactively*

sputtered Nb_2O_5-based thin-film devices,

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Abhishek Rakshit

This thesis is dedicated to my Baba, Maa and Mom

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Summary and future scope of work

In this PhD thesis work, an attempt was made to investigate the insulator-to-metal transition (IMT) phenomena in vanadium oxides (VO) thin-films, when subjected to a voltage stimuli. The VO were deposited by reactive rf-sputtering of a metallic target in different Ar/O_2 ratios. The material/physical properties of these films were probed by grazing incidence x-ray reflectivity (GI-XRR), differential scanning calorimetry (DSC), grazing incidence x-ray diffraction (GI-XRD) and x-ray photoelectron spectroscopy (XPS). The GI-XRD characterizations were performed using a synchrotron radiation-based x-ray source. The XPS unit was equipped with an *in-situ* substrate heating facility. In order to measure the electrical characteristics of these insulating VO, aluminium metal was deposited using electron beam evaporation. The metallic film was subsequently patterned into gate electrodes by UV-Photolithography technique, resulting in the overall metal-oxide-semiconductor (MOS) structure. All the process steps of MOS fabrication were performed at the class 1000 and class 100 grade clean room facility of Saha Institute of Nuclear Physics. The current-voltage ($I-V$ characteristics) and resistance-

temperature ($R-T$ characteristics) measurements were primarily investigated for signatures of IMT phenomena. The onset of IMT was either denoted by a sharp increase in current ($\sim 3/4$ orders of magnitude) at a critical threshold voltage in the $I-V$ characteristics or by a sudden fall in resistance at a critical temperature value in the $R-T$ measurements. Detailed studies were performed to investigate the effect of deposition conditions namely, oxygen content in the reactive plasma and amorphous-to-crystalline transition temperature (T_c) on the IMT properties. Moreover, the IMT of VO was also studied as a function of measurement temperature of the electrical probe station. The various physical characterization tools were employed to understand the underlining driving mechanisms of electrically triggered IMT (E-IMT). These E-IMT was chiefly attributed to voltage-induced Joule heating effect and strong electron correlations resulting in collapse of the band-gap. In addition, structural phase transition and a trade-off between various crystalline/amorphous phase mixtures of VO played an ancillary role. A direct correlation was also sought between the crystallization temperature of VO and the resulting IMT. In its totality, the primary objective in this thesis was to obtain a large magnitude of IMT, reduce the onset voltage of E-IMT and try to understand the driving mechanisms. Moreover, the physical properties of the VO were correlated with its IMT ptoperties.

The results of this thesis work are summarised in the following,

A major achievement of this thesis work is that the thickness of SiO_x interfacial layer(IL) could be reduced during the deposition of high-κ gate dielectric or oxide thin-films on silicon substrates via reactive rf-sputtering of a metallic target in different Ar/O_2 ratios. In general during deposition via reactive rf-sputtering, a low-κ SiO_x IL was formed at the high-κ/Si interface. This IL reduced the total

capacitance of the entire gate-dielectric/oxide stack and was detrimental to the device performance. In order to circumvent this problem, an improvisation was made in the deposition chamber of a sputtering unit. A copper grid was added co-axially with the substrate shutter. HfO_2 was reactively rf-sputtered from a metallic Hf target and the deposition occurred through the copper grid. Furthermore, increasing negative dc biases were applied to the copper grid during depositions. Using this instrumental modification, the thickness of SiO_x IL could be reduced from 3.5 nm to 0.6 nm, at a grid bias of -200 V. Furthermore, the accumulation capacitance improved from 26 pF to 114 pF and the dielectric constant of total oxide stack increased from 4.11 to 11.1.

The emphasis of the work was to investigate how the oxygen content in the Ar/O_2 plasma during sputter deposition at room temperature plays a role in achieving a reversible IMT of reactively sputter–deposited vanadium oxide (VO) thin-films where the electrical characteristics of the VO-based MOS devices were measured at room temperature. A qualitative and quantitative analysis of the various oxidation states of vanadium in the deposited films were performed using XPS. The study revealed that above a particular O_2 content in the Ar/O_2 plasma, the VO underwent a reversible IMT which was $\geq 60\%$ in this case. The voltage induced joule effect resulted in the formation of filamentary metallic conduction channel across an otherwise insulating VO. At low oxygen content, oxygen vacancies preserved the metallic nature of VO, when the applied voltage stress was reduced. Thus the IMT was irreversible at lower O_2 content in the plasma.

This work puts stress on effect of temperature dependent changes in different crystallographic orientations namely, monoclinic to orthorhombic on the IMT of VO films, deposited using sputtering at room temperature. The electrical mea-

surements were carried out at elevated substrate temperature ranges from room temperature (RT) to 200 °C as identified from the DSC scan. The GI-XRD was also carried out at a few discrete temperatures selected from the IMT data. A quantized IMT phenomenon at discrete measuring temperatures was observed and caused due to a trade-off between the crystalline and amorphous phase mixtures of VO. The IMT was initially triggered by an increase in carrier concentrations, resulting in a collapse of the band gap. Once the magnitude of current increased at the onset of IMT, Joule effect also contributed to the phenomena. Structural phase transition also played an ancillary role in contributing to the IMT.

The VO films were reactively sputter-deposited at elevated substrate temperatures, lying above their amorphous-to-crystalline transition temperature (T_C). The T_c was identified from the cooling cycle of the DSC scan and was found to increase with increasing O_2 content in the reactive plasma. The XPS studies indicated increasing concentrations of V^{4+} and O 1s (V^{4+}) states were responsible for large magnitudes of IMT at higher O_2 content in the plasma. For VOs deposited above T_C, crystallization caused an increase in grain size accompanied by a simultaneous reduction in the density of grain boundaries. These two cumulative effects contributed to a large and sharp IMT.

Future Scope of Work

One of the future directions of this thesis work would be to study how the residual stress in vanadium oxide thin-films contributes to its IMT properties. The residual stress may be estimated from synchrotron radiation-based GIXRD of the VO films.

The rise time for transition from the insulating to metallic state during IMT may be estimated by performing pulse-$I-V$ measurements of the VO-based MOS

devices. Having an idea of the rise time, one can better understand the exact underlining mechanism of IMT and determine whether Joule heating or strong electron correlations or both drive the IMT phenomena.

A model may be designed that simulates the electrically triggered insulator-to-metal transition (E-IMT) in oxides of vanadium using the various underlining driving mechanisms. This model would exemplify the physics of the IMT phenomena.

It has been long observed for VO_2, undergoing an IMT at $\sim 67\ ^{\circ}C$, that doping with certain metals raises/lowers its IMT temperature. This IMT was triggered in response to a thermal stimuli. However, the effect of metal-doping on the E-IMT phenomena in VO has not been investigated. It is expected that metal-dopants should affect the value of threshold voltage at the onset of E-IMT. A thorough and exhaustive study, establishing a direct relationship between doping and E-IMT, is thus required.

SYNOPSIS

Introduction: The scaling down of semiconductor devices to sub-10 nm dimensions is based on the application of electronic band theory. In the classical band theory, the electrons in a crystalline solid are treated as particles which move in an effective periodic potential, independent of other electrons. The above periodic potential arises from the lattice and other electrons of the solid. The overlap of atomic/molecular orbitals of each individual electrons leads to formation of electronic bands. Band formation finally leads to the delocalization of electrons. The bandwidth is related to the energy gain of the crystal as a result of electron delocalization or effectively, the electron's kinetic energy. Materials having partially filled orbitals also have partially filled bands which render them a metallic character. In case of metals, the Fermi energy lies within the band but the Fermi energy lies within the bandgap for insulators and semiconductors [1, 2]. The classical band theory renders a proper justification for the properties of many materials. However, it has been observed since 1937 that the classical approach to band theory fails to address the conduction and electrical properties of many transition metal oxides with partially filled d- and f- electronic orbitals. These compounds which were expected to be metallic on account of unfilled electron orbitals are actually insulating in nature. Moreover, these metal-oxides underwent phase transitions from the insulating to the metallic states [3].

The classical approach to band theory failed for the above transition metal oxides owing to the basic assumption that electrons move independently in the periodic lattice without interacting with the neighbouring electrons. As compared to s and p orbitals, d or f shells are more localized that in turn form narrower bands. Thus the electron correlations (or Coulomb repulsion) are stronger for the

d or f shells and the repulsion energy is comparable to the delocalization energy. In the year 1949, Mott proposed a theory, taking into account the electron-electron interactions and was able to explain the insulating states of transition metal oxides [4]. The term *Mott insulators* was used for referring to these materials. Not only the Mott materials exhibited insulating character, these compounds also underwent phase transitions with sharp change in their electrical or magnetic properties when subjected to external stimuli [5]. *Mott materials* was a terminology for referring to the materials with strong electron correlation that showed insulator-to-metal transitions (IMT). The IMTs are a result of a competition between electron localization due to electron correlation and delocalization due to band formation.

Transition metal oxides with partially filled *3d*, *4d* or *4f* orbitals are the classic examples of Mott insulators. The underlying mechanisms of IMT in these materials can be understood from the band-theory picture. As predicted by classical band theory, energy band forms from the overlap of atomic/molecular orbitals. The bandwidth W is directly related to the energy gain of the system from electron delocalization or electron's kinetic energy t. For gaining insights into the properties of Mott insulators, an important aspect needs to be taken into consideration: *electron-electron interactions*. As expected transition metal oxides should have partially filled *d*- and *f*- orbitals that in turn offer a metallic character. However, in such materials the Coulomb repulsion energy between electrons or *electron-correlation* (denoted by U) is stronger than the kinetic energy t. This hinders the delocalization of electrons to form bands within the lattice. The original partially filled electronic bands splits into one completely empty and one completely occupied bands thus rendering an insulating character to the material [1].

In the present thesis work, the IMT phenomena of oxides of vanadium were

investigated and the underlining driving mechanisms were understood. VO_2 undergoes a metal-to-insulator (MIT) transition at 340 K ($\sim$ 67 °C) accompanied by a sharp change in its resistivity by $\sim$ four orders of magnitude [25, 26]. VO_2, initially a semiconductor (optical bandgap $\sim$ 0.6 eV) near room temperature, changes to its metallic phase above $\sim$ 67 °C [2]. The MIT in VO_2 is a first-order phase transition [27]. The above MIT in VO_2 near 340 K is also accompanied by a structural phase transition (SPT) from the monoclinic insulating phase (*M1*) to a tetragonal (rutile) metallic phase (R). V_2O_3 also undergoes metal-to-insulator transition (MIT) triggered by changes in temperature, pressure or by doping with certain elements [31]. It undergoes a first-order transition at a temperature of 160 K and pressure of 1 atm from the high-temperature paramagnetic metallic to low-temperature antiferromagnetic insulating phase [32] wherein the resistivity changes by $\sim$ seven orders of magnitude. A change in the structural symmetry also occurs from the high-temperature rhombohedral phase to low-temperature monoclinic phase [32]. V_3O_5 exhibits an insulator-to-metal transition (IMT) at $\sim$ 430 K and also offers the highest IMT temperature (T_c) amongst the vanadium oxide family [41]. Besides VO_2, it is the only oxide of vanadium which displays IMT above room temperature [42]. V_2O_5 per se does not exhibit MIT. However a reduction of V_2O_5 to other oxides of vanadium of different stoichiometry under certain deposition and/or annealing conditions offers a metallic character of the oxides responsible for IMT [54].

The IMT in oxides of vanadium may be triggered by a thermal stimulus or upon the application of an electric field. For instance, VO_2 is driven to an insulating state in response to a temperature stimulus near $\sim$ 68 °C, resulting in $\sim$ *4-order change* in its resistivity [58]. The transition has been attributed to an increase in

electron concentrations and was confirmed by Hall-effect measurements [59]. VO_2 films also undergo an IMT when an electric field of $\sim 10^6$ V/m is applied across it [63]. Various electronic devices utilize the electrically triggered IMT (E−IMT) property for various applications such as neuromorphic computing [64], coupled oscillators [65] and steep-swing switches [65]. The driving mechanisms of E−IMT have been ascribed to either a voltage induced Joule Heating effect model [66] or band gap collapse caused by strong electron correlations [58]. In the remainder of synopsis, the effects of these competing mechanisms have been discussed in detail.

Experimental details: In this thesis work the deposition, material characterizations, fabrication and characterization in thin-film of high-κ dielectric-based metal-oxide-semiconductor (MOS) structures have been discussed. The high-κ dielectric thin-films are reactively rf-sputter deposited on Si(100) substrates. The as-deposited films were then physically characterized using differential scanning calorimetry (DSC), lab-source based grazing incidence x-ray reflectivity (GI-XRR) and x-ray photoelectron spectroscopy (XPS). Synchrotron radiation (SR) based grazing incidence x-ray diffraction (GI-XRD) and x-ray photoelectron spectroscopy (XPS) were also used for characterizing the deposited films at the Indian synchrotron source Indus-2, Raja Ramanna Centre for Advanced Technology-Indore. Since the deposited films possess insulating character, aluminium metal was deposited by electron-beam deposition and subsequently patterned into gate electrodes by UV-Photolithography for performing various electrical measurements. The gate current corresponding to gate voltage sweep ($I - V$ characteristics), capacitance-voltage ($C - V$ characteristics) and resistance-temperature ($R - T$ characteristics) measurements were performed on the MOS devices. The thesis is organized in the following order.

The first chapter presents an **Introduction and Literature Survey** about metal-insulator transitions in transition metal oxides. The failure of classical band theory in explaining the insulating properties of transition metal compounds having partially filled d-orbitals is presented. The importance of strong electron correlations in Mott materials is mentioned. A literature survey about Mott insulators and the main underlining mechanisms of IMT are discussed. The IMT observed in various oxides of transition metals such as Titanium and Iron are discussed. Since the research activities presented in the thesis is based on the IMT phenomena of vanadium oxides, emphasis has been put here on oxides of vanadium. Recent works in this field have been highlighted. The motivation behind the work undertaken in this thesis has also been discussed.

The second chapter entitled **Theory of MOS devices** encompasses the physics of MOS devices [78, 79]. The band diagrams of MOS capacitors on n-type and p-type substrates are elucidated and discussed. The application of a voltage bias to the metallic electrode leads to either the *accumulation* or *depletion* or *inversion* regions at the semiconducting surface. These phenomena have been elaborately discussed for a better understanding of MOS devices. The concepts of *ideal threshold voltage* and *flatband voltage* have been further highlighted [84]. The capacitance-voltage ($C-V$) characteristics are discussed at length. The various kinds of oxide and interface traps are mentioned [86]. The current-voltage ($I-V$) characteristics of MOS capacitors are explained. The conduction mechanisms namely, Fowler-Nordheim ($F-N$) tunnelling [79], Direct tunnelling and Poole-Frenkel ($P-F$) emission [75] are also illustrated.

The third chapter entitled **Experimental Details** deals with the instrumental techniques used for depositing high-κ dielectric thin-films. The various physical

characterization tools used for the material characterization of the films are also mentioned in detail. The entire process flow entailed in the fabrication of MOS capacitors based on the deposited films has been illustrated. The basic underlining principles behind the working of all experimental setup are highlighted followed by a brief overview of the operational procedures. In the entire thesis work the films were reactively rf-sputter deposited on Si(100) substrates. Aluminium metal was evaporated on the films using electron beam evaporation and patterned into gate electrodes by the UV-Photolithography technique. The physical characterizations were done using either lab source based x-rays or a synchrotron source. The Indus-2 beamlines stationed at Raja Ramanna Centre for Advanced Technology Indore, India were used for material characterization of the samples.

The fourth chapter, **Control of interfacial layer growth during deposition of high-κ oxide thin-films in reactive RF-sputtering system**, describes an improvisation of an existing reactive rf-sputtering system for the deposition of high-κ dielectric/oxide thin-films from metallic sputtering targets in Ar/O_2 plasma. A common problem associated with the deposition of high-κ dielectric/oxide-films via reactive sputtering is the formation of low-κ SiO_x interfacial layer (IL) at the oxide/silicon interface [105, 106]. This IL reduces the overall capacitance of the gate-dielectric stack and hinders scaling down of the effective-oxide-thickness (EOT) to sub-nm dimensions [110]. This problem is circumvented by an added instrumental modification to the deposition chamber of a sputtering system. The analysis of x-ray reflectivity data suggests that the IL thickness could be restricted to ~ 0.6 nm in the modified sputtering unit. Furthermore, the accumulation capacitance (as estimated from the $C-V$ characteristics) increases with decreasing IL thickness suggesting an improvement of the device performance. Thus the electri-

cal characteristics of the MOS devices based on reactively sputter-deposited oxide thin-films shows a drastic improvement with the added instrumental modification as outlined in this chapter.

The fifth chapter, **Effect of oxygen content on the electrical properties of sputter deposited vanadium oxide thin-films**, describes the role of oxygen content in the Ar/O_2 plasma in determining the electrical properties of reactively sputter-deposited vanadium oxide films on Si(100) substrates. The depositions were performed at room temperatures. The oxide films were probed using laboratory source-based x-ray photoelectron spectroscopy for identifying the various constituent oxide phases of vanadium. The oxidation states of vanadium were identified with respect to oxygen peak and the contents of different oxidation states of vanadium and O 1s states of oxygen in the films are determined by deconvoluting the XPS using CasaXPS software. The $I-V$ characteristics reveal that the films deposited at the highest oxygen content offers insulator-to-metal transition (IMT) property. The IMT has been described by a voltage-induced Joule heating model which results in the formation of a localized filamentary metallic conduction channel within an otherwise insulating oxide layer [66, 70]. This study implies that the Ar/O_2 ratios play a critical role in governing the IMT of vanadium oxide films.

The sixth chapter of the thesis, **Insulator-to-metal transition of vanadium oxide-based metal-oxide-semiconductor devices at discrete measuring temperatures**, highlights the role of measuring temperatures in governing the IMT properties of vanadium oxide based MOS devices. The films were deposited in different Ar/O_2 ratios at room temperature. However, the $I-V$ characteristics were measured at elevated substrate temperatures. The various oxide phases of vanadium were identified by differential scanning calorimetry (DSC) and

synchrotron-based grazing incidence x-ray diffraction (GI-XRD). An amorphous to crystalline phase transition with increasing oxygen content in the reactive plasma is observed. The underlining mechanisms of IMT have been attributed to both electric-field induced carrier injection [180] as well as structural phase transitions. Joule heating also plays an effective role [71]. The IMT is absent at intermediate measuring temperatures due to the presence of crystalline and amorphous phase mixtures.

In the seventh chapter, **the effect of oxygen content and crystallization temperature on the insulator-to-metal transition properties of reactively sputter deposited vanadium oxide films** is studied. The crystallization temperatures of vanadium oxides (VOs) deposited at various Ar/O_2 ratios are identified by differential scanning calorimetry (DSC) technique and accordingly, the deposition temperatures were set at above their respective crystallization temperatures. The DSC study further reveals that amorphous-to-crystalline transition temperature (T_c) increases with the increase in pO_2 in the plasma. $I-V$ studies reveal ~ 4 order IMT for the devices with VO deposited at 60% pO_2. An abrupt change in resistance is observed in the $40-50$ °C temperature range for vanadium oxide samples deposited at 40% pO_2 in Ar/O_2 plasma and at higher deposition temperatures. The grain/crystallite size increases with an increase in deposition temperatures accompanied by a simultaneous reduction in the density of grain boundaries. This in turn leads to an enhancement in the magnitude of IMT with the increase in deposition temperatures.

The final chapter presents a brief summary and future scope of the current thesis work.

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1

Introduction and Literature Survey

1.1 Metals, Semiconductors and Insulators

The miniaturization of semiconductor-based devices to sub-10 nm dimensions is relied upon the application of electronic band theory. In the classical band theory, the electrons in a crystalline solid is treated as particles moving in an effective periodic potential. This periodic potential is due to the lattice and other electrons in the material. The electrons, being treated here as particles move independently of other electrons. The overlap of atomic or molecular orbitals leads to electronic bands which in turn causes delocalization of electrons. The bandwidth is related to the energy gain of the crystal as a result of electron delocalization or effectively, the electron's kinetic energy. Materials having partially filled orbitals in turn have partially filled bands resulting in a metallic character. In case of metals, the Fermi energy lies within the band but the Fermi energy lies within the bandgap for insulators and semiconductors [1, 2]. The classical band theory renders a proper justification for the properties of many materials. However, since 1937, an anomaly

arose that the classical approach to band theory failed to address the conduction and electrical properties of many transition metal oxides with a partially filled d- and f- electron bands. These compounds, expected to be metallic on account of unfilled electron orbitals, were actually insulating or underwent phase transitions from the insulating to the metallic states [3].

The above failure of the classical band theory arises due to the underlying assumption that electrons move independently across the periodic lattice without interacting with the neighbouring electrons. As compared to s and p orbitals, d or f shells are more localized on the atoms and thus form narrower bands. Thus the electron correlations (or Coulomb repulsion) are stronger for the d or f shells and the repulsion energy is comparable to the delocalization energy. In the year 1949, Mott proposed a theory, with due consideration to the electron-electron interactions and was able to explain the insulating states of transition metal oxides [4]. The term *Mott insulators* was later coined for referring to these materials. Later it was known that besides displaying insulating character, these materials underwent phase transitions with sharp change in their electrical or magnetic properties when subjected to external stimuli [5]. *Mott materials* was a terminology for referring to the materials with strong electron correlation that showed insulator-to-metal (IM) transitions. Thus IM transition arises as a result of a competition between electron localization due to electron correlation and delocalization due to band formation.

1.2 Classification of Insulators

The discussion in the previous section referred to a class of insulators where metal-to-insulator transition(MIT) arises due to strong electron correlations. However, in addition to the Mott theory which considers electron-electron interactions, the

metal-insulator transition may also occur due to other interactions within the crystal lattice. The insulators are thus categorized in the following [6],

1.2.1 Bloch-Wilson insulator

An insulator which falls within the framework of classical band theory without considering electron-electron interactions is called a band insulator or Bloch-Wilson insulator. The insulators within this category include diamond and common undoped semiconductors. In 1931, Wilson proposed that a metal-to-insulator transition (MIT) can occur when volume or composition of the system was changed [7]. In a crystalline insulator with all bands filled or empty, the band gap is indirect. Upon decreasing the volume, the gap shrinks to zero and changes sign rendering a metallic character to the material with partially filled bands [8]. This kind of transition is found in Ytterbium upon application of an external pressure [9].

1.2.2 Mott-Hubbard insulator

Mott theorised a model for MIT which considered electron-electron interactions [4]. As per Mott's theory there exists a critical carrier density n_c such that ${n_c}^{1/3}\ a_H \sim 0.2$, where a_H is Bohr radius of the respective material. Once the electron carrier density in the material crosses n_c, a phase transition takes place due to strong electron-electron interaction (also known as electron correlation). This kind of carrier-induced MIT is referred to as the Mott MIT or Mott-Hubbard MIT and accordingly, the insulators are referred as Mott-Hubbard insulator [6]. Oxides of vanadium like VO_2 and V_2O_3 are archetypes of Mott-Hubbard insulator.

1.2.3 Peierls insulator

A MIT may also occur owing to electron-phonon or electron-lattice interaction, referred to as Peierls MIT [10]. A lattice structural change induces a lattice deformation which in turn modifies the periodic lattice potential of the material. A corresponding change in the band-structure of the material results in a MIT. $K_{0.3}MoO_3$ undergoes a Peierls MIT at 181 K exemplified by a conductivity change which is simultaneously associated with a structural change [11].

1.2.4 Anderson insulator

Anderson MIT is a result of electron localization effect owing to disorder in the system [12]. Anderson observed that randomly distributed lattice defects results in a insulating state in such materials. The disorder-induced electron localizations give rise to a mobility edge, separating the localized and delocalized states in the bands. Insulating states are formed when the Fermi energy level lies between a band edge and its mobility edge. This kind of MIT is prevalent in strongly disordered materials and compounds with strong impurity scattering. Heavily doped semiconductors like Si:P fall within this category of insulators [6].

1.3 Metal-to-insulator transition(MIT) mechanism in Mott insulators

Transition metal oxides with partially filled *3d*, *4d* or *4f* orbitals are the classic examples of Mott insulators. The underlying mechanisms of MIT in these materials can be understood from the band-theory picture. As predicted by classical band

theory, energy band forms from the overlap of atomic/molecular orbitals. The bandwidth W is directly related to the energy gain of the system from electron delocalization or electron's kinetic energy t. For gaining insights into the properties of Mott insulators, an important aspect needs to be taken into consideration: *electron-electron interactions*. As expected, transition metal oxides should have partially filled *d*- and *f*- bands that in turn offer a metallic character. However, in such materials the Coulomb repulsion energy between electrons or *electron-correlation* (denoted by U) is stronger than the kinetic energy t. This hinders the delocalization of electrons to form bands within the lattice. The original partially filled electronic bands splits into one completely empty and one completely occupied bands thus rendering an insulating character to the material.

The transition between the insulating and metallic states of Mott insulators is driven by a competition between electron localization and delocalization. The bandwidth W or the magnitude of delocalization energy t can be modulated that in turn induces a MIT. For instance, an external stress applied to the system decreases the lattice parameter and increases W thereby, causing a MIT. This phenomenon is termed as *bandwidth-controlled MIT* where decreasing the interatomic distance increases the electronic band-width and delocalization energy t resulting in an insulator-to-metal transition for $t > U$. In other way round, the effective U between electrons can be adjusted. On the addition of electrons/holes into the lattice, the energy cost for hopping is reduced for certain electrons which effectively reduces the Coulomb repulsion energy U. The added electrons screen the electron-electron interaction and reduce U. This carrier induced phase transition is referred to as *filling controlled MIT*.

Thus for Mott insulators, the originally partially filled band splits into occupied

and unoccupied bands due to electron correlation and the Fermi energy lies in the bandgap. Upon increasing the bandwidth W or incorporation of carriers the bandgap collapses [1], thus driving a transition from insulating to metallic states. A schematic of band width controlled and filling controlled MIT is illustrated in Figure 1.1.

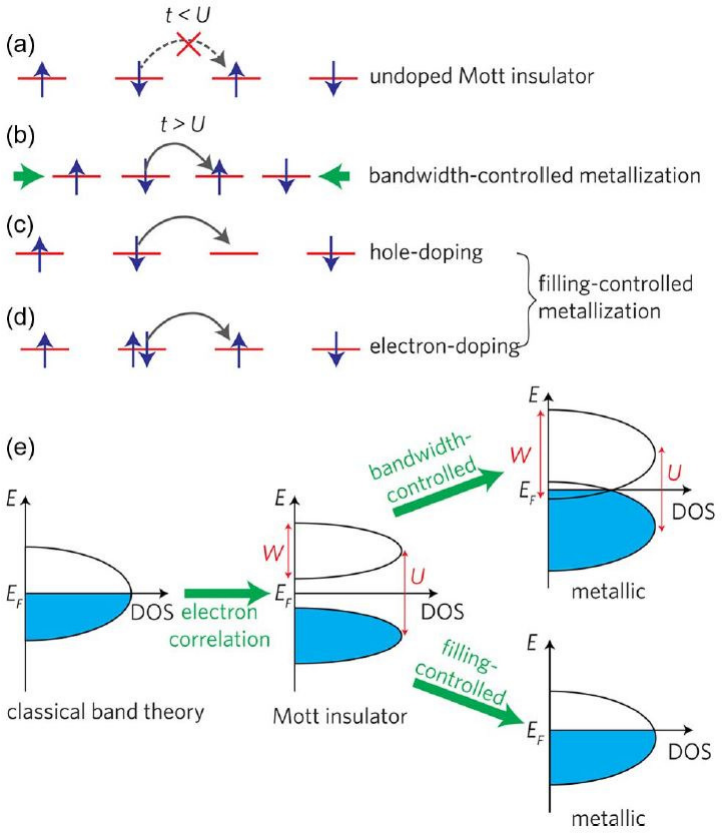

Figure 1.1: Metal-to-Insulator transition mechanisms in Mott-insulators. Taken from Ref. [1].

The above Mott transitions are purely electronic phenomena and discard other interactions of the crystal lattice. Nevertheless, energy of many interactions is of the same order of magnitude with electron-electron correlation U and kinetic energy t and becomes equally relevant in giving rise to a material's electronic prop-

erties. These include electron-lattice, spin-spin and various other interactions. The coupling of these interactions leads to a fascinating observation namely, *Electronic phase transitions in transition metal oxides are accompanied by structural and other types of transition.* For instance, VO_2 undergoes a resistivity change by four orders of magnitude at a temperature of 67 °C, accompanied with a structural change from a monoclinic insulating phase (*M1*) to a tetragonal (rutile structure) metallic phase (R) [13].

1.4 MIT in Transition metal oxides/compounds

This section illustrates the MIT phenomenon in some of the oxides/compounds of transition metals.

1.4.1 Titanium

Titanium sesquioxide (Ti_2O_3) in the corundum crystal undergoes a MIT in the temperature range of 400-600 K [14]. However the MIT is not accompanied by any structural phase change [15] or any magnetic ordering [16]. Ti_2O_3 possesses a direct band gap of ~ 0.1 eV close to room temperatures. The low temperature phase is a non-magnetic insulator. Yan *et al.* have attributed the MIT to alterations of the unit cell parameters of the crystal which eventually increases the c/a ratio [17].

1.4.2 Nickel

Nickel chalcogenide ($NiS_{2-x}Se_x$) exhibits MIT and magnetic phase transition when its composition is varied or upon application of temperature and pressure [18]. MIT due to a change in composition falls within the bandwidth-control type where the

ratio of intra-atomic Coulomb repulsion to the bandwidth (U/W) plays the decisive role [19]. NiS_2 has been regarded as a Mott insulator where transitions to a metallic phase takes place upon application of pressures exceeding ~ 3.5 GPa or by doping with Se atoms in the S lattice sites [20].

1.4.3 Lanthanum and Strontium

Lanthanum Titanate ($LaTiO_3$) is a Mott insulator whereas Strontium Titanate ($SrTiO_3$) is a band insulator. However, epitaxial $LaTiO_3$ films deposited on $SrTiO_3$ substrates exhibits a metallic character at the Mott insulator/band insulator interface [21]. This metallic character at the heterointerface is due to the transfer of localized electrons from the Mott insulator to the band insulator [22]. Epitaxial strain at the interface also causes an electronic structural modification that gives rise to a metallic state.

1.4.4 Iron

Verwey in the year 1939 reported a MIT in bulk Fe_3O_4 wherein a transformation from a metallic phase to an insulating state takes place when the temperature is reduced below 123 K [23]. This temperature is now popularly known as the Verwey transition temperature (T_v). The transition has been attributed to a charge ordering of Fe^{2+} and Fe^{3+} ions in the octahedral sites. Below T_v, localized electrons are distributed amongst three Fe sites called trimerons [24].

1.5 MIT in oxides of Vanadium

1.5.1 VO_2

The widely studied oxide of vanadium oxide is VO_2 which undergoes a metal-to-insulator (MIT) transition at 340 K ($\sim 67\,^{\circ}$C) evidenced by a sharp change in its resistivity by upto four orders of magnitude [25, 26]. The proximity of the transition temperature close to room temperature makes it an ideal candidate for integration into phase change based memory devices. VO_2, initially a semiconductor (optical bandgap ~ 0.6 eV) near room temperature, changes to its metallic phase above $\sim 67\,^{\circ}$C [2]. The MIT in VO_2 is a first-order phase transition [27]. While measuring the resistivity of VO_2 with increasing temperatures (heating cycle) a sharp fall in resistivity occurs near 340 K denoting the onset of metallic-phase. The resistivity switches to a higher value (insulating state) for resistivity measurements with respect to decreasing temperatures in the cooling cycle. It is noteworthy to mention that the transition temperature is lower as compared to the heating cycle. This renders an overall hysteresis to the *Resistivity vs Temperature* measurements after a complete cycle [28] as illustrated in Figure 1.2.

The above MIT in VO_2 near 340 K is also accompanied by a structural phase transition from the monoclinic insulating phase (*M1*) to a tetragonal (rutile) metallic phase (R). The *M1* insulating phase has a symmetry of the $P2_1/c$ space group whereas the metallic R phase belongs to the $P4_2/mnm$ space group [29]. During transition from the rutile to monoclinic phase, a displacement of the vanadium atoms out of the octahedral planes occurs. Subsequently, these atoms are paired with each other such that the V-V bond is tilted with respect to the octahedral planes in the rutile phase.

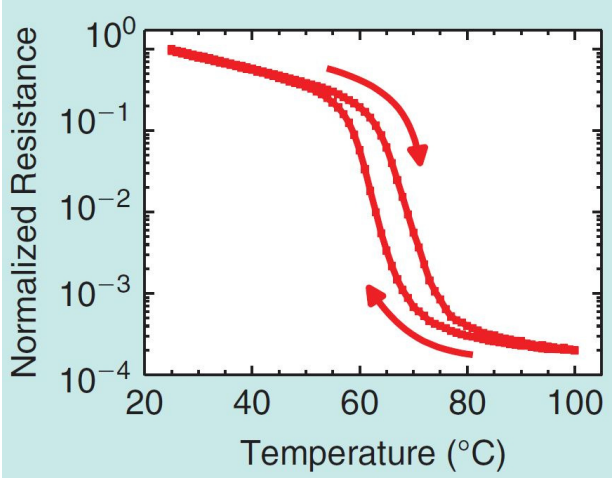

Figure 1.2: Normalized resistance as a function of temperature for VO_2 thin film. Taken from Ref. [2].

The electronic band structure of VO_2 changes during transition from the insulating to metallic phase [14]. In the metallic rutile phase, the t_{2g} levels split respectively into $d_{\|}$ and π^* bands under the octahedral crystal field. These two energy bands overlap and consist of electronic states near the Fermi energy of metallic state. The $d_{\|}$ levels are non-bonding whereas π^* hybridises with the O *2p* π, lying at higher level relative to the $d_{\|}$ level. Both the bands are partially filled and thus VO_2 offers a metallic character. When MIT takes place, VO_2 transforms to the monoclinic structure where the V-V pairing (vanadium atoms dimerization) occurs followed by a tilt of the paired atoms along the rutile c axis. Consequently, *3d-2p* hybridization splits the $d_{\|}$ energy band into bonding state and anti-bonding state. The π^* band is upshifted off the Fermi energy level [1]. The above reasoning for accounting MIT in VO_2 does not take electron-correlation into account and is referred to as the Goodenough picture [29]. Mott introduced electron correlation for explaining the MIT [30]. He proposed that the structural change in VO_2 upshifts and depopulates the π^* band. The resulting free carriers lead to less

screening of electron correlation in the $d_{\|}$ band. Subsequently, the $d_{\|}$ band splits into upper and lower Hubbard bands in turn triggering the transition. Thus it becomes apparent that the purely-electronic Mott transition and the structural phase transition work in conjugation for driving the MIT. The simultaneous reduction in effective electron correlation (from Mott transition) and decrease in bandwidth (from structural change) drive the MIT in VO_2. The mechanism of MIT in VO_2 is illustrated in Figure 1.3.

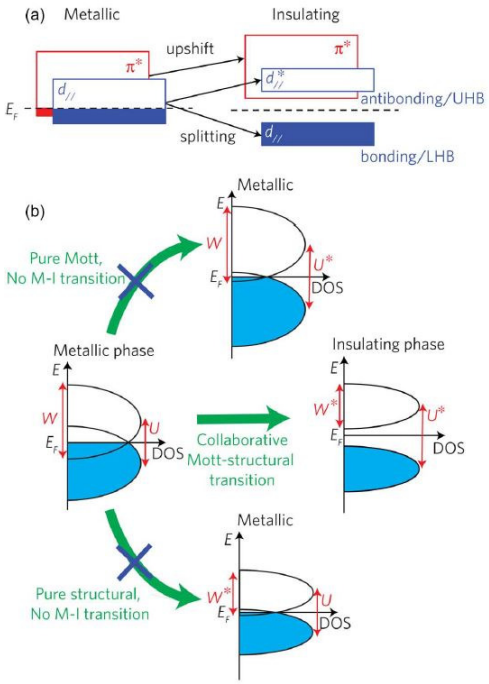

Figure 1.3: Mechanism of MIT in VO_2. Taken from Ref. [1].

The above discussion on electronic band structure opens very important question for discussion : *To what degree the purely-electronic Mott transition and the structural phase transition (SPT) are coupled ? Does the Mott transition in turn trigger SPT or does an SPT precede the Mott transition ?* An attempt has been made to address these questions in the following chapters/subsections.

1.5.2 V_2O_3

Vanadium sesquioxide (V_2O_3) is known to undergo metal-to-insulator(MIT) transitions which can be brought about by changes in temperature, pressure or by doping with certain elements [31]. It undergoes a first-order transition at a temperature of 160 K and pressure of 1 atm from the high-temperature paramagnetic metallic to low-temperature antiferromagnetic insulating phase [32] wherein the resistivity changes by upto seven orders of magnitude. A change in the structural symmetry also occurs from the high-temperature rhombohedral phase (belonging to $R\bar{3}c$ space group) to low-temperature monoclinic phase (belonging to I2/a space group) [32]. V_2O_3 also undergoes a second-order phase transition from a metallic to semiconducting state at about 500 K [33]. A MIT accompanied by a structural phase transition might suggest a Peierls transition [10]. However, upon doping with chromium $(V_{1-x}Cr_x)_2O_3$ shows a transition from paramagnetic metal to a paramagnetic insulator without any change in the corundum crystal symmetry ($R\bar{3}c$) at room temperature conditions [33]. This indicates a Mott-Hubbard transition solely based on electron-correlations [34]. The paramagnetic ordering of Cr doped V_2O_3 is preserved across the MIT at room temperature. Only when the temperature is lowered below 180 K, a change in magnetic ordering takes place resulting in the formation of an antiferromagnetic monoclinic phase. Generally, doping with Ti stabilizes the paramagnetic metallic phase of V_2O_3 whereas upon Cr doping the paramagnetic insulating phase is stable, preserving the corundum crystal structure [35, 36]. The complex temperature vs doping phase diagram of V_2O_3 is illustrated in the Figure 1.4 [35, 37].

The phase transition in Ti- or Cr-doped V_2O_3 was explained by Lechermann *et al.* [36]. V^{3+} having $3d^2$ electronic configuration occupies the t_{2g} orbitals which

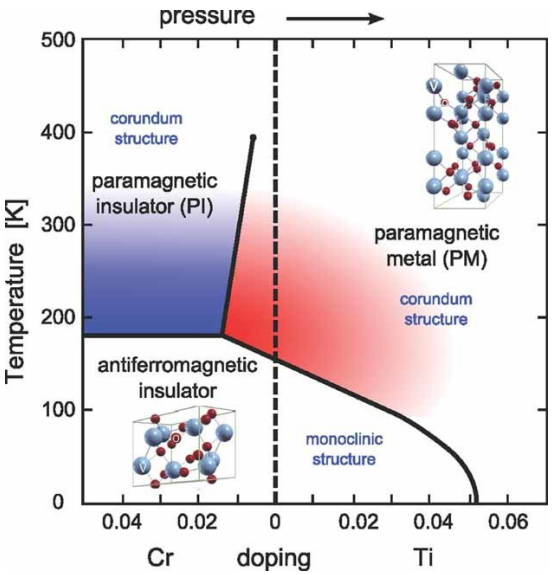

Figure 1.4: Phase diagram of V_2O_3. Taken from Ref. [35, 37].

are triply degenerate. Under the crystal field of the corundum structure, the t_{2g} orbitals split into a lower ${e^{\pi}}_g$ doublet state and a higher a_{1g} singlet state. In the Ti-doped V_2O_3, the t_{2g} states of Ti lie higher than those of V. This results in loss of electrons of Ti and doping of the corresponding V bands. Thus in a $(V_{1-x}Ti_x)_2O_3$, the originally V_2O_3 oxide is now doped with *x/1-x* electrons. The addition of electrons to the Mott-insulator leads to its metallization. On the other hand, Cr-doping as in $(V_{1-x}Cr_x)_2O_3$ causes a structural distortion which stabilizes the insulating behaviour.

As mentioned previously, pure V_2O_3 undergoes a MIT accompanied simultaneously by a structural symmetry transition at 160 K. Recently, Majid *et al.* deposited strained V_2O_3 film on [001] Si using pulsed laser deposition technique [38]. The inherent stress present in the deposited films lowered the electronic MIT temperature to $\sim$ 122 K whereas the structural transition occurred at $\sim$ 145 K. V_2O_3 existed in a monoclinic metallic phase in the temperature ranges from 122 K to 145 K. The decoupling of the structural transition temperature from the

MIT temperature gives more relevance to the electron correlation effects of the Mott-Hubbard model over the Peierls model.

Valmianski *et al.* studied the role of pressure in affecting the MIT in V_2O_3 thin-films of various thickness deposited on Al_2O_3 substrates. Keeping at room temperature, the thin-films were subjected to increasing pressures from 1 atm to 1.5 GPa [39]. Resistivity measurements as a function of temperature sweep were performed. It was found that below 500 MPa the MIT temperature is lowered as compared to bulk V_2O_3. At pressures more than 500 MPa, the transition temperature of V_2O_3 thin-films resembled that of bulk. The transition also shows sharp dependence on the film thickness and orientation.

1.5.3 V_3O_5

Owing to the multivalent character of vanadium, it exists in a variety of oxide forms. The Magnéli phases with the V_nO_{2n-1} composition (for n=3,4,.....9), have attracted quite an attention [40]. The first member of this series is V_3O_5 which exhibits an insulator-to-metal transition(IMT) at $\sim$ 430 K and offers the highest IMT temperature (T_c) amongst the vanadium oxides family [41]. Besides VO_2, it is the only other oxide of vanadium which displays IMT above room temperature [42]. As opposed to MIT in VO_2 where a sharp transition at 340 K marked by a resistivity change of upto *four-orders* of magnitude occurs, the IMT in V_3O_5 is far less pronounced. Resistivity measurements with respect to temperature in both bulk single crystals [43] and thin-films [44] of V_3O_5 reveal that the resistivity changes only by a factor of 20 at T_c without any measurable hysteresis after a heating-cooling cycle. Moreover, the transition from the insulating to metallic phase is not a sharp descent in resistivity at a particular temperature but spans

over a broad range from 395 K to 465 K [44]. Nevertheless, the IMT of V_3O_5 has several advantages over VO_2. In complementary metal-oxide-semiconductor (CMOS)-based devices, miniaturization of device dimensions leads to an inadvertent increase in junction temperatures [45]. Thus resistive switching-based devices, incorporating the IMT of VO_2 would mandate the cooling of devices in order to prevent thermally induced transition. As the T_c of V_3O_5 is much higher compared to VO_2 and it could sustain the higher junction temperature, V_3O_5 can act as an alternative gate dielectric in CMOS devices. Moreover, the SPT associated with IMT in VO_2 leads to a significant change in its lattice volume and symmetry that in turn generates mechanical stress that may damage VO_2-based devices after a couple of repetitive cycles across T_c [46]. The structural change associated with V_3O_5 is minimal and thus it may replace VO_2 in such devices. V_3O_5 is a paramagnetic insulator and the magnetic ordering changes to anti-ferromagnetism only when the temperature is reduced below 75 K. Thus the IMT in V_3O_5 is completely decoupled from a magnetic phase transition [47].

At temperatures below T_c, V_3O_5 has a monoclinic symmetry (belonging to $P2/c$ space group) having four formula units per unit cell [48]. Across the transition temperature, V_3O_5 retains its monoclinic structure with only small changes in the lattice parameter. However, the monoclinic phase now belongs to the more symmetric $I2/c$ space group as revealed by x-ray diffraction(XRD) studies [44]. The IMT of V_3O_5 might be suggestive of a first-order phase transition but the change in lattice parameters along with resistivity values spans a broad temperature spectrum. These characteristics are an indication of order-disorder (second-order) phase transition [42].

Electron correlations play a vital role in stabilizing the insulating phase of V_3O_5.

However, the underlying mechanism behind its IMT is not a pure Mott-Hubbard transition [49]. In the monoclinic symmetry of V_3O_5, oxygen octahedra arrange around the vanadium atoms. While in the insulating state, the unit cell comprises of two different V-O octahedra which split into four independent octahedrons, known as V(11), V(12), V(21) and V(22), respectively [50]. The V(11) site contains a V^{4+} ion while the rest of V(12), V(21) and V(22) contain the V^{3+} ions. The V(1) octahedra can contain V^{4+}/V^{3+} ions (a mixed valence state of 3.5) while the V(2) octahedra only consists of V^{3+} ions. The IMT is triggered by changing the spatial ordering of the V^{4+} and V^{3+} ions [49].

Baldassare *et al.* showed the dependence of IMT in V_3O_5 as a function of temperature and pressure [47]. The T_c of IMT is continuously decreased upon the application of increasing hydrostatic pressure to V_3O_5 single crystals. Moreover, the IMT took place at room temperature when the applied pressure reached $\sim$ 6 GPa. On further application of pressure beyond 6 GPa, the T_c can be further reduced down to 4 K. Beyond a pressure value of 9 GPa, the resistivity measurements show no trace of an IMT and V_3O_5 gains the metallic character [51]. The insulating and metallic states of V_3O_5 with respect to temperature and applied pressure are represented in the Figure 1.5 [47, 51].

The IMT in V_3O_5 can also be triggered electrically as evident from DC $I-V$ characteristics measured for polycrystalline samples [41]. Application of high-currents resulted in excessive heating of the samples owing to which the samples switched to a metallic character.

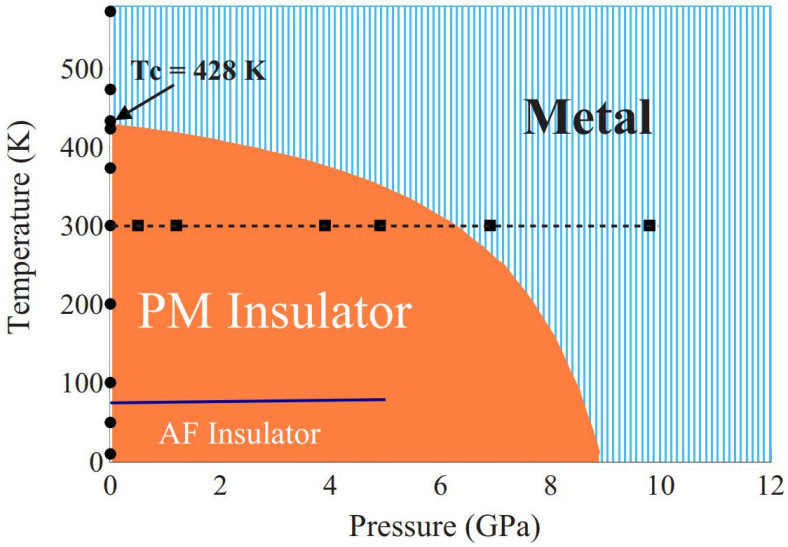

Figure 1.5: Pressure vs Temperature phase diagram of V_3O_5. Taken from Ref. [47, 51].

1.5.4 V_2O_5

Metal-insulator transitions in bulk V_2O_5 are not reported. However, Blum *et al.* reported a reversible MIT in the 350-400 K temperature range for V_2O_5 (001) single crystal surface [52]. The single crystals were heated from room temperature to 800 K and characterized by scanning tunnelling microscopy (STM) combined with scanning tunnelling spectroscopy (STS). It was revealed that the MIT was a result of restructuring in the surface layers of the crystals since the bulk did not show any signs of MIT. During the heating process, the oxygen atoms of the vanadyl (V=O) bond were removed from the surface layers resulting in oxygen vacancies. In these scenario, the surface V_2O_5 rearranges itself into V_6O_{13} without much atomic displacement. It is well reported that V_6O_{13} has a metallic character at temperatures above 150 K [53]. For further elevated temperatures until 800 K, V_6O_{13} reduces itself to V_2O_3. Thus the reported MIT by Blum *et al.* was

driven by oxygen vacancies from the vanadyl bond at the surface layers followed by restructuring and reduction from $V_2O_5(001) \rightarrow V_6O_{13}(001) \rightarrow V_2O_3(0001)$.

It is quite apparent from the above that V_2O_5 inherently does not exhibit MIT. However a phase change from V_2O_5 to other oxides of vanadium, having a different composition/stoichiometry and a metallic character, can trigger an MIT [54]. For instance, Lu *et al.* obtained a phase change-based MIT in vanadium oxide thin-films by reversible phase transitions between $VO_2 \leftrightarrow V_2O_5$ upon application of an electrochemical bias [55]. They surveyed that as the band gap of VO_2 (*M1*) monoclinic insulating phase is low (~ 0.6 eV), the ON/OFF ratio of the resistivity change is limited to $\sim 10^3$ in VO_2 thin-film based devices [56]. Moreover, as discussed earlier owing to the T_c of MIT in VO_2 being close to room temperature, the temperature regime for operating the VO_2-based devices is limited. These requires cooling of the devices so that the operation temperatures remain below T_c. On the other hand, V_2O_5 is an insulator having a wide band gap (~ 2.2 eV) [57]. By varying the oxygen content of the deposited films, a MIT-based phase change between VO_2 (*metallic*) $\leftrightarrow$ V_2O_5 (*insulator*) resulted in higher ON/OFF resistivity ratios and a wider operating temperature range.

1.6 Temperature induced insulator-to-metal transition(IMT)

It is widely reported that VO_2 exhibits an IMT in response to a temperature stimulus near ~ 68 °C, resulting in upto *4-order change* in its resistivity [58]. Ruzmetov *et al.* have attributed this sharp change in resistivity to the increase in electron concentrations at the onset of MIT as confirmed by Hall-effect measurements [59].

Moreover, the optical band gap collapses during the IMT phenomena [60, 61]. The detailed mechanisms underlining the transition phenomena owing to band gap collapse is still not completely understood. It has been construed that an impurity band comprising mostly of thermally activated carriers contributes to the IMT phenomena [58]. Oxygen defects also cause additional doping in vanadium oxide. The actual concentration of carriers is dependent on firstly, the magnitude of doping and secondly, on the activation energy of carriers comprising the impurity band.

1.7 Electrically induced IMT(E-IMT)

Electrically triggered insulator-to-metal transitions(E-IMT) describes a subset where the transition in vanadium oxides from an insulating to metallic character is brought about by an applied voltage stress or current. No external thermal stimuli in the form of change in temperature is applied to the material [62]. It has been reported that VO_2 thin-films undergo an IMT under the application of electric field$\sim 10^6$ V/m [63]. E-IMT phenomenon has been recently integrated into device structures for various applications namely, neuromorphic computing [64], coupled oscillators [65], memory selectors [58] and steep-swing switches [65] etc. The current-voltage characteristics $(I-V)$ in an E-IMT phenomenon is illustrated in Figure [1]. The I-V characteristics are linear below a threshold voltage V_{Th} and denote the insulating regime of VO. This region of the $I-V$ curve is known as OFF state of the device. Once the applied voltage stress reaches the value of V_{Th}, a sharp jump in current occurs where its magnitude changes by three to four orders. The sudden transition of current signifies that the resistance is reduced sharply and the device is turned ON to a metallic state. On further increase in

applied voltage, the $I-V$ characteristics again follow a linear trend and a metallic state of the device is achieved. On reducing the applied voltage the device switches back to an insulating state at a lower threshold voltage value of V_{Th}^{*}. Thus after a complete gate voltage sweep cycle a hysteresis in the $I-V$ characteristics is observed [1]. E-IMT can also be triggered by a current source whereby a current-controlled negative differential resistance occurs at a threshold current I_{Th}. The key aspect for incorporating E-IMT phenomena in device applications lies in achieving a large and steep ON/OFF ratio at low operating voltages [62]. A sharp transition where the magnitude of current changes by *3 to 4* orders is desirable. The underlining driving mechanisms of E-IMT have been chiefly attributed to either a voltage-induced Joule Heating effect model [66] or band-gap collapse owing to strong electron correlations [58]. These two mechanisms are briefly discussed in the subsequent sections.

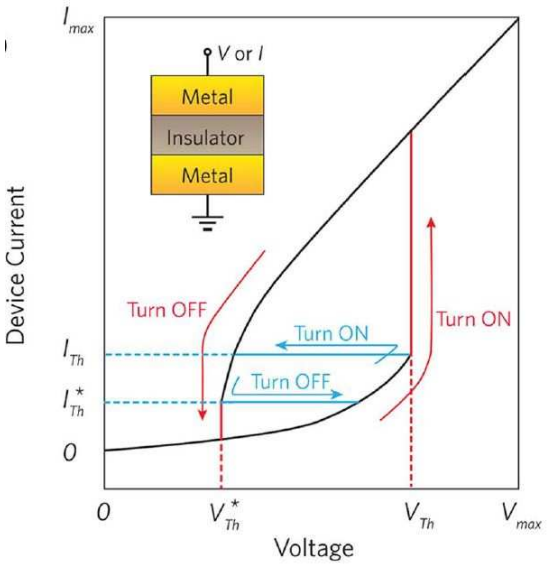

Figure 1.6: Gate current vs Gate voltage characteristics demonstrating the electrically triggered insulator-to-metal transition. Taken from Ref. [1].

1.8 Mechanisms of E-IMT

1.8.1 Joule-Heating model

The Joule-Heating model attributes the E-IMT to excessive heating of the device due to a large flow of current on the application of an applied voltage stress which increases the device temperature. The heating of the device results in the appearance of a localized filamentary conduction channel across the insulating VO layer [67] at the beginning of IMT. A rise in temperature $\sim$ 150 °C is observed in the conduction channel [68]. Since this temperature lies above the structural phase transition temperature of $\sim$ 67 °C, the conduction channel has a metallic character [66]. Studies from hard x-ray diffraction revealed that the channel comprises of metallic R phase although the remaining material shows insulating M1 phase [69]. In sharp contrast to temperature-induced IMT (T-IMT) where the entire bulk of the sample transitions to a metallic phase, Joule-Heating model describes the E-IMT in the form of occurrence of a localized metallic conduction channel across an otherwise insulating sample [66]. The sharp transition in current at the onset of E-IMT is thus solely attributed to the narrow conduction channel which has gained a metallic character [70]. Owing to the partial metallization of only a filamentary channel while the remaining area of the device is still an insulator, the magnitude of current-jump (ON/OFF ratio) is small compared to the resistivity ratio change in T-IMT. The threshold voltage of E-IMT in the Joule-Heating model is largely dependent on the device dimensions and the substrate temperature of measurement set-up [70, 71]. In a purely Joule-Heating model, the magnitude of threshold voltage decreases with increasing substrate temperatures.

1.8.2 Electronic model

A change in electron density for a Mott insulator causes strong electron correlation that finally leads to collapse of the bandgap [58]. Thus addition of carriers (electrons/holes) to the valence or conduction band of vanadium oxide causes an E-IMT phenomenon [1]. Past reports have revealed that E-IMT can be triggered by electric field alone without any flow of current through the device [72]. The order of applied electric field was 10^6-10^7 V/m [72]. The electric field leads to carrier injection thereby resulting in strong electron correlations [73]. However, electric field solely could not satisfactorily demonstrate the E-IMT in a three-terminal Mott-FET device geometry [74]. The carrier injection was thus also ascribed to the Poole-Frenkel ($P-F$) effect [75]. On the application of a large electric field across the device the thermal energy barrier faced by the valence band electrons for excitation into the conduction band is reduced by the $P-F$ effect. Presence of the $P-F$ effect is concluded when $\ln(I/E)$ varies linearly with $\sqrt{E}$. Here E denotes the applied electric filed and I is the measured current. Therefore, application of a large electric field results in rapid injection of electrons into the insulating VO_2, mediated by the $P-F$ mechanism [76].

1.8.3 Simultaneous contributions of Electronic and Joule-Heating model

Since the applied electric field is uniform, the metallic phase of VO_2 should have been achieved throughout the bulk of sample. Instead Markov *et al.* reported evidence of conduction across a narrow filament which supports a localized heating via Joule-effect [76]. Thus it was concluded that first of all high electric field initi-

ates carrier injection via the $P-F$ mechanism. The emitted electrons are highly energetic which causes rapid heating and current flow. Afterwards, the electric field falls and the Joule-effect conducts the current across the narrow conduction channel.

Gopalakrishnan *et al.* also reported that the E-IMT phenomenon cannot be initially triggered by Joule-effect alone. It is triggered by an electric field which results in a large flow of current. This leads to heating of the device via Joule-effect which further increases the current flow through a narrow region. Generally, the E-IMT phenomenon is also followed by a structural phase transition due to Joule-Heating of the device [77].

1.9 Outline of this Thesis

This thesis describes the fabrication and thereupon characterization of high-κ dielectric/oxide thin-film-based metal-oxide-semiconductor (MOS) memory devices. Various oxide films are reactively rf-sputtered on Si(100) substrates. The as-deposited films were then physically characterized using differential scanning calorimetry(DSC) and grazing incidence x-ray reflectivity(GI-XRR). Synchrotron radiation(SR) based grazing incidence x-ray diffraction(GI-XRD) and x-ray photoelectron spectroscopy(XPS) were also used for characterizing the deposited films. Since the deposited films possess insulating character, aluminium metal was deposited by electron-beam evaporation and subsequently patterned into gate electrodes by UV-Photolithography for performing various electrical measurements. The thesis is organized in the following order.

Chapter 2 presents the underlining physics of MOS Capacitors. The Band Diagrams of MOS devices on n-type and p-type semiconducting substrates are

elucidated. The application of a voltage bias to the metallic electrode leads to either the *accumulation* or *depletion* or *inversion* regions at the semiconducting surface. These have been elaborately discussed for a better understanding of MOS devices. The concepts of *ideal-threshold voltage* and *flat-band voltage* have been further highlighted. The capacitance-voltage ($C-V$) characteristics are discussed at length. The various kinds of oxide and interface traps are mentioned. The current-voltage ($I-V$) characteristics of MOS capacitors are explained. The conduction mechanisms namely, Fowler-Nordheim ($F-N$) tunnelling, Direct tunnelling and Poole-Frenkel ($P-F$) emission are also illustrated.

Chapter 3 is dedicated to the entire process flow entailed in the fabrication of MOS Capacitors. The deposition techniques and instruments used in the fabrication steps are elaborately mentioned. The physical characterization of high-κ dielectric/oxide thin-films are illustrated. The various electrical characterizations performed on MOS capacitors are also described.

Chapter 4 describes an improvisation of a reactive rf-sputtering system for the deposition of high-κ dielectric/oxide thin-films from metallic sputtering targets in Ar/O_2 plasma. A common problem associated with the deposition of high-κ dielectric/oxide-films via reactive sputtering is the formation of low-κ SiO_x interfacial layer (IL) at the oxide/silicon interface. This IL reduces the overall dielectric constant of the gate-dielectric stack and hinders its scaling down to sub-nm dimensions. This problem is circumvented by an added instrumental modification to the deposition chamber of a sputtering system. The analysis of x-ray reflectivity data suggests that the IL thickness could be restricted to ~ 0.5 nm in the modified sputtering unit. Furthermore, the accumulation capacitance (as estimated from the $C-V$ characteristics) increases with decreasing IL thickness suggesting an

improvement of the device performance.

Chapter 5 describes the role of oxygen content in the Ar/O_2 plasma in determining the electrical properties of reactively sputter-deposited vanadium oxide films on Si(100) substrates. The films were deposited at room-temperature. The oxide films were probed using laboratory source-based x-ray photoelectron spectroscopy for identifying the various constituent oxide phases of vanadium. The $I-V$ characteristics reveal that the films deposited at the highest oxygen content show signatures of insulator-to-metal transition(IMT). The IMT has been described by a voltage-induced Joule heating model which results in the formation of a localized filamentary metallic conduction channel across an otherwise insulating oxide layer. This study implies that the Ar/O_2 ratios play a critical role in governing the IMT of vanadium oxide films.

Chapter 6 highlights the role of measuring temperatures in governing the IMT properties of vanadium oxide based MOS devices. The films were deposited in different Ar/O_2 ratios at room temperature. However, the $I-V$ characteristics were measured at elevated substrate temperatures. The various oxide phases of vanadium were identified by differential scanning calorimetry (DSC) and synchrotron-based grazing incidence x-ray diffraction (GI-XRD). An amorphous to crystalline phase transition with increasing oxygen content in the reactive plasma is observed. The underlining mechanisms of IMT have been attributed to both electric-field induced carrier injection as well as structural phase transitions. Joule heating also plays an effective role. The IMT is absent at intermediate measuring temperatures due to the presence of crystalline and amorphous phase mixtures.

Chapter 7 describes the effect of glass transition temperature (T_g) on the IMT properties of vanadium oxide based MOS devices. The cooling cycle of the

DSC scan was used for arriving at the T_g of the oxide films. It is revealed that the T_g increases with increasing oxygen partial pressures in the Ar/O_2 plasma. The magnitude of IMT is enhanced when the films are deposited above T_g. The grain/crystallite size increases with increase in deposition temperatures accompanied by a simultaneous reduction in the density of grain boundaries. This in turn leads to an enhancement in the magnitude of IMT with the increase in deposition temperatures.

Chapter 8 presents a brief summary and future scope of the current thesis work.

2

Theory of MOS devices

2.1 Introduction

In electronics, metal-oxide-semiconductor field effect transistor (MOSFET) and complementary metal-oxide-semiconductor field effect transistor (CMOS) are the most extensively used devices in very-large-scale integrated (VLSI) circuits [78, 79]. A MOSFET is a unipolar device wherein the transport is mediated by carriers of one polarity [79]. It is also known as an insulated-gate field-effect transistor (IGFET). The description of a IGFET was first conceived by Lilienfeld and Heil although no fabrication was done owing to process limitation [80, 81]. The first working MOSFET based on thermally oxidised SiO_2 on a silicon substrate was successfully fabricated by Kahng and Attala in the year 1960 [82]. The MOS structure was initially viewed as a voltage-variable capacitor [83]. In a MOSFET, application of a voltage bias at the gate electrode modulates the channel current. An insulating layer separates the gate electrode from the channel. An understanding of the basic metal-oxide-semiconductor (MOS) structure is pertinent for understanding

of its operation, device fabrication and integration into electronic circuits.

2.2 The MOS Capacitor

A schematic of MOS structure or capacitor is illustrated in Figure 2.1. It consists of a dielectric oxide/insulating layer in-between a metallic gate electrode and a semiconducting substrate. The thickness of the gate dielectric is d and the magnitude of applied voltage bias on the gate electrode is V. Application of a positive voltage V implies that the gate electrode is biased positively with reference to the semiconducting substrate. Similarly, the gate electrode is biased negatively with reference to the semiconducting substrate when a negative voltage V is applied [79]. The MOS Capacitor with silicon used as a semiconducting substrate is most widely studied.

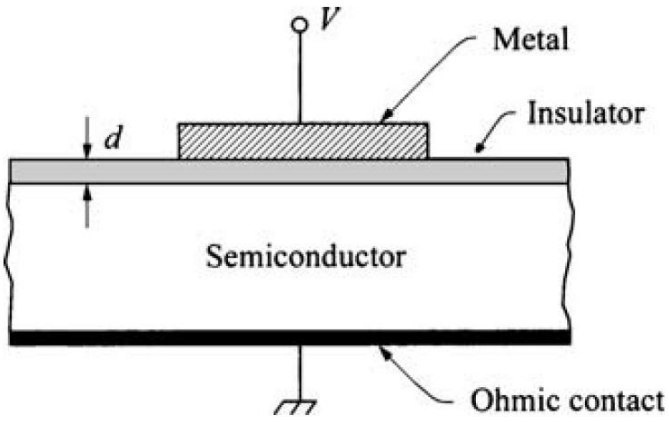

Figure 2.1: A schematic of a MOS Capacitor. Taken from Ref. [79].

2.3 Band diagram for the Ideal MOS Capacitor

2.3.1 Assumptions

The equilibrium conditions of a MOS capacitor refers to the case where $V = 0$. The band diagrams of a MOS capacitor for n-type and p-type semiconducting substrate, under equilibrium conditions are represented in Figure 2.2.

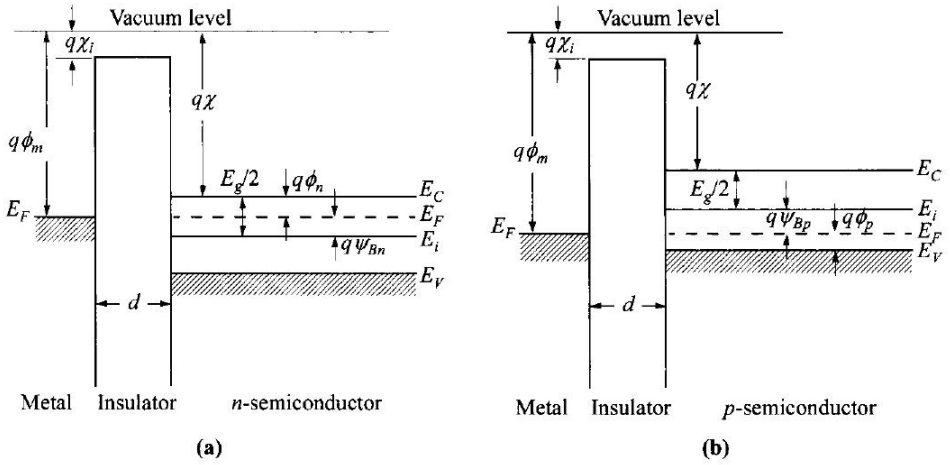

Figure 2.2: Band diagram of a MOS Capacitor under equilibrium conditions ($V = 0$) for (a) n-type semiconducting substrate (b) p-type semiconducting substrate. Taken from Ref. [79].

The work function of the metal refers to the energy required to remove an electron from the Fermi level to outside the metal. A modified work function for the metal-oxide interface is measured from the Fermi level of the metal to the conduction band of the oxide. Similarly, a modified work function for the semiconductor-oxide interface is measured from the Fermi level of the semiconductor to the conduction band of the oxide.

The assumptions behind an ideal MOS Capacitor can be summarized in the following,

(a) Under equilibrium conditions ($V = 0$), the metal work function (ϕ_m) is equal to the semiconductor work function (ϕ_s). In other words, the work-function difference (ϕ_{ms}) is zero. This means,

for n-type semiconducting substrate,

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_{Bn}\right) = \phi_m - (\chi + \phi_n) = 0 \qquad (2.1)$$

and for p-type semiconducting substrate,

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_{Bp}\right) = \phi_m - \left(\chi + \frac{E_g}{q} - \phi_p\right) = 0 \qquad (2.2)$$

In equations (2.1) and (2.2) χ denotes the semiconductor electron affinity, χ_i is the insulator electron affinity, E_g denotes the band gap, ϕ_B is the metal-insulator potential barrier and ψ_B represents the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. Thus for zero applied voltage bias, the band should be flat which is also referred to as the flat-band condition.

(b) There are no charges within the insulator /oxide. Moreover, no charge exists at the oxide-semiconductor interface. Under any biasing conditions of a MOS capacitor, charges exist only within the semiconductor. These charges are equal and opposite in polarity to the charges on the metallic surface lying adjacent to the insulator.

(c) The insulator has an infinite resistivity so that under application of a dc voltage no transport of carrier occurs through the insulator [79].

2.3.2 Biasing of a MOS Capacitor

In the earlier section, we addressed the equilibrium conditions of a MOS Capacitor wherein no voltage bias is applied at the gate electrodes ($V = 0$). On the application of a positive or negative voltage bias, the following cases may arise at the semiconducting surface which are also schematically represented in Figure 2.3.

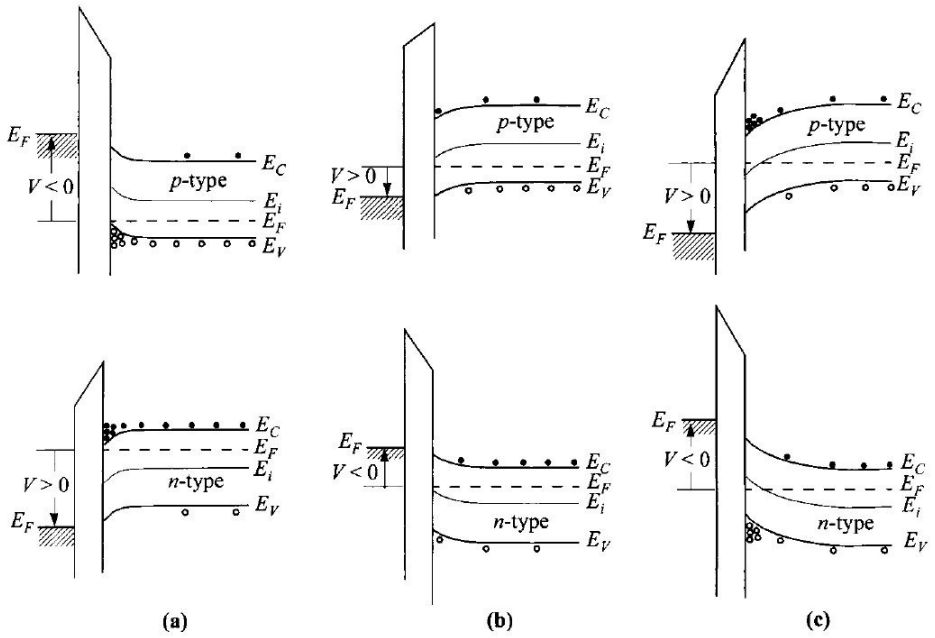

Figure 2.3: Band-diagrams of a MOS Capacitor upon application of a voltage bias (a) Accumulation (b) Depletion (c) Inversion for p-type semiconducting substrate (represented by top figures) and for n-type semiconducting substrates (represented by bottom figures). Taken from Ref. [79].

2.3.3 Accumulation

On the application of a negative voltage ($V < 0$) to the metallic gate and keeping the semiconducting substrate grounded, the MOS structure acts like a parallel-plate capacitor. The substrate and the gate behave like electrodes separated by

an insulating oxide layer [84]. In a way for p-type semiconductors, $V < 0$ applied to the gate implies that negative charge induces an equal net positive charge at the semiconductor/oxide interface [78]. In this case, holes accumulate at the semiconductor/oxide interface.The accumulation of holes can be understood from the band diagram in Figure 2.3(a). When a negative bias is applied to a p-type MOS structure, the Fermi level of the metal E_F is raised above its equilibrium position as represented by Figure 2.3(a). In the semiconductor, the top of the valence band E_V bends upwards and approaches closer to the Fermi level. The E_F of the semiconductor remains constant since for an ideal MOS Capacitor no current flows through the structure. The bending of E_V towards E_F in the semiconductor leads to an accumulation of majority carriers (holes in the case of p-type substrate) at the semiconducting surface since the carrier density varies exponentially with the difference (E_F - E_V). This condition is referred to as *Accumulation*.

2.3.4 Depletion

Application of a positive voltage bias ($V > 0$) to the gate implies that positive charge induces an equal net negative charge at the semiconductor/oxide interface. For a p-type semiconductor this scenario is achieved by depletion of holes leading to net immobile negative charge at the semiconducting surface. In the Band diagram picture of a MOS structure containing a p-type semiconductor (Figure 2.3 (b)), application of a $V > 0$ to the gate lowers the Fermi level E_F of the metal relative to its equilibrium value. The E_F of the semiconductor remains unchanged. The valence band E_V and conduction band E_C of the semiconductor bend downwards causing a depletion of majority carriers. This condition is referred to as *Depletion*.

2.3.5 Inversion

When the applied positive voltage is further increased, the bands at the semiconductor surface bend downward even more such that the intrinsic energy level E_i crosses the Fermi level E_F as shown in Figure 2.3 (c). The concentration of minority carriers at the semiconductor surface increases. For a p-type semiconductor this implies that electron concentration at the surface is larger than that of holes. In fact, the originally p-type surface now has the conduction properties of a n-type material. Thus, on the application of a large positive voltage the p-type semiconductor surface is inverted to an n-type. This condition is referred to as *Inversion*. The inverted n-type layer lies separated from the p-type layer by the depletion region and is crucial for MOS transistor operation.

2.4 Threshold voltage of a MOS Capacitor

The threshold voltage is defined as that value of V that must be applied to the gate metal electrode in order to generate an *inversion layer* at the semiconductor surface [84].

2.4.1 Ideal threshold voltage

The voltage applied to the gate V equals the summation of potential drops across the insulator/oxide layer and the semiconductor substrate,

$$V = \phi_s + \frac{Q_g}{C_{ox}} \tag{2.3}$$

In equations (2.3), ϕ_s is the surface potential of the semiconductor substrate, C_{ox} is the capacitance of the oxide layer and Q_g is the charge deposited at the metallic gate. In writing the above equation, one assumes that the semiconductor is grounded.

For the case of a p-type semiconductor, application of a positive bias at the gate induces an equal number of negative charge at the semiconductor. The negative charge consists of ionized impurities in the *depletion* region and free electrons at the semiconductor surface which form the *inversion* layer. At the beginning of formation of *inversion* layer, the charge owing to free electrons is far less as compared to that due to ionized impurities. In that scenario, equation (2.3) may be modified as

$$V = 2\phi_F - \frac{Q_d}{C_{ox}} = V_{Th} \tag{2.4}$$

where Q_d is the depletion charge. V_{Th} is defined as the *ideal threshold voltage*, assuming that both the source and substrate are grounded.

2.4.2 Flat-band voltage

The Fermi level of the metallic gate E_{FM} is not equal to the Fermi level of the semiconductor E_F. When a MOS structure is fabricated, alignment of the Fermi levels takes place resulting in the bending of energy bands in the semiconductor near the oxide/semiconductor interface as illustrated in Figure 2.4 [84]. However, the energy bands in the semiconductor should be flat. In order to retrieve the *flat-band condition*, a suitable voltage must be applied to the gate metal. This voltage, termed as the flat-band voltage ϕ_{MS}, equals the difference between the work functions of the metal (ϕ_m) and that of the semiconductor (ϕ_{sc}),

$$\phi_{ms} = \phi_m - \phi_{sc} \tag{2.5}$$

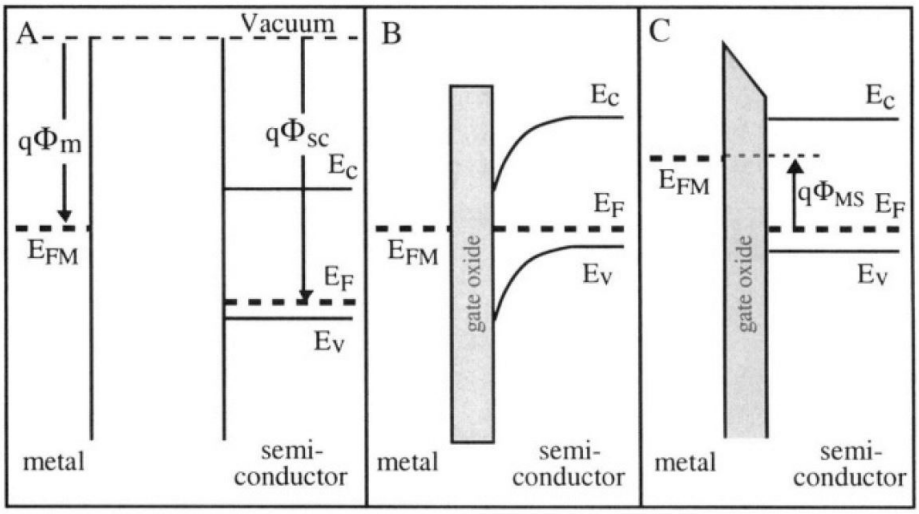

Figure 2.4: Band-diagrams of a MOS Capacitor (A) The metal and the semiconductor are separate and their Fermi levels are not equal (B) Fabrication of a MOS structure results in allignment of the metal and semiconductor Fermi levels. Bending of bands in the semiconductor takes place at the oxide/semiconductor interface (C) A suitable voltage is applied to retrieve the flat-band condition. Taken from Ref. [84].

2.5 Relation between Capacitance and Voltage for a MOS structure

2.5.1 Surface space-charge region

In order to arrive at the capacitance-voltage characteristics of a MOS structure one first needs to establish a relation between the surface potential, space charge and electric field [79]. The band diagram at the semiconductor/oxide interface for

a p-type semiconductor is illustrated in Figure 2.5.

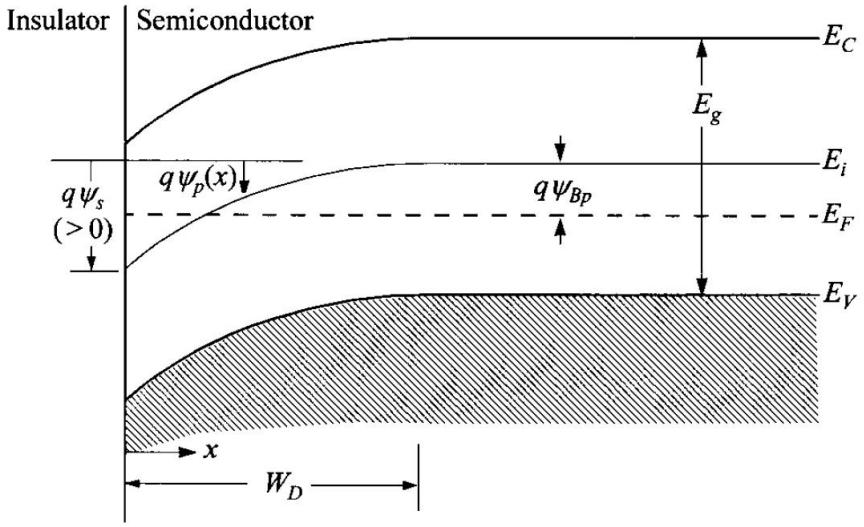

Figure 2.5: Band-diagram at the oxide/semiconductor interface of a p-type semiconductor. Taken from Ref. [79].

If $\psi_p(x)$ is the potential $E_i(x)/q$ of the semiconductor with respect to its bulk, $\psi_p(x)$ may be expressed as

$$\psi_p(x) \equiv -\frac{[E_i(x) - E_i(\infty)]}{q} \tag{2.6}$$

$x = 0$ denotes the surface of the semiconductor such that $\psi_s = \psi_p(0)$ represents the potential at the surface.

The concentration of electrons $n_p(x)$ and that of holes $p_p(x)$ varies exponentially with the potential $\psi_p(x)$ as,

$$n_p(x) = n_{p0} \exp(\beta\psi_p) \tag{2.7}$$

$$p_p(x) = p_{p0} \exp(-\beta\psi_p) \tag{2.8}$$

where $\psi_p > 0$ when the energy band bends downwards and $\beta = q/kT$. In equilibrium conditions ($V = 0$), the electron and hole densities are represented by n_{p0} and p_{p0}, respectively. For $x = 0$ (surface of the semiconductor) equations (2.7) and (2.8) reduce to the following forms,

$$n_p(0) = n_{p0} \exp(\beta\psi_s) \tag{2.9}$$

$$p_p(0) = p_{p0} \exp(-\beta\psi_s) \tag{2.10}$$

Depending upon the values of the surface potential ψ_s, the different regions can be identified as,

$\psi_s < 0$ means Holes are Accumulated and the bands bend upwards

$\psi_s = 0$ implies condition of flat-band voltage

$\psi_{Bp} > \psi_s > 0$ means holes are getting depleted and the bands bend downwards

$\psi_s = \psi_{Bp}$ implies that the Fermi-level lies in the middle of the gap. $E_F = E_i(0)$, $n_p(0) = p_p(0) = n_i$.

$2\psi_{Bp} > \psi_s > \psi_{Bp}$ means weak inversion and electron enhancement $n_p(0) > p_p(0)$.

$\psi_s > 2\psi_{Bp}$ means strong inversion $n_p(0) > p_{p0}$ or N_A.

From the $1 - D$ Poisson equation, $\psi_p(x)$ varies with distance from the oxide/semiconductor interface as,

$$\frac{d^2\psi_p}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{2.11}$$

In equation (2.11), $\rho(x)$ denotes the total space charge density and may be expressed as,

$$\rho(x) = q(N_D^+ - N_A^- + p_p - n_p) \tag{2.12}$$

In equation (2.12), N_D^+ and N_A^- denotes the densities of ionized donors and acceptors, respectively. Now the condition of charge-neutrality must be satisfied in the semiconductor bulk. Thus at $\psi_p(\infty) = 0$, $\rho(x) = 0$ and moreover

$$N_D^+ - N_A^- = n_{p0} - p_{p0} \tag{2.13}$$

Solution of the Poisson equation in the depletion region reduces to,

$$\frac{d^2\psi_p}{dx^2} = -\frac{q}{\epsilon_s}(n_{p0} - p_{p0} + p_p - n_p) \tag{2.14}$$

$$\frac{d^2\psi_p}{dx^2} = -\frac{q}{\epsilon_s}\left[p_{p0}\left\{\exp\left(-\beta\psi_p\right) - 1\right\} - n_{p0}\left\{\exp\left(\beta\psi_p\right) - 1\right\}\right] \tag{2.15}$$

Integrating equation (2.15) from the surface to the bulk, one arrives at

$$\int_0^{\frac{d\psi_p}{dx}} \frac{d\psi_p}{dx}\; d\left(\frac{d\psi_p}{dx}\right)$$

$$= \left(\frac{2kT}{q}\right)^2 \left(\frac{qp_{p0}\beta}{2\epsilon_s}\right)\left\{[\exp(-\beta\psi_p) + \beta\psi_p - 1] + \frac{n_{p0}}{p_{p0}}[\exp(\beta\psi_p) - \beta\psi_p - 1]\right\} \tag{2.16}$$

The electric field $\mathcal{E} = \frac{d\psi_p}{dx}$ is related to ψ_p as,

$$\mathcal{E}(x) = \pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi_p, \frac{n_{p0}}{p_{p0}}\right) \tag{2.17}$$

In equation (2.17) $\mathcal{E} > 0$ for $\psi_p > 0$ and $\mathcal{E} < 0$ for $\psi_p < 0$. The extrinsic Debye length for holes is represented by $L_D \equiv \sqrt{\frac{\epsilon_s}{qp_{p0}\beta}}$ and

$$F\left(\beta\psi_p, \frac{n_{p0}}{p_{p0}}\right) \equiv \sqrt{[\exp(-\beta\psi_p) + \beta\psi_p - 1] + \frac{n_{p0}}{p_{p0}}[\exp(\beta\psi_p) - \beta\psi_p - 1]} \tag{2.18}$$

For $\psi_p = \psi_s$ one arrives at the relation of electric field near the oxide/semiconductor interface,

$$\mathcal{E}_s = \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \tag{2.19}$$

Applying Gauss Law to equation (2.19), the total space charge per unit area equals,

$$Q_s = -\epsilon_s \mathcal{E}_s = \mp \frac{\sqrt{2}\epsilon_s kT}{qL_D} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right) \tag{2.20}$$

Considering a p-type semiconductor,

$Q_s > 0$ for $\psi_s < 0$ (Accumulation zone)

$Q_s = 0$ for $\psi_s = 0$ (Condition of flat-band)

$Q_s < 0$ for $\psi_{Bp} > \psi_s > 0$ (Depletion zone and Weak-inversion)

$Q_s \propto \exp(q\psi_s/2kT)$ for $\psi_s > 2\psi_{Bp}$ (Strong inversion)

2.5.2 Capacitance-Voltage $(C - V)$ characteristics

The condition of charge neutrality in an ideal MOS Capacitor implies,

$$Q_M = -(Q_n + qN_A W_D) = -Q_s \tag{2.21}$$

In equation (2.21), Q_M represents the charges per unit area on the metal and Q_S denotes the semiconductor's total charge per unit area. Q_n is the electrons per unit area near the inversion zone's surface. $qN_A W_D$ denotes ionized acceptors per unit area of the space-charge region having depletion width W_D.

For the ideal MOS devices, the difference between work functions of the metal and semiconductor must be zero ($\phi_{ms} = 0$). In that scenario, the voltage bias applied to the gate metal will cause a potential drop in the oxide/insulating layer

and the semiconductor meaning, $V = V_i + \psi_s$. Here V_i represents the potential drop in the insulator such that,

$$V_i = \mathcal{E}_i d = \frac{|Q_s|d}{\epsilon_i} = \frac{|Q_s|}{C_i} \tag{2.22}$$

In equation (2.22), d and ϵ_i denote the thickness and dielectric constant of the oxide layer, respectively. In a MOS structure of a fixed thickness d, C_i is a constant representing the maximum capacitance. However the capacitance of the semiconductor C_D varies with ψ_s and the frequency of measurement. The net capacitance of the MOS Capacitor is represented as,

$$C_{net} = \frac{C_i C_D}{C_i + C_D} \tag{2.23}$$

The semiconductor capacitance (C_D) is calculated as,

$$C_D \equiv \frac{dQ_s}{d\psi_s} = \frac{\epsilon_s}{\sqrt{2}L_D} \frac{1 - \exp(-\beta\psi_s) + (n_{p0}/p_{p0})[\exp(\beta\psi_s) - 1])}{F\left(\beta\psi_s, n_{p0}/p_{p0}\right)} \tag{2.24}$$

The $C - V$ characteristics of an ideal MOS Capacitor is illustrated in Figure 2.6.

2.6 Charges in the Oxide and Oxide/semiconductor interface

In section 2.3.1, an underlining assumption of an ideal MOS capacitor was that no charges are trapped within the gate-dielectric/oxide layer. Moreover, no traps should exist at the oxide/semiconductor interface. However during the standard

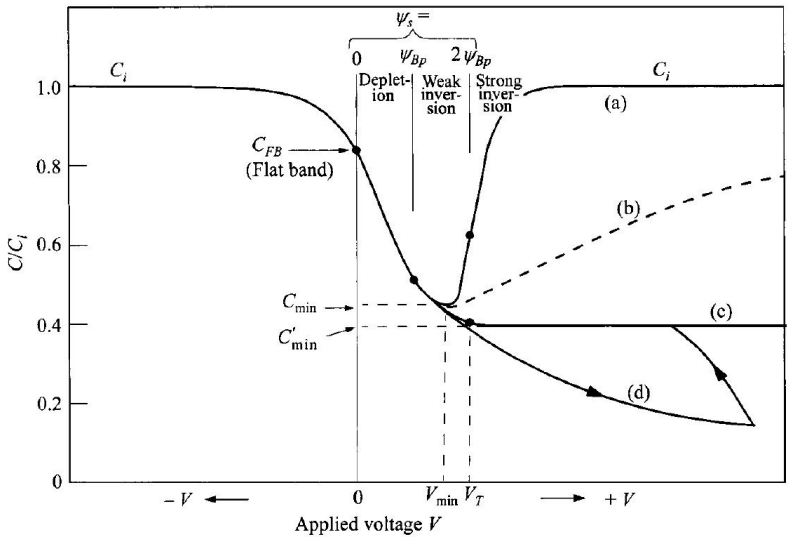

Figure 2.6: Capacitance vs voltage characteristics for a MOS capacitor in the regimes of (a) Low frequency (b) Intermediate frequency and (c) High frequency respectively. A voltage bias is applied to the gate electrode with respect to a p-type semiconductor. It is assumed that the flat-band voltage is zero ($V = 0$).Taken from Ref. [79].

process fabrication steps of a MOS structure, charges are generated within the bulk of the oxide layer as well as at the oxide/semiconductor interface. These charges affect the electrical characteristics of the device. For the case of SiO_2/Si (oxide/semiconductor system), these charges are categorised as fixed oxide charge, mobile oxide charge, oxide trapped charge and interface trapped charge [85, 86].

2.6.1 Interface trapped charge

The interface trapped charge arises owing to structural defects, radiation-induced defects or defects caused by breaking of bonds. The charges may also originate from defects caused by oxidation process or from those arising out of metal impurities. The interface trapped charge are found in the vicinity of oxide/semiconductor interface and are in direct electrical contact with the semiconductor. The charges

can be either positive or negative. The surface potential ψ_s determines whether these traps are charged or discharged. Annealing in hydrogen at low temperatures or in a mixture of hydrogen/nitrogen results in the neutralization of interface traps. At the Si/SiO_2 interface there are some unfulfilled or dangling $Si-Si$ bonds which give rise to energy states in the energy band gap at the silicon surface known as interface states or interface traps [84]. An interface trap density N_{it} means a charge of magnitude $qN_{it}(\phi_s)$ at the oxide/semiconductor interface. For electrons trapped at the interface states, an increase in surface potential from ϕ_s to $\phi_s+\delta\phi_s$ enhances the magnitude of trapped charge by $-qN_{it}\delta\phi_s$. In the presence of inversion layer at the semiconductor surface, $\phi_s = 2\phi_F$. In order to compensate for the interface traps, a voltage bias of magnitude V_{it} is applied at the gate such that,

$$V_{it} = \frac{2qN_{it}\phi_F}{C_{ox}} \tag{2.25}$$

The effect of interface traps on the $C-V$ characteristics is illustrated in Figure

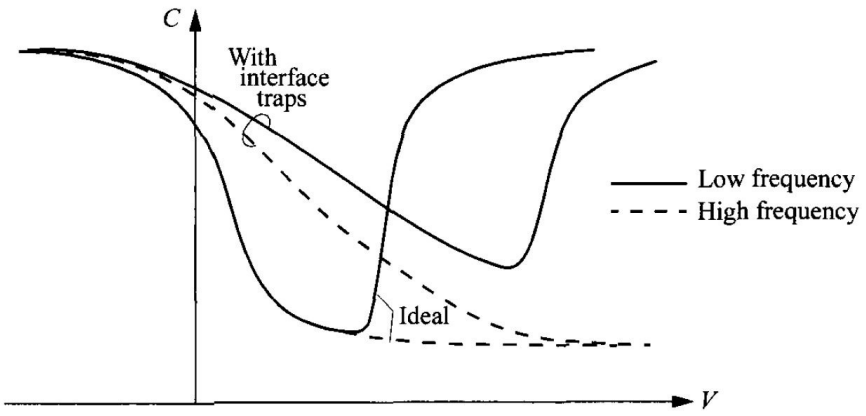

Figure 2.7: Effect of interface traps on the capacitance-voltage characteristics of a MOS device.Taken from Ref. [79].

2.7. It is evident that the $C-V$ characteristics are stretched in the direction of

applied voltage since carriers/charges are also occupying the traps. Thus a higher magnitude of applied voltage bias is required in order to achieve the same surface potential ψ_s [79].

2.6.2 Fixed oxide charge

Fixed oxide charges are positively charged and occur at the oxide/semiconductor interface. These originate from the oxidation process and their density is determined by the conditions and temperature of oxidation, conditions of silicon and the crystallographic orientation of the semiconducting substrate. Before any analysis of fixed oxide charge densities, the interface traps are first eliminated by annealing in H_2 or H_2/N_2 at low temperatures. Unlike the interface traps, fixed-oxide charge are not in electrical contact with the semiconductor. Increasing the oxidation temperature, lowers the density of these charges. In case oxidation at higher temperatures is not permissible in the process fabrication step, the charge can be reduced by a post-oxidation annealing treatment in N_2 or O_2 [84].

2.6.3 Oxide trapped charge

Holes/electrons trapped in the oxide/insulating layer give rise to oxide trapped charge. The charge may be either positive or negative. The trapping of holes/electrons occur by ionizing radiation, avalanche injection or Fowler-Nordheim tunnelling. These charge are reduced by annealing in temperatures $\leq 500^0C$.

2.6.4 Mobile oxide charge

Ionic impurities such as Na^+, Li^+, K^+ and H^+ give rise to mobile oxide charge. These charge may also arise from heavy metals or negative ions.

All the three kinds of oxide charges (as described above) are independent of the applied voltage bias [79]. Thus the presence of these charges causes a parallel shift in the $C-V$ characteristics along the direction of applied voltage as illustrated in Figure 2.8.

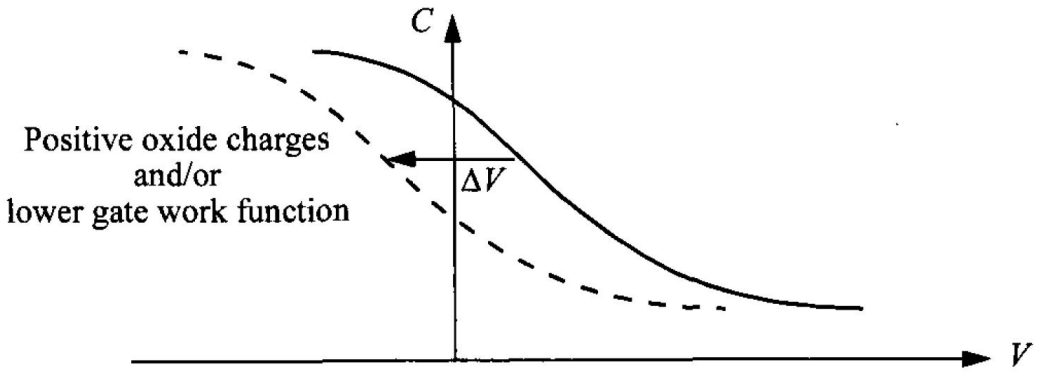

Figure 2.8: Effect of oxide charges on the capacitance-voltage characteristics of a MOS device.Taken from Ref. [79].

2.7 Current-Voltage ($I-V$) characteristics of MOS Capacitors

No conduction should take place through the gate-dielectric layer in an ideal MOS capacitor. However, in reality leakage current arises in the insulator which varies as a function of the applied voltage or electric field [78]. The electrons in the conduction band of semiconductor face a potential barrier at the oxide/semiconductor interface. Although the energy of electrons is less compared to the barrier height, the electrons may undergo quantum mechanical tunnelling for small width of the barrier and under application of high electric fields. The conduction mechanism via tunnelling is largely dependent on the applied voltage and independent of the

measuring temperature. The carriers cross the potential barrier either by Fowler-Nordheim mechanism [87] or by direct tunnelling as discussed below [79].

2.7.1 Fowler-Nordheim (FN) tunnelling

In the FN tunneling, the electrons in the semiconductor face a triangular potential barrier at the semiconductor/oxide interface during tunnelling into the conduction band of the oxide. Moreover, the tunnelling occurs through a part of the oxide layer only. The mechanism of FN tunnelling is demonstrated in Figure 2.9(a). The electrons after tunnelling across the triangular barrier are not hindered by the remaining oxide layer. Thus the entire oxide layer indirectly affects the current density in presence of the applied electric field. The thickness of the oxide layer must be $\geq$ 5 nm for the F-N tunnelling to occur. Since width of the barrier is inversely proportional to the applied electric field, the current density in FN tunnelling has the form [79]

$$J = \frac{q^3 E_{ox}^2}{16\pi^2 \hbar \phi_{ox}} \exp\left(-\frac{4\sqrt{2m^*}\phi_{ox}^{3/2}}{3\hbar q E_{ox}}\right) \tag{2.26}$$

where E_{ox} is the electric field across the oxide/insulator, ϕ_{ox} is height of the potential barrier faced by electrons and m^* is the effective mass of an electron in the conduction band of semiconductor. The current-voltage $(I-V)$ relations for FN tunnelling is written as

$$ln\left(\frac{I}{V^2}\right) = -\frac{8\pi\sqrt{(2qm^*)}\phi_{ox}^{3/2} d}{3hV} + C \tag{2.27}$$

where d is the oxide thickness and C is a constant.

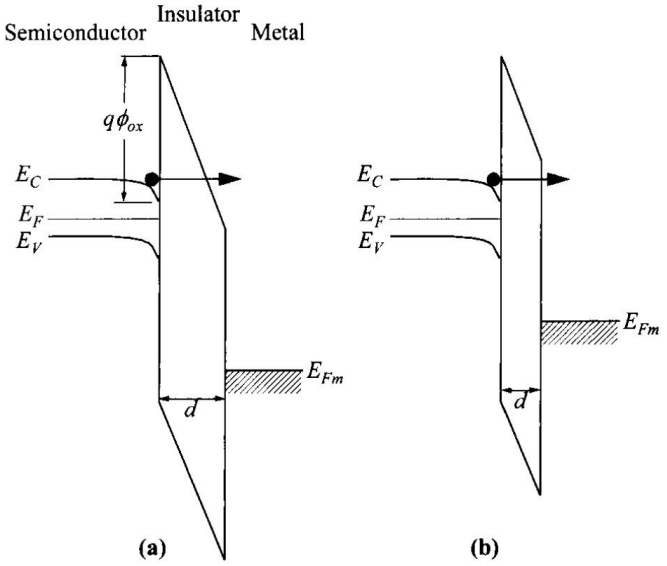

Figure 2.9: Tunnelling mechanims in MOS Capacitor (a) Fowler-Nordheim tunnelling occurs through a traingular potential barrier in oxides of thickness $\geq$ 5 nm (b) Direct tunneling occuring through the oxide having thickness of $<$ 5 nm.Taken from Ref. [79].

2.7.2 Direct tunnelling

Direct tunnelling occurs in thin oxide layers (thickness $<$ 5 nm) wherein the electrons of the semiconductor face a trapezoidal potential barrier as illustrated in Figure 2.9 (b). Unlike FN mechanism, direct tunnelling occurs across the entire insulating layer. The electrons in the conduction band of semiconductor tunnel through the oxide layer and appear at the gate metal without going through the conduction band of the oxide/insulator. The expression of current density in direct tunnelling is given as [79].

$$J = AE_{ox}^2 \exp\left\{ -\frac{B\left[1 - \left(1 - \frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right]}{E_{ox}} \right\} \tag{2.28}$$

where $A = q^3/16\pi^2\hbar\phi_{ox}$ and $B = 4\sqrt{2m^*}\phi_{ox}^{3/2}/3\hbar q$.

The current-voltage $(I-V)$ relations for direct tunnelling is written as

$$I = \left(\frac{-aq^2}{2\pi hd^2}\right) V \exp\left\{\frac{-4\pi\sqrt{2qm^*\phi_{ox}}d}{h}\right\} \tag{2.29}$$

where d is the thickness of oxide layer.

2.8 Poole-Frenkel Emission

Literature studies have revealed that the conduction mechanism of carriers in VO_2 is mainly mediated by the Poole-Frenkel (PF) emission [88, 89]. In the PF mechanism, under the influence of strong electric fields and temperatures, electrons are emitted from the traps into the conduction band [75] by thermal excitations [79]. The barrier height is a measure of the depth of the potential well of traps. High fields lower the effective height of trap potential well and thereby lower the thermal energy needed for emission of electrons into the conduction band. The mechanism of PF emission is illustrated in Figure 2.10.

In PF emission the current density varies as [79]

$$J \propto E_{ox} \exp\left\{-\frac{q\left(\phi_{ox} - \sqrt{\frac{qE_{ox}}{\pi\epsilon_{ox}}}\right)}{kT}\right\} \tag{2.30}$$

where E_{ox} and ϵ_{ox} are the electric field and dielectric constant of the oxide/insulator. ϕ_{ox} is depth of the trap potential well and k is the Boltzmann constant.

The current-voltage $(I-V)$ characteristics during PF emission can be written

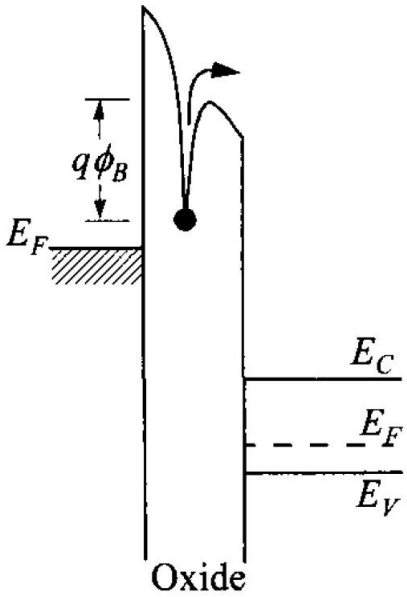

Figure 2.10: Band diagram for Poole-Frenkel emission.Taken from Ref. [79].

in the form,

$$ln\left(\frac{I}{V}\right) = \frac{q^{3/2}V^{1/2}}{\left(\pi\epsilon_0\epsilon_{ox}d\right)^{1/2}kT} + C \tag{2.31}$$

where d is the oxide thickness and C is a constant.

Thus a plot of $ln\left(\frac{I}{V}\right)$ vs $V^{1/2}$ should have linear characteristics as evident from equation (2.30).

3

Experimental Details

3.1 Introduction

The deposition of high-κ gate-dielectric and oxide thin-films are elaborately discussed in this chapter. A detailed description of the various techniques and instruments entailed in the physical characterization of the as-deposited films is also mentioned. Furthermore, the process steps involved in the fabrication of metal-oxide-semiconductor (MOS) capacitors are outlined. The electrical characterization of MOS capacitors and the techniques involved therein are also briefly discussed.

3.2 MOS Capacitor Fabrication

The process steps entailed with the fabrication of a MOS capacitor starts with the cleaning of semiconducting substrate. The gate-dielectric or insulating oxide layer is then deposited on the cleansed semiconducting substrate. A suitable metal

for the purpose of electrical characterization is deposited afterwards on the oxide layer. The metallic film is then patterned into gate electrodes using a lithography technique. A detailed discussion of the above steps, engaged for the work carried out in this thesis, are discussed in the following subsections.

3.2.1 Choice of the semiconducting substrate

A $4 - inch$ diameter n-type Si (100) wafer having resistivity of 1-10 $\Omega - cm$ was used for depositing the high-κ dielectric or oxide thin-films. The Si wafer was cut into several substrates of dimensions $1\ cm \times 1\ cm$. These substrates were used for oxide-film deposition and subsequent device fabrication and characterization.

3.2.2 RCA Cleaning of substrates

The *Radio Corporation of America (RCA) Standard Clean technique* is a set of recommended procedures for cleaning of silicon wafers prior to fabrication of very-large-scale integration(VLSI) and ultra large scale integration(ULSI) silicon circuits which is widely used in the semiconductor industry [90, 91]. The wafer-cleaning methodology was devised by Werner Kern in the year 1965, while he was working for the Radio Corporation of America, from where the abbreviation RCA has been derived.

The RCA Standard Clean comprises of the following three steps which are performed consecutively in order to strip away the various contaminants and native silicon oxide (SiO_x) layer present on the wafer surface.

Removal of Organic Contaminants (Organic Clean):

A chemical solution termed hereby as $RCA-1$ is prepared which consists of a mixture of deionized water, ammonium hydroxide (NH_4OH, 29% by weight) and hydrogen peroxide (H_2O_2, 30% by weight) in the volumetric-ratios of $5:1:1$, respectively.

The silicon substrates are immersed in $RCA-1$ and the solution is heated at $\sim 75-80^{\circ}C$ for 10 minutes. The base-peroxide mixture of $NH_4OH-H_2O_2$ effectively removes the organic residues from the silicon surface. After the cleaning, the substrates are removed and rinsed in de-ionized water.

Removal of Ionic and Metallic Contaminants (Ionic Clean):

A chemical solution termed hereby as $RCA-2$ is prepared which consists of a mixture of deionized water, anhydrous hydrochloric acid (HCl, 37% by weight) and hydrogen peroxide (H_2O_2, 30% by weight) in the volumetric-ratios of $5:1:1$, respectively.

Following the cleansing by $RCA-1$, the silicon substrates are now immersed in $RCA-2$ solution and is heated at $\sim 75-80^{\circ}C$ for 10 minutes duration. In this step, the metallic and ionic contaminants present on the substrate surface are removed effectively. The substrates are afterwards removed and rinsed in de-ionized water.

Native oxide removal (Oxide Strip):

In the bulk, Si is tetrahedrally bonded to four neighbouring Si bonds forming $Si-Si$ bonds. In contrast to the bulk, the surface of the silicon substrates contains unsatisfied or dangling bonds. Since the wafer surface is exposed to the atmosphere, the dangling bonds co-ordinate with the atmospheric oxygen and form a native

SiO_x layer. It is imperative to strip-off the SiO_x layer since it reduces the overall capacitance of high-κ dielectric stack and hinders the scaling down of *effective oxide thickness* (EOT) to below sub-nm dimensions.

1 % hydrofluoric acid (HF) solution is prepared in Teflon beakers. The *RCA cleansed* substrates are now immersed in HF solution and gently stirred for 1-minute duration at room temperature. Subsequently, the substrates are rinsed in de-ionized water and dried. This step effectively strips away the native oxide layer.

Since the silicon surface is sensitive to further reaction with atmosphere, the *RCA cleansed* and HF *etched* substrates need to be immediately loaded into the oxide-deposition chamber as discussed in the following section.

3.2.3 High-κ dielectric or oxide layer deposition by RF sputtering

The *RCA cleansed* and HF *etched* Si(100) substrates are loaded into the deposition chamber of sputtering system, equipped with dc and rf magnetron cathodes, manufactured by Korea Vacuum Tech., Ltd. (Model name: KVS-T4065) for the purpose of depositing high-κ gate dielectric or oxide thin-films. The sputtering unit, as displayed in Figure 3.1, is installed in the class 1000 grade clean room facility of the Surface Physics and Materials Science Division at Saha Institute of Nuclear Physics, Kolkata, India. For the purpose of this thesis work, vanadium oxide and hafnium oxide thin-films were deposited by reactive rf-sputtering in Ar/O_2 plasma environment. Diagrams of the sputtering unit and its different portions are illustrated in Figures 3.1 and 3.2.

Description and Operation of the Sputtering Unit:

The Sputtering unit comprises of three components, namely the vacuum pumping system, deposition chamber and a control panel.

The pumping system comprises of a *rotary pump (RP)* and a *turbo molecular pump (TMP)*. The vacuum line of the RP is connected to the TMP through a *fore-line valve* (FV). The line of the main deposition chamber is connected to the RP through a *roughing valve (RV)*. The connection of the deposition chamber to the TMP is mediated by a gate-valve known as the *main-valve (MV)*. The deposition chamber, usually in *high-vacuum* conditions, is vented using a *high-leak valve (HLV)* so that the chamber pressure can reach the atmospheric pressure. To begin any deposition, first of all the RP is switched-on and the valve FV is opened. This connection known as the *backing-line* is evacuated by RP to a vacuum of $\sim 10^{-3}$ Torr measured by a pirani gauge (*Gauge A*). The TMP is powered on once the backing-line reaches a vacuum level of $\sim 10^{-3}$ Torr. The valve FV is now closed and the valve RV is opened so that the RP can evacuate the deposition chamber. RP is able to evacuate the sputtering chamber to a vacuum level of 5×10^{-3} Torr as displayed by the *Gauge B*. In this case, once the sputtering chamber reaches a vacuum level of $\sim 10^{-3}$ Torr, the valve RV is closed, and the valve FV is opened and now, the gate-valve MV is opened so that the TMP can directly evacuate the deposition chamber. An *Ion Gauge* displays the vacuum level in the deposition chamber by the TMP. A base pressure of $\sim 5 \times 10^{-6}$ Torr should be reached prior to beginning of the sputter-deposition process. Thus to summarize, the rotary pump evacuates the deposition chamber from atmospheric pressure to a vacuum level of $< 5 \times 10^{-2}$ Torr. Afterwards, the turbo molecular pump evacuates the chamber to a base-pressure of $\sim 5 \times 10^{-6}$ Torr. All the valves are pneumatically

controlled which require a continuous flow of compressed dry air (CDA).

The deposition chamber is vented by opening the valve HLV. Once its pressure reaches atmospheric level, the deposition chamber can be opened. The sputtering chamber comprises of three magnetron heads; of which 2 are for DC sputtering and 1 for RF sputtering. The sputtering targets are of *2-inch* diameter discs having a thickness of *4 mm*. The targets may be either pure metallic (99.9 % purity) or may be in oxide/ceramic form. Metallic targets can be used for RF as well as DC sputtering whereas oxide targets are solely reserved for RF sputtering. Three target shutters are available which can be opened/closed during sputtering. The silicon substrates are placed on the substrate or sample stage. A rotation of upto 60 rpm can be applied to the substrate stage in order to ensure uniformity of the deposited film. Moreover, a proportional–integral–derivative (PID)-based Hanyoung NP 100 temperature controller, attached to the substrate holder, can raise the substrate stage temperature upto 800 °C. A shutter is also present at the substrate end. As per the requirements of sputtering, Ar and O_2 gases can be introduced into the chamber whose flow-rates can be controlled and monitored by mass-flow controllers (MFC). A programmable throttle valve is in place between the MV and chamber to control and set a constant chamber pressure, independent of the gas flow rates, during deposition. Although the base pressure is 5×10^{-6} Torr, the deposition pressure is set $\times 10^{-3}$ Torr owing to the presence of process gases. In order to prevent heating of the sputtering system, water lines are connected to the magnetron heads and deposition chamber walls.

The control panel comprises of the control units for DC and RF power supplies, panels for displaying pressure, controlling and monitoring the rotation and substrate heating, MFCs and valves. The control panel for the RF power gun has

provisions for monitoring the *Forward power* and *Reflected power*. The reflected power should be reduced to zero. The RF-plasma is ignited at a higher chamber pressure (typically, 20 mTorr) and higher flow-rate of Ar (75 sccm). However, once the plasma is ignited it can be sustained at lower pressures (say, 5 mTorr) and lower Ar flow-rates (say, 50 sccm) and the sputter-deposition proceeds unhindered. A *RF matching control unit* is used for matching the impedance of the RF-power supply with that of the sputtering chamber and thus the Reflected power is reduced to zero, once the impedance is matched. For the DC power supply, the applied voltage and current can be set and monitored by the dc power supply, positioned in control panel so that the deposition occurs at a constant power.

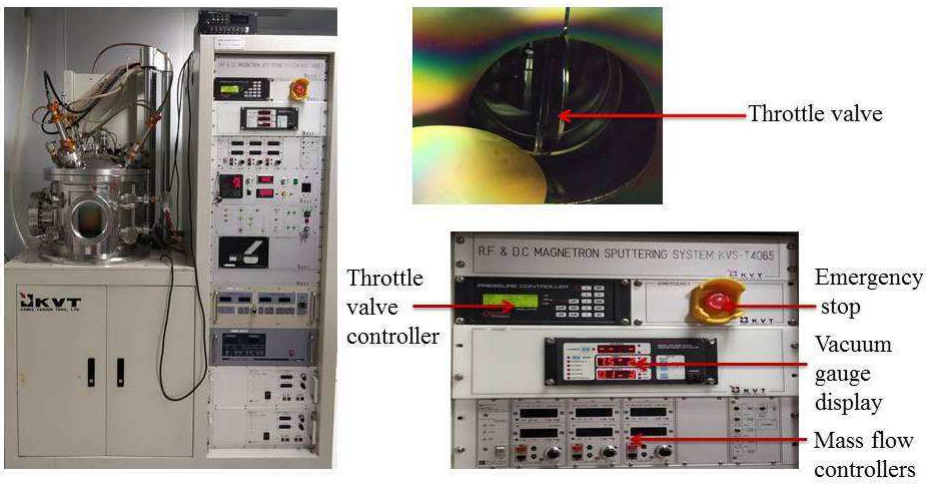

Figure 3.1: The DC and RF sputtering system manufactured by Korea Vacuum Tech., Ltd. (Model name: KVS-T4065) : Part-1

A description of the principles of sputter-deposition:

A solid surface when bombarded with energetic particles like accelerated ions results in collisions between the energetic ions and the atoms of the solid surface. As a consequence of the collisions, the atoms of the solid surface are ejected back-

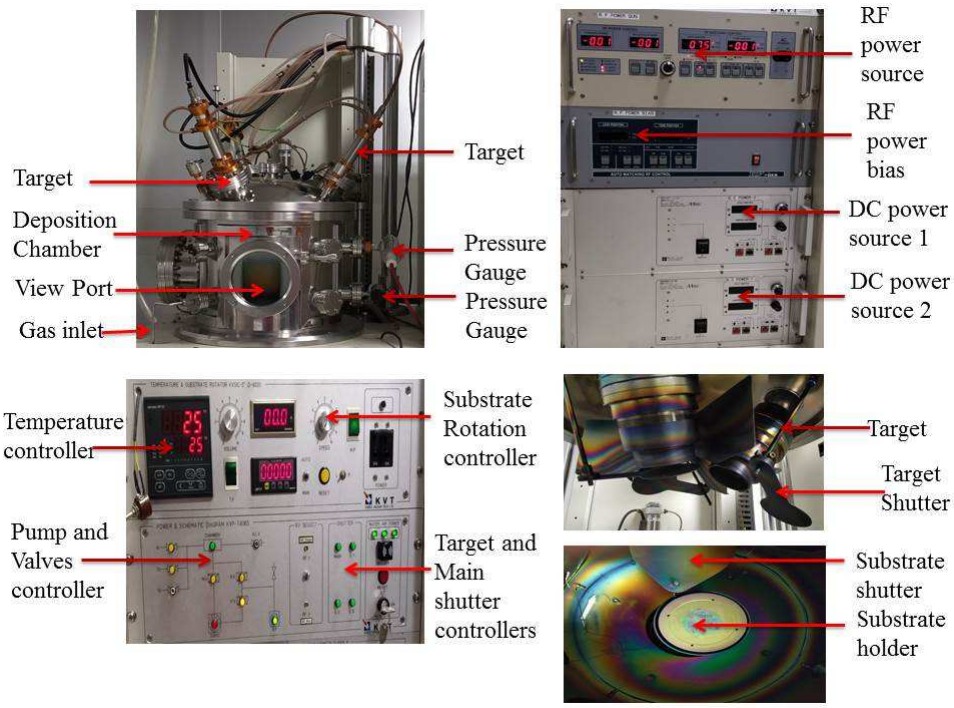

Figure 3.2: The DC and RF sputtering system manufactured by Korea Vacuum Tech., Ltd. (Model name: KVS-T4065) : Part-2

wards. This physical process is known as *back-sputtering* or just *sputtering* [92]. This technique has been used for the thin-film depositions.

For the purpose of film deposition, a target material is bombarded by inert gas ions of Argon (Ar^+). Argon is the most common gas for sputtering due to its mass and abundance. The *DC sputtering* system comprises of two electrodes, one of which acts as a cold cathode and the other one acts like the anode. The target material to be sputtered is fixed at the cathode. The silicon substrates are placed on the substrate holder, acting as the anode. The sputtering chamber, which was till now in high-vacuum conditions (base pressure of 5×10^{-6} Torr), is now purged with Ar gas. The typical chamber pressures after introduction of Ar reaches $\sim 10^{-3}$ Torr. Upon application of a threshold DC voltage across the two electrodes, the Ar gas is ionised to a plasma state of Ar^+ ions. The glow discharge

(or current flow) is sustained by the DC voltage bias. The Ar^+ ions constituting the glow discharge are accelerated towards the cathode in presence of negative voltage . The highly energetic ions hit the target and eject its atoms/molecules from the surface, resulting in thin-film deposition on the silicon substrates. The target material selected for DC sputtering should be pure metallic since the glow discharge is generated between metallic electrodes. Since the metallic target has a large number of free electrons, the striking Ar^+ ions are neutralised after collisions with the surface atoms of the target and returned back to the plasma.

Had the target material of a DC sputtering system been an insulator or oxide/ceramic target, the Ar^+ ions cannot be neutralised. The glow discharge can no longer be sustained owing to the presence of surface charge comprising of positively charged Ar ions near the oxide target surface. This layer of positively charged surface repels away the further incoming Ar^+ ions from hitting the target. In such a scenario, the process of sputtering comes to a standstill. In order to circumvent the problem, a RF bias needs to be applied to the insulating target so that the periodic reversal of polarity removes the layer of surface positive charge. The process is thereby termed as *RF sputtering* wherein oxide/insulator thin films can be directly sputter-deposited from an insulator target. In addition to the dc/rf sputtering technique, a magnetic field closer and grossly parallel to the target surface is present in the magnetron sputtering to get a better secondary electron confinement. Due to such confinement, a significant improvement on ionization of gas molecules/atoms takes place because of hopping movement of the trapped electrons in presence of electric and magnetic fields.

For the case of *magnetron sputtering*, a magnetic field produced by ceramic small cylindrical magnets is applied to the cathode and glow discharge, in a direc-

tion parallel to the target surface confining ionized Ar atoms and electrons about the target zone. The electrons of the glow discharge thus undergo the motion of a cycloid. The centre of the cycloid orbit follows the direction of $\mathbf{E} \times \mathbf{B}$ having a drift velocity E/B. Here $\mathbf{E}$ and $\mathbf{B}$ denote the electric field generated in the plasma and the transverse magnetic field, respectively. The magnetic field is directed in such a way that the electrons form a closed-loop path which in turn enhances the rate of collisions between the electrons and Ar gas molecules. Thus to summarize, in a magnetron sputtering set-up, the applied magnetic field increases the plasma density. This enhances the current density at the target surface leading to higher sputtering rates than conventional glow discharge-based sputtering technique. Moreover in case of microwave-based sputtering system, the deposition pressure may be lowered to $\sim 10^{-5}$ Torr which in turn increases the mean-free path of sputtered target atoms. This further increases the rates of sputtering [92].

In order to deposit oxide/nitride thin films from pure metallic target, reactive gases like O_2, N_2 or N_2O are introduced into the chamber along with Ar. This kind of sputtering is termed as *reactive sputtering* and can occur in both DC and RF Sputtering systems.

In the work undertaken in this thesis, hafnium oxide and vanadium oxide thin-films were reactively sputter-deposited from pure metallic Hafnium and Vanadium targets (99.9 % purity), respectively. The reactive gas O_2 was introduced along with Ar in the glow discharge of plasma. The targets were fixed at the RF magnetron heads.

3.2.4 Metallic gate deposition with e-beam evaporation

The oxide films deposited on silicon substrates by reactive rf-sputtering can now be studied by various physical characterization techniques. However, for electrical measurements a metallic film needs to be deposited on the as-deposited oxide/insulator for electrical contact. For our work, aluminium was deposited on the oxide thin-films by an electron-beam (e-beam) deposition system with e-beam source manufactured by Telemark (Model name: 211). The e-beam unit as displayed in Figure 3.3, is installed in the class 1000 grade clean room facility of the Surface Physics and Materials Science Division at Saha Institute of Nuclear Physics, Kolkata India.

Description and Operation of the E-beam unit:

The *vacuum system* of the e-beam unit is similar to that of the sputtering unit discussed in subsection 3.2.3. It comprises of a *Rotary Pump* (RP) and a *Turbo Molecular Pump* (TMP). The TMP is cooled by air-flow in contrast to the water-cooled TMP of the sputtering unit. The RP evacuates the deposition chamber to a vacuum of $\sim 10^{-2}$ Torr when the *Roughing Valve* (RV) is opened. Once the chamber reaches the required vacuum level, RV is closed and the *Backing Valve* (BV) is opened. Now the backing-line is evacuated to $\sim 10^{-2}$ Torr. At this point, the power on the TMP is switched on. Once the TMP reaches its maximum rpm (revolutions per minute) of 715 Hz, the *High-Vacuum valve* (HV) is opened. The TMP now directly starts evacuating the deposition chamber from an initial vacuum level of $\sim 10^{-2}$ Torr to a base-pressure of $\sim 10^{-7}$ Torr. The readings of the vacuum level are displayed in the pressure-gauge panel supplied by Edwards. During deposition, the chamber pressure falls slightly from $\sim 10^{-7}$ Torr to $\sim$

10^{-6} Torr, indicating the presence of evaporated material within the deposition chamber. All the valves are pneumatically operated requiring a constant flow of compressed dry air.

The *deposition chamber* comprises of four pocket-based e-beam deposition system where appropriate crucibles containing materials to be deposited are placed in the pockets. The advantage of the system is to deposit multilayers without breaking the vacuum. In our case, a crucible where the aluminium material to be evaporated is placed. The electron-beam is ejected from a gun comprising of tungsten filament. The crucible should be made of an element/compound having a high melting point and compatible to the material(s). In our case, a tungsten crucible is selected. The sample stage comprises of a large metallic disk placed above the crucible. The oxide thin-films are affixed on the sample stage using adhesive tapes at the corners of the film. A substrate shutter is present co-axially at a certain distance from the stage. A beam of electrons impinging on the metal raises its temperature beyond its melting point. Once the substrate shutter is opened, the melted metal, Al in this case evaporates and deposits on the oxide films placed vertically above on the sample stage. A quartz crystal micro-balance (QCM) is placed near the sample stage to measure the thickness of the deposited aluminium. A rotation is applied to the sample stage during deposition in order to ensure film uniformity. The sample stage is equipped with a heating-facility such that its temperature may be raised upto 800° C.

The *control panel* comprises of the power supply of 7 kV with electromagnetic focussing and alignment set-up. A high-voltage of $\sim$ 6 kV is applied during the deposition. The *source* has two components of current namely, *emission current* and *filament current*. A magnitude of filament current $\leq$ 20 A, indicates that the

tungsten filament of electron gun is in healthy conditions and may be operated. The emission current (measured in mA) directly determines the flow and intensity of electron-beam impinging on the metal within the crucible. A joystick sweeps the movement of electron-beam in the lateral or longitudinal direction and places it inside the tungsten crucible. For values of emission current $\geq$ 100 mA, the aluminium is melted and evaporated towards the sample stage.

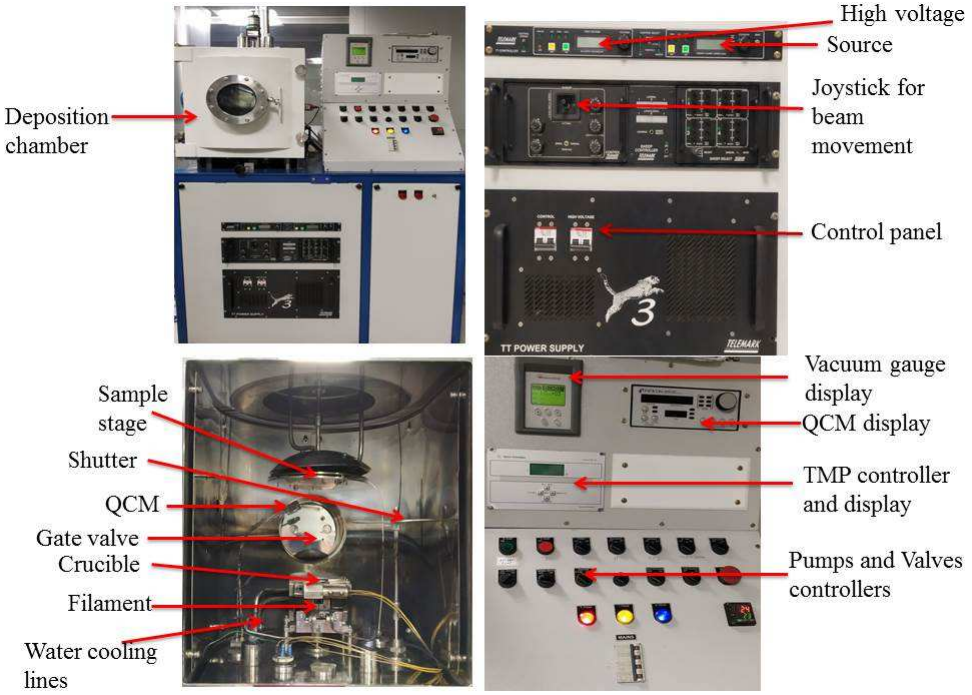

Figure 3.3: The electron-beam evaporation unit.

A description of the principles of electron-beam evaporation:

The principle of evaporation can be summarised as follows: Metals when heated to high temperatures gain a high vapour pressure. In high vacuum conditions, the evaporated atoms would be deposited on the substrate [93]. In an e-beam evaporation system, an electron gun placed under the crucible emits a highly energetic

beam. The applied high voltage accelerates the electron beam. A strong magnetic field bends the direction of the electron beam and curves its path such that the focussed beam now falls on the material placed inside the crucible. High rates of deposition enables film thickness $\sim$ 1 micron in relatively short span of time as compared to sputtering. Refractory materials like tungsten and graphite are used as crucibles so that the molten aluminium at high temperatures does not react with the crucibles [93].

3.2.5 UV-Photolithography

Principle of Photolithography:

In semiconductor device fabrication process flow, a technique termed as Photo-Lithography is used whenever one needs to transfer a given pattern to a substrate. The transfer of pattern is required for various purposes during fabrication namely, selective diffusion, metallization, implantation, etching etc. The substrates are first coated with a highly viscous photosensitive organic liquid known as *photoresist*. The photoresist are spin-coated for ensuring a uniform deposition followed by baking in a oven for thermal hardening. The photoresists are categorized into two namely, *positive* or *negative* photoresist. When *positive photoresists* are exposed to light, its long-chain organic molecules are broken down into shorter chains. This shorter chains are soluble in a chemical solution termed as *Developer*. When *negative photoresist* is exposed to light, the organic molecules are cross-linked to form longer-chains molecules with higher atomic mass such that the unexposed sections of the photoresist are soluble in a suitable Developer solution [84].

A suitable mask is used wherein the desired pattern is imprinted. The mask is placed on the substrate and ultra violet light is exposed through it for transferring

the pattern onto the substrate. The mask consists of chromium patterns imprinted on a soda lime glass. The patterns may vary depending on the process step like etching of metallic gate. The mask is placed either in *immediate contact* with the underlying substrate or in *close proximity*. In contact mode, the resolution of the transferred pattern is the best however the mask or substrate may get scratched. In *close-proximity mode* the mask is placed at small but fixed distance. However the patterns projected on the photoresist are less sharp. The minimum pattern size (l_m) transferred to the substrate in close-proximity mode may be expressed as

$$l_m \sim \sqrt{\lambda x} \tag{3.1}$$

In equation (3.1) x is the separation between mask and substrate and λ is the wavelength of light used at the time of exposure.

The resolution of the patterns in *close proximity* mode is usually improved by sophisticated optics system in UV photolithography. High resolution may also be achieved by imprinting patterns using focussed electron/ion beam. However the process requires long exposure times. X-rays may also be used in place of UV light in case of a non-divergent beam generated from a synchrotron source.

Process steps in photolithography:

In the current thesis work, due to different technical constraints at times, two approaches have been adopted to pattern the gate electrodes for HfO_2- and vanadium oxide-based MOS devices. The approaches are the following:

a) Pattern transfer using photolithography was carried out after Al metallization and then undesired Al was etched away in acid solution.

b) Photolithography was first performed on the oxide film and stripping of resid-

ual photoresist was done. This was followed by aluminium metal deposition and removal of undesired photoresist and metals over it by lift-off process in acetone.

The first photolithography process involving etching in *acid solution* is described below:

Spin Coating of photoresist:

The substrates comprising of metallic aluminium on oxide film are spin-coated with AZ 1518 photoresist (positive photoresist). The spin coater is manufactured by Brewer Science Inc. The substrates are placed on the vacuum chuck of the spin coater and photoresist are dispensed on the substrate. The photoresist smears the entire substrate surface. The chuck is then rotated in steps with the final speed of 4000 rpm. The resultant centifugal force leads to a uniform coating of photoresist on the substrate. Typical thickness of the coating varies from $\sim$ 1.8 micron.

Baking:

The photoresist coated substrate are introduced into an oven supplied by Lenton Thermal designs. The temperature for baking is set at 95° C using a Eurotherm temperature conroller. The substrates are baked for 30-minutes duration. The viscous photoresist are thermally hardened. Moreover, any solvents which are not photo sensitive are successfully removed.

Exposure in UV light using Mask Alligner:

A mask aligner manufactured by Neutronix Quintel (model: NXQ 8000ML) is used for exposing the ultraviolet rays of light on the substrate through the photomask. The photomask is placed on the substrate in *closed proximity mode* having a separation of 5 micron. The exposed regions of the photoresist coated substrate react with the UV rays to form a compound that is soluble in developer solution. The intensity of the UV light is 13 mwatt/cm^2 and the exposure time is

12 seconds. A photograph of the installed mask alligner is depicted in Figure 3.4.

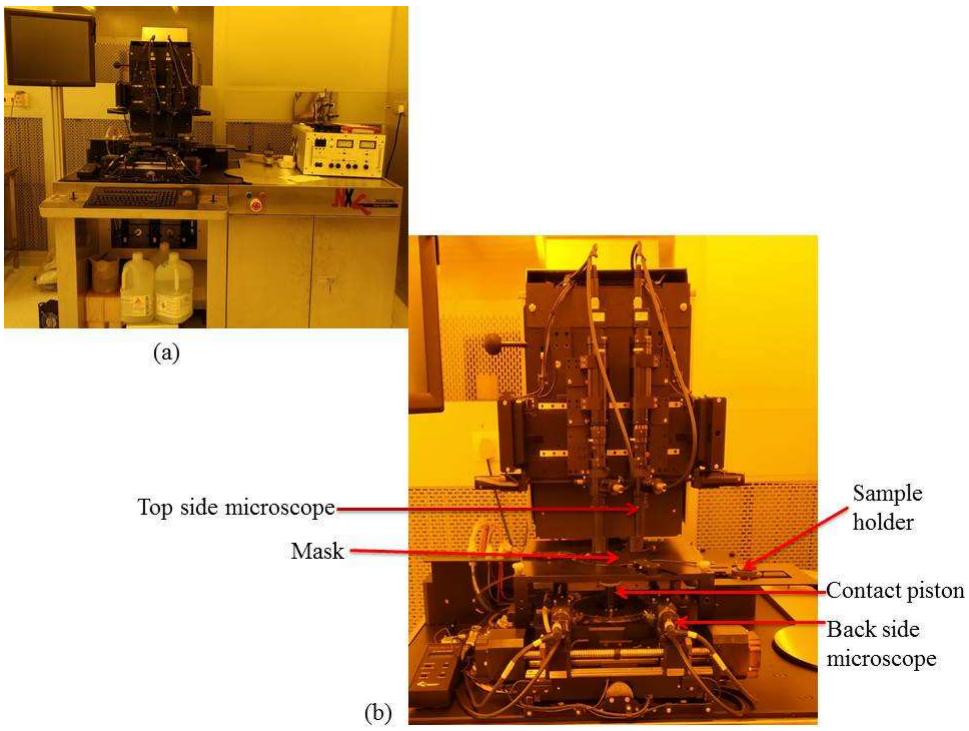

Figure 3.4: A photograph and schematic of the installed mask alligner

Photoresist development:

A solution mixture comprising of deionised water and AZ 351 B Developer is prepared in the volumetric ratios of 5 : 1, respectively. The substrates are immersed in the developer solution and gently stirred for 15 seconds. Afterwards, the substrates are rinsed in deionised water. The UV-exposed regions of the photoresist are soluble and thus washed away in the developer solution.

Metal etching in Acid solution:

Now only selective regions of the substrate are covered with the photoresist. In the rest of the regions, the bare aluminium metal remains exposed. For etching away the aluminium metal, a chemical bath comprising of H_3PO_4, HNO_3, CH_3COOH and deionised water is prepared in the volumetric ratios of 80 : 5 :

5 :10, respectively. The etching time depends on the thickness of the deposited metal. After etching, the photo-resist is removed using acetone.

The second photolithography process is described below

Spin-coating of photoresist:

The substrates comprising of oxide film are spin-coated with AZ 1518 photoresist. The substrates are placed on the vacuum chuck of the spin coater and photoresist are dispensed on the substrate. The photoresist smears the entire substrate surface.The chuck is initially rotated at 500 rpm; with an accelaration of 500 rpm/sec for 2 seconds. This is followed by a rotation at 4000 rpm; with an acceleration of 4000 rpm/sec for 1-minute duration. The thickness of the photoresist coating is $\sim$ 1.8 micron.

Baking:

The photoresist coated substrates are thermally hardened in the Lenton Thermal designs furnace at 90° C for 30-minutes duration. The substrates are now ready for exposure in UV-light.

Exposure in UV light using Mask Alligner:

A mask aligner manufactured by Neutronix Quintel (model: NXQ 8000ML) is used for exposing the ultraviolet rays of light on the substrate through a negative photomask. The photomask is placed on the substrate in *closed-proximity mode* having a gap separation of 5 micron. The patterns on the soda lime mask block the UV rays at selected regions from reaching the substrate. The exposed regions of the photoresist coated substrate react with the UV rays to form a compound that is soluble in developer solution. The intensity of the UV light is 12 mwatt/cm^2 and the exposure time is 9 seconds.

Photoresist development:

A solution-mixture comprising of deionised water and AZ 351 B Developer is prepared in the volumetric ratios of 5 : 1, respectively. The substrates are immersed in the developer solution and gently stirred for 15 seconds duration. Afterwards, the substrates are rinsed in deionised water. The UV-exposed regions of the photoresist are soluble and thus washed away in the developer solution.

Removal of residual photoresist:

The residual photoresist are etched way using a solution-mixture of deionised water and AZ 100 Remover in the volumetric ratios of 4 : 1 respectively. The substrates are immersed and stirred gently for 50 seconds duration. The substrates are then rinsed in pure deionised water.

Metal deposition and lift-off in acetone:

The aluminium metal is deposited on the substrates followed by lift-off in acetone.

3.3 Electrical Characterization of MOS Capacitors

The fabricated MOS capacitors are characterized by electrical measurement techniques. The capacitance corresponding to an applied gate voltage sweep ($C-V$ characteristics) and gate current corresponding to an applied gate voltage sweep ($I-V$ characteristics) were measured. Moreover, resistance vs. temperature measurements ($R-T$ characteristics) of MOS capacitors were also performed. The various components of the electrical measurement set-up are described below.

3.3.1 Probe station

The substrates comprising of the MOS devices are placed on the substrate-chuck of Signatone probe station as shown in Figure 3.5. The chuck is equipped with a heating facility such that its temperature may be raised from room temperature to 250° C using a Signatone Athena S-1045 controller. Thus the electrical characterizations can be performed at higher measuring temperatures. The chuck is also cooled by water circulation from a chiller manufactured by Therma Electron Corporation (Model: ThermoFlex 1400). The substrates are held to the chuck through vacuum suction. Since the MOS devices have dimensions of 100 micron diameter, the tungsten probe is placed on the devices using PSM-1000 microscope. The characterization is done using two probes: one of the probes are placed on the gate electrode of the device and a high-frequency (HF) gate voltage sweep is applied through it whereas the second one is placed on the electrically grounded substrate chuck. The Signatone probe station, placed within a metallic enclosure, is closed during characterization so that all the measurements are done in dark and electrically shielded conditions.

3.3.2 $C-V$ measurements

The $C-V$ characteristics are measured using a Agilent E4980A precision LCR meter. The measurements may be performed in the frequency range of 20 Hz - 2 MHz. During $C-V$ measurements, an ac signal superimposed on a dc gate voltage sweep is applied at the metal gate of a MOS capacitor. The ac voltage is required for measuring the capacitance but the gate capacitance is displayed as a function of the applied dc voltage sweep. The $C-V$ characteristics were

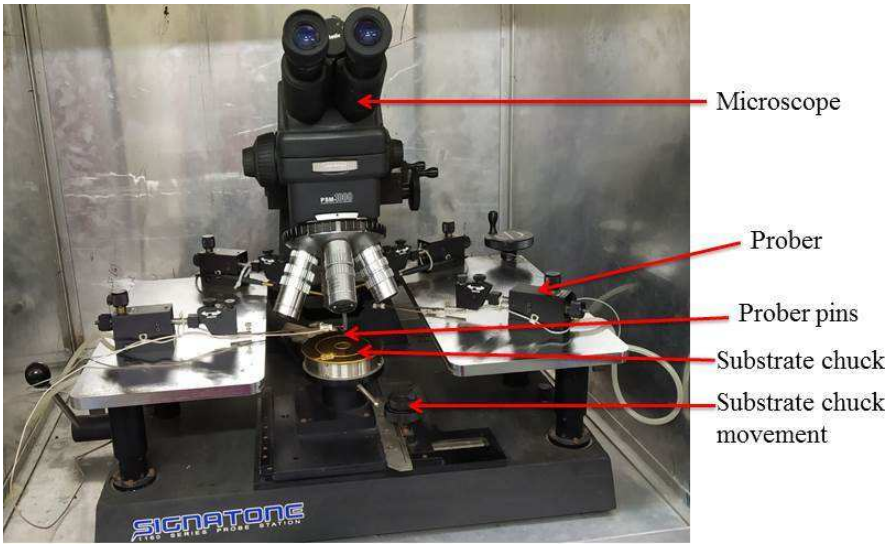

Figure 3.5: A schematic of the Signatone probe station

measured at a frequency of $\sim$ 1 MHz (high frequency characteristics). In order to investigate the interface traps and oxide defects states, measurements are done in the low frequency range. The dc gate voltage sweep is gradually increased during measurements so that the capacitance can reach the *accumulation* state. The conductance can also be measured using the LCR meter. The voltage bias corresponding to the maximum conductance shows the *flat-band voltage*.

3.3.3 $I-V$ measurements

The $I-V$ characteristics are measured using a Keithley 4200-SCS semiconductor parameter analyzer (SPA). It is also equipped with a preamplifier (4200-PA). The gate current is measured corresponding an applied dc voltage sweep.

3.3.4 Switch Matrix

The probers used for measurement, Agilent LCR meter and Keithley 4200-SCS SPA are connected to the Keithley 708A switch matrix. The switch matrix toggles

between the instruments with minimum time delay. The Keithley 708A model acts as a programmable switch that connects signal paths in the form of a matrix topology. This specific model has been designed for switching of relay setups for matrices, having a maximum of 8 rows by 12 columns to 8 rows by 60 columns. The mainframe comprises of three circuit boards and one power supply. Relay cards connecting the mainframe use analog circuits for signal paths while digital circuits for control.

3.3.5 $R-T$ measurements

A LABVIEW-based GUI was used for data acquisition during resistivity measurements. The temperature of the substrate chuck in the Signatone probe station was raised from room temperature (25° C) to 250° C and the resistance of MOS devices may be measured, using a constant voltage/current source. A Keithley based source meter was used for applying a dc voltage bias of 0.5 V and the resistance of MOS devices was measured.

3.4 Physical Characterization of high-κ dielectric and oxide thin-films

The high-κ dielectric films or the oxide films deposited on silicon substrate by sputtering are physically characterized by the techniques described below:

3.4.1 Synchrotron radiation

Electrons/charged particles moving at relativistic velocities in circular orbit are known to emit electromagnetic (EM) radiation. These circular paths arise owing

to the application of a magnetic field in a direction perpendicular to the direction of motion of electrons. These EM radiation are called *synchrotron* radiation (SR). A SR source provides highly intense and coherent x-rays encompassing a broad range of the EM spectrum, starting from the *infrared* to the *hard x-ray* region.

The grazing incidence x-ray diffraction (GI-XRD) and x-ray photoelectron spectroscopy (XPS) characterizations of the oxide thin films were performed at the Angle Dispersive X-ray diffraction (ADXRD) Beamline (BL-12) and the X-ray Photo-Electron Spectroscopy (PES) Beamline (BL-14), respectively of the synchrotron source of storage ring energy 2.5 GeV at Indus-2, Raja Ramanna Centre for Advanced Technology (RRCAT), Indore, India.

A brief overview of Indus Synchrotron source

The accelerator complex of Indus comprises of two sources namely, Indus-1 and Indus-2. The electrons are initially produced and accelerated to energies of order $\sim$ 20 MeV in a *microtron* which is basically a linear accelerator. After reaching the energies of 20 MeV, the electrons are transferred into a *booster* synchrotron wherein their energies are enhanced to 450 or 550 MeV. The electrons of energies 450 MeV are subsequently extracted and transferred to the Indus-1 storage ring and the process is repeated until a current of 100 mA is reached. The electrons of booster synchrotron having energy of 550 MeV are separated and transferred to Indus-2 storage ring. After achieving a desired magnitude of current, the energy of the electron beam in Indus 2 is increased to 2.5 GeV. The Indus accelerators are remotely operated from a control room.

The electron beam of Indus-1 and Indus-2 are made to follow circular paths upon application of a bending magnetic field. In the process, energy is lost and

synchrotron radiation is emitted along a direction tangential to the circumference of the storage ring at that point. A beamline is designed and commissioned at this point. Radio Frequency (RF) cavities are in place which provide the requisite energy for accelerating the electron beam as well as compensating for the energy loss due to emission of synchrotron radiation. The electric fields needed for accelerating the electrons are produced by high power RF amplifiers of the RF cavity.

Angle Dispersive X-ray Diffraction (ADXRD) beamline (BL-12)

The beamline is used for probing the material characteristics of amorphous or crystalline samples by x-ray diffraction (XRD). In contrast to lab-source based XRD, SR-based XRD offers extra benefits owing to much higher intensity and collimated nature of beam. Moreover, the wavelengths of SR beam can be chosen from a wide range of the EM spectrum.

At the BL-12 beamline, *firstly* a pre-mirror made up of platinum collimates the SR beam in the vertical direction. After passing through this, the photon beam is rendered monochromatic by a Double Crystal Monochromator (DCM) comprising of Si(111) crystals. In order to improve the resolution of SR beam, a pair of Si(311) crystals may also be used. Following the passage through DCM crystals, a *second* platinum-coated mirror is in place for vertical collimation of the beam.

The energy range of the x-ray beam at BL-12 may be tuned in the 5-20 keV range with an energy resolution of 1 eV at 10 keV. The experimental hutch comprises of a *Huber-5020* six-circle diffractometer coupled with a *NaI scintillation* detector. An Image Plate Mar-345 area detector is used for recording XRD pattern of powdered samples.

X-ray Photo-Electron Spectroscopy (PES) Beamline (BL-14)

High-energy resolution XPS characterization of samples in the *hard x-ray* regime are performed at the PES beamline (BL-14). It provides an energy range of 2-15 keV. The composition, valence states and electronic structure of the materials in the surface region can be studied. An x-ray beam incident on the material leads to emission of photoelectrons. From the kinetic energy spectrum of the emitted electrons, their binding energies in the sample are determined. Thus an elemental mapping and nature of bonding with other elements are obtained using the XPS technique. A major drawback associated with lab-source based XPS techniques is that these offer information about the probed materials depths of $\sim$ 10 nm. It is known that there is an increase in the mean-free path of electrons with an increase in their energies. The SR provides highly intense x-ray beams covering a wide range of wavelengths/energies. The XPS characterization performed at different energies provides information about the sample at varying depths.

At the BL-14, a toroidal mirror coated with platinum focusses the x-ray beam. The focussed beam passes through a Double Crystal Monochromator wherein a range of x-ray energies upto 15 keV can be chosen. A hemispherical analyzer having high resolution acquires the XPS data. The base pressure of ultra-high vacuum chamber is $\leq 5 \times 10^{-9}$ mbar for investigating the properties of samples. An energy resolution of $\sim 10^{-4}$ is achieved using the hemispherical analyser. The emitted photoelectrons from the samples are detected by a micro-channel plate (MCP) detector comprising of a high-resolution 2D imaging system.

3.4.2 X-ray diffraction

The crystallographic information of both amorphous/crystalline samples are obtained from x-ray diffraction (XRD) data. A diffraction pattern is generated whenever x-rays interact with a crystalline substance. The positions and relative intensities of the constituent peaks in a XRD pattern are the defining characteristics of the material. Upon comparison of the XRD data of a given sample with that of the standard diffraction databases, information about the various constituent phases and their respective crystallographic orientations is obtained. A mixture of various crystalline phases or a crystalline-amorphous phase mixtures can also be separately identified by analysing their XRD pattern and subsequent comparison with standard literature data.

General theory of x-ray diffraction (XRD)

Atoms of a crystalline material are arranged in a ordered fashion at the crystallographic lattice sites. X-rays incident on a material causes the electrons of the respective atoms to vibrate in the same frequency as that of the incident beam. Thus a scattered beam is emitted from the oscillating atoms. The scattered beam may interfere constructively or destructively with the incident beam. When interfering constructively, the scattered beams give rise to the diffraction pattern. The condition of XRD for any material is given by the famous *Bragg's law* which is basically a condition of *constructive interference* between the incident and scattered beams. The Bragg's law may be written as

$$n\lambda = 2dsin\theta \tag{3.2}$$

where d is the inter-planar distance in the crystalline lattice, θ is the angle between the sample surface and the incident x-ray beam, n takes integer values and λ denotes the wavelength of incident x-ray beam. The inter-planar spacing d may be calculated from the Miller indices and the lattice parameters as,

$$d = \frac{1}{\sqrt{\frac{h^2}{a^2} + \frac{k^2}{b^2} + \frac{l^2}{c^2}}} \tag{3.3}$$

where the set (hkl) denotes the Miller indices. The lattice parameters are represented by a, b and c. The position of the Bragg peak in a XRD pattern are denoted by the 2θ values.

In thin-film characterization using ordinary XRD set-up wherein the incident angle is ≥ 4 °, the x-ray beam penetrates through the film and reaches the underlying substrate. Thus signatures of the substrate become evident in the XRD patterns. In order to circumvent this problem, the XRD is performed at grazing incidence angles (GIXRD). In GIXRD, the incidence angle θ is fixed at small values (typically, equal to or slightly higher than the critical angle). The XRD pattern thus generated contains only Bragg peaks belonging to the thin-film and is devoid of any contributions from the underlying silicon substrate. The XRD patterns, recorded for the various samples in this thesis work, were performed at grazing incidence angles. The GIXRD was performed at the Beamline-12 of RRCAT Indore, India as discussed in the preceding section.

3.4.3 X-ray photoelectron spectroscopy

A qualitative and quantitative analysis of elemental composition in a material is investigated by means of x-ray photoelectron spectroscopy (XPS) technique.

Valence states of the constituent elements, bonding between elements and their electronic structure may also be probed. The technique is sensitive to the surface of the sample upto a certain depth as determined by the energy/wavelength of incident radiation. The underlining principle of XPS is Einstein's photoelectric effect. For the compositional analysis of a given sample, it is irradiated with a x-ray beam such that the photon beam interacts with the surface atoms. In the process, the electrons in core energy shells absorb the energy of incident x-rays. In the scenario when energy of incident beam (hv) is greater than the binding energy E_B of electron, it is emitted out of the sample with a kinetic energy E_k. The kinetic energy E_k is directly dependent on the binding energy E_B. Now it is known that E_B of the electron is a characteristic feature of every element. Thus, knowing the energy of incident x-ray beam and measuring the kinetic energy E_k (using a hemispherical analyzer in the x-ray setup), the binding energy E_B may be calculated using the given equation,

$$E_B = hv - E_k - \phi \tag{3.4}$$

where ϕ is a spectrometric correction factor. In general, the C 1s peak lying at a binding energy of 285.1 eV is used as a reference energy level for calibrating the XPS spectra. However for some elements like vanadium, the O 1s energy level at 530 eV serves as a reference energy level.

The XPS characterization performed in this thesis work were carried out using lab-source as well as synchrotron radiation based sources. The synchrotron based XPS facility has been discussed in the previous sections. The lab-source based XPS set-up is described below.

The XPS measurements were performed using a Omicron Multiprobe Electron

Spectroscopy System manufactured by Omicron Nanotechnology, UK. The source of x-rays are provided by monochromated Al Kα at 1486.7 eV (Model: XM 500). The emitted photo-electrons are detected by a 180 ° hemispherical analyser. The analyser is equipped with five channeltron detector. A base-pressure of 2.5×10^{-10} mbar may be achieved in the Omicron system.

3.4.4 Differential Scanning Calorimetry

Any phase transitions or chemical reactions are associated with heat evolution from the system (*exothermic process*) or heat absorption by the system (*endothermic process*). In the differential scanning calorimetric technique (DSC) heat is continuously supplied to or depleted from the sample and a reference, wherein the ramp up or ramp down rates needed to raise/lower the temperatures are kept same. Since the sample additionally undergoes phase transitions or chemical reactions thereby further contributing to heat loss/gain, a difference in supply of heat to the sample and the reference material would be observed. This difference in heat to the sample with respect to the reference are monitored in a DSC setup. The heat loss/gain in a sample due to phase transitions or reactions are depicted in the form of peaks or troughs as a function of temperature or time in a DSC thermogram. A photograph of the DSC instrument is illustrated in Figure 3.6.

The DSC measurements in the present thesis work were performed in a Netzsch 204 F1 DSC setup. It comprises of two holders; one of which holds the sample while the other acts as a reference. The holders are connected to resistive heater equipped with a temperature sensor. Crucibles of Pt or Al may be placed on the heaters. The sample under investigation is placed inside the sample crucible whereas the reference crucible is empty. Same amount of heat is supplied to the

crucibles on the application of currents to the resistive heaters which raises the crucibles' temperatures at a given ramp-up rate. In ideal conditions when both the crucibles are empty, the same value of current suffices for maintaining the crucibles at a given temperature. In contrast when a sample is placed inside the crucible, it additionally undergoes heat gain/loss owing to phase transition/chemical reaction. Thus the currents applied to sample crucible and reference crucible differ while maintaining a given temperature. From this variation in the values of currents, the difference in heat flow is thereby estimated as

$$\left(\frac{dQ}{dt}\right)_P = \left(\frac{dH}{dt}\right) \tag{3.5}$$

(dH/dt) is measured in mJ/sec for a given per unit sample mass in mW/g. The difference in heat supplied to the sample crucible and reference crucible is denoted as

$$\delta\left(\frac{dH}{dt}\right) = \left(\frac{dH}{dt}\right)_{sample} - \left(\frac{dH}{dt}\right)_{reference} \tag{3.6}$$

The sign of $\delta\left(\frac{dH}{dt}\right)$ depends on whether the sample undergoes an exothermic or endothermic process. In case of an endothermic process, the value of $\delta\left(\frac{dH}{dt}\right)$ is positive whereas for an exothermic process the value is negative.

A protective gas flow of N_2 is circulated during a temperature scan for maintaining a dry atmosphere in the vicinity of temperature sensor. The gas flow also prevents oxidation of the sample at higher scan temperatures.

Figure 3.6: A photograph of the differential scanning calorimetry unit

3.4.5 X-ray reflectivity

X-ray reflectivity (XRR) is a surface sensitive characterization tool used for studying thin-films and layered structures. It can also be used to probe the surface characteristics of materials as well as the interfaces of adjoining layers. The basic principle of XRR lies in the phenomenon of total external reflection of x-rays. XRR is used for probing single layer, bilayer or multilayer films [94].

In XRR technique x-rays are made incident on the samples at grazing angles such that the angle of incidence (θ_i) lies near about the critical angle θ_c. In the scenario when $\theta_i \leq \theta_c$, the penetration depth of the incident x-rays are restricted to a few nanometres depth of the sample. For $\theta_i > \theta_c$, the x-rays venture to larger depths of the sample. While penetrating the sample, a part of the incident x-rays are reflected whenever there is a variation in the electron density of the sample. These reflected rays interfere and give rise to oscillations as observed in a reflectivity spectrum. From a thorough analysis of these oscillations, the thickness of the layers, electron-density profile, surface and interface roughness may be derived. The XRR results are invariant to the crystalline/amorphous

nature of the samples.

The intensity of the reflected x-rays is measured in the specular direction wherein the angle of incidence equals the angle of reflection. When the interface is rough, the intensity of the reflected rays will not strictly follow the law of Fresnel reflectivity. These deviations are then investigated for arriving at the electron density profile at the interface normal to the surface. The intensity of x-rays reflected from the layers with varying electron densities at different sample depths are recorded by a detector. The XRR profile is then fitted using Parratt's recursion relations for estimating the various thin-film parameters [95].

In this thesis work, the x-ray reflectivity measurements were performed with a Rigaku Smart Lab diffractometer equipped with a goniometer of 300 mm radius, Cu target and NaI scintillation detector. A Ge 2-bounce and 4-bounce monochromators are present at the incident optics whereas a Ge 2-bounce analyzer is available at the receiving optics.

4

Control of interfacial layer growth during deposition of high-κ oxide thin films in reactive RF-sputtering system

4.1 Introduction

Recent trends in microelectronics demand that the thickness of the dielectric be scaled down to sub-nm regime for metal-oxide-semiconductor (MOS)-based device applications. Such a demand requires an alternative gate dielectric because in the conventional SiO_2-based dielectric with a thickness of 2.5 nm or less there is an increase in gate leakage current, unacceptable to the semiconductor industry. The gate leakage current also degrades the device performance [96, 97]. The researchers have found many high-κ-based materials as alternatives to SiO_2 among which HfO_2 and ZrO_2 are found to be the most suitable candidates [98, 99].

Different deposition techniques namely, dc and rf sputtering, atomic layer de-

position (ALD), pulsed laser deposition (PLD), metal-organic chemical vapour deposition (MOCVD), molecular beam epitaxy (MBE) etc. have been employed to deposit/grow high-κ dielectric gate oxides [100, 101, 102, 103, 104]. It has been found that a growth of low-κ interfacial layer (IL) takes place at the high-κ oxide/Si interface during its deposition [105, 106, 107, 108, 109]. The growth of such an IL takes place in the form of silicon oxide (SiO_x) or metal silicate alloy. The IL reduces the total capacitance of the dielectric stack creating difficulties in scaling down of effective oxide thickness (EOT) to less than 1 nm [110, 111].

Among the above techniques, reactive sputtering technique and ALD have been most widely used to deposit/grow high-κ gate dielectrics. The beginning of the research in this field started with sputtering due to the advantages like better control over the physical properties of the film and the film stoichiometry [112, 113, 114]. But this technique has not been so popular despite its wide availability because of thicker IL growth. The main source of IL growth are the O radicals generated in Ar/O_2 reactive plasma that diffuse through the already deposited high-κ oxide film and react with the underlying Si substrate resulting in the formation of SiO_x IL [115, 116]. Metal silicate and silicide are also formed when the oxide film on Si is subjected to higher temperature annealing process [117].

In order to circumvent IL growth problem, the first and foremost issue is to prevent the O radials from reaching the Si substrate. Interestingly, a decrease in IL thickness enhances the overall device performance due to an increase in the total dielectric constant of the stack [118, 119]. It has been further reported that ~ 7 Å thick IL is necessary for better device performance indicating a requirement of an optimal IL thickness [101, 120].

In view of the above information and technological challenges, this chapter de-

scribes a technique wherein a modification in the plasma chamber of a sputtering deposition system is made to prevent the O radials from reaching the substrate and thereby, a significant reduction in the growth of IL thickness has been achieved. The thickness of IL using the modified sputtering system is within the acceptable limit to get an optimized device performance [101, 120]. This instrumental modification is also very useful for the future use of the sputtering technique to deposit oxide materials, particularly when reactive sputtering is involved. Hafnium oxide is taken here as a representative gate oxide to investigate the performance of the modifications where Ar/O_2 plasma was used for sputtering. The deposited oxide film has been studied using grazing incidence x-ray reflectivity technique (GIXRR). Further, MOS devices are fabricated to investigate the dielectric properties of the deposited films by capacitance-voltage $(C-V)$ measurement.

4.2 Experimental

A sputtering deposition unit (dc and rf) is used here for hafnium oxide deposition. As a part of instrumental modification, a copper grid was placed at a height of $\sim$ 1 cm above the sample stage and fixed to the axle of substrate shutter in such a way that when substrate shutter was fully opened, the grid takes the position of the shutter allowing the deposition to occur through the grid. After a number of trials, a $4'' \times 4''$ rectangular grid area was taken with a separation of 2.6 mm between two adjacent wires. The grid wire was made of copper (without insulation) having a diameter of 0.4 mm. A Keithley 2635 source meter was used to apply bias voltages of 0, -50, -100, -150 and -200 V across the grid where coaxial cable and a vacuum feed through connectors were used to make contact between the grid and source meter. A schematic of the instrumental modification is depicted as Figure

4.1. After modifying the setup, depositions were carried out for 7.5 minutes after attaining a base pressure of 3.14×10^{-6} mTorr at 50 W rf power.

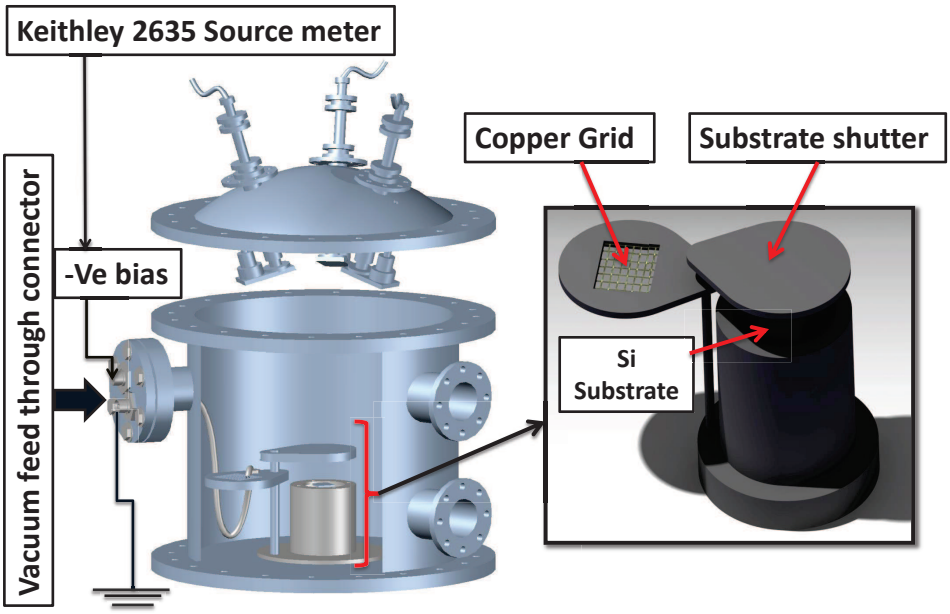

Figure 4.1: Schematic of Sputtering system with rectangular copper grid and vacuum feed through connector.

Hafnium oxide films were deposited at room temperature on n-type Si(100) substrate using 99.99% pure Hf metal target by reactive rf-sputtering at 4:1 Ar/O_2 ratio at a constant pressure of 5 mTorr, controlled by a programmable throttle valve [115]. The Ar/O_2 ratio was controlled by their respective flow rates using mass flow controllers. Before loading the substrates into the chamber, Si substrates was cleaned using standard RCA technique and 1 min-dip in 1% HF to remove organic, metal contaminants and native oxide layer from Si surface, respectively [91].

After the deposition, the x-ray reflectivity (XRR) technique was employed to study the films. The reflectivity measurements were carried out using Rigaku Smart Lab diffractometer equipped with goniometer of 300 mm radius, Cu tar-

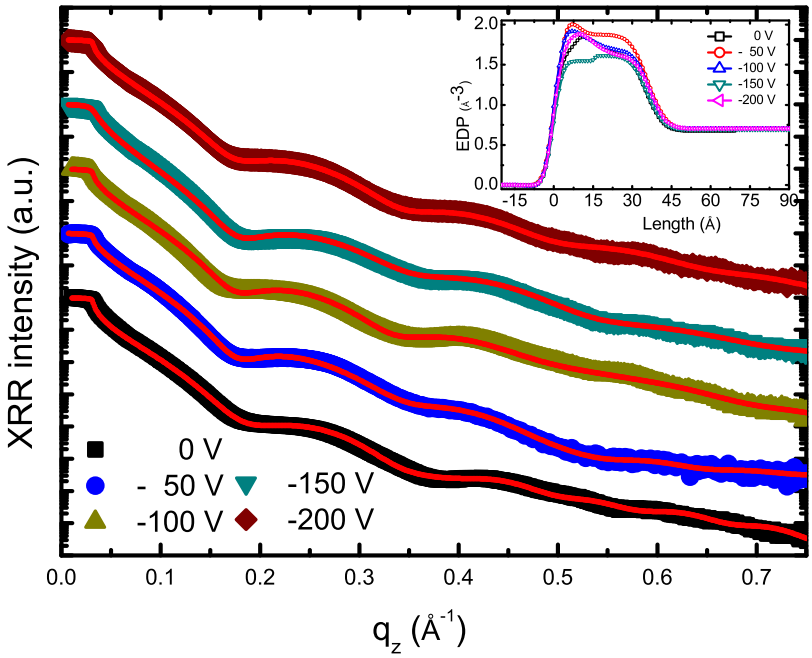

Figure 4.2: GIXRR data of all the samples at different grid bias voltages and electron density profiles (EDP) of all the films are shown in the inset.

get and NaI scintillation detector. The system is also fitted with a Ge 2-bounce and 4-bounce monochromators at the incident optics and Ge 2-bounce analyzer at the receiving optics. A power of 1.3 kW was applied to produce the CuKα_1 x-ray radiation with the wavelength of 1.5406 Å. The extracted data were fitted and analysed using Parrat formalism to study the IL thickness, interface roughness and electron density profile (EDP) for the films, deposited under different grid biases [95]. As the IL was formed between hafnium oxide and Si, a basic three layer model was considered for Parrat fitting followed by a further slicing of each layer in the stack to represent the film precisely. Parameterization of interface roughness and IL thickness has led to the evaluation of EDP. For electrical characterisation, aluminium was deposited on all the samples by electron beam evaporation tech-

nique and gate electrodes of area $5 \times 10^3\ \mu m^2$ were patterned by photolithography with a suitable mask using NXQ 8000 mask aligner. High frequency $C-V$ characteristics were measured at 1 MHz with Agilent E4980A LCR meter connected to Signatone probe station under electrically shielded and light tight condition.

4.3 Results and Discussions

The XRR data and corresponding fitted curves of the hafnium oxide films, deposited under different applied grid voltages are shown in Figure 4.2 and the EDP for all the films are presented at the inset. The oscillations of x-ray intensities as observed in the curves show a variation for the samples deposited under different grid voltages. Figure 4.3 shows the variation of hafinium oxide and SiO_x IL thickness with the applied grid bias. It can be inferred that the thickness of the hafnium oxide layer remains more or less constant with the change in grid bias and the SiO_x IL thickness decreases with the increase in bias voltages. The lowest IL thickness is observed at the grid voltage of -200 volt. The growth of IL thickness during the hafinium oxide deposition can be explained by quenching mechanism [115, 121]. During rf sputtering, in presence of higher Ar ratio in Ar/O_2 plasma (4:1), a large number of reactive O radicals were generated due to quenching reaction and the excited electrons present in the Ar/O_2 plasma follow the reactions:

$$e + O_2 \rightarrow e + O^* + O \tag{4.1}$$

$$e + O \rightarrow e + O^* \tag{4.2}$$

$$O + ne \rightarrow O^{n^-} (0 \leq n \leq 2) \tag{4.3}$$

Table 4.1: Parameters obtained by XRR analysis of oxide layers and capacitance values obtained by $C-V$ measurements of all the films at different grid bias voltages.

Grid voltage (V)	Hafnium oxide thickness (nm)	Roughness of Hafnium oxide (Å)	SiO_x IL thickness (nm)	Roughness of SiO_x (Å)	Total thickness (nm)	Total Capacitance (pF)	Dielectric constant of total oxide stack (κ_{eff})
0	3.5	2	3.5	5	7	26	4.11
-50	3.6	2	2.5	5	6.1	38	5.24
-100	3.6	2	1.3	5	4.9	70	7.75
-150	3.6	2	0.8	5	4.4	80	7.95
-200	3.7	2	0.6	4	4.3	114	11.1

$$Ar^M + O_2 \rightarrow Ar + O + O \tag{4.4}$$

The above reactions show that the density of O radicals is high at 4:1 Ar/O_2 gas mixture due to the presence of meta-stable Ar atoms i.e. Ar^M in the reactive plasma [115, 116]. These O radicals comfortably penetrate through the hafnium oxide/Hf stack due to their smaller radii and react with underlying Si substrate resulting in the formation of SiO_x IL between the hafnium oxide film and Si substrate. The O radicals, generated in the plasma were repelled by the negative bias voltages applied across the copper grid. As the applied negative voltage was increased from zero to -200 volt, the O radicals got lesser chance to reach the substrate surface and to form SiO_x IL penetrating through the already deposited hafnium oxide film. Figure 4.3(a) clearly depicts that higher negative voltage causes greater repulsion of reactive O radicals resulting in lesser thickness of SiO_x IL. The error bars shown in the curves correspond to their respective roughness. It is further observed that the surface roughness of hafnium oxide films is more or less constant for the depositions at 0 and -200 V grid biases. As the IL thickness at -200 volt attains almost a saturation level, this voltage is considered here as the limiting voltage and therefore, no further higher bias voltage was applied.

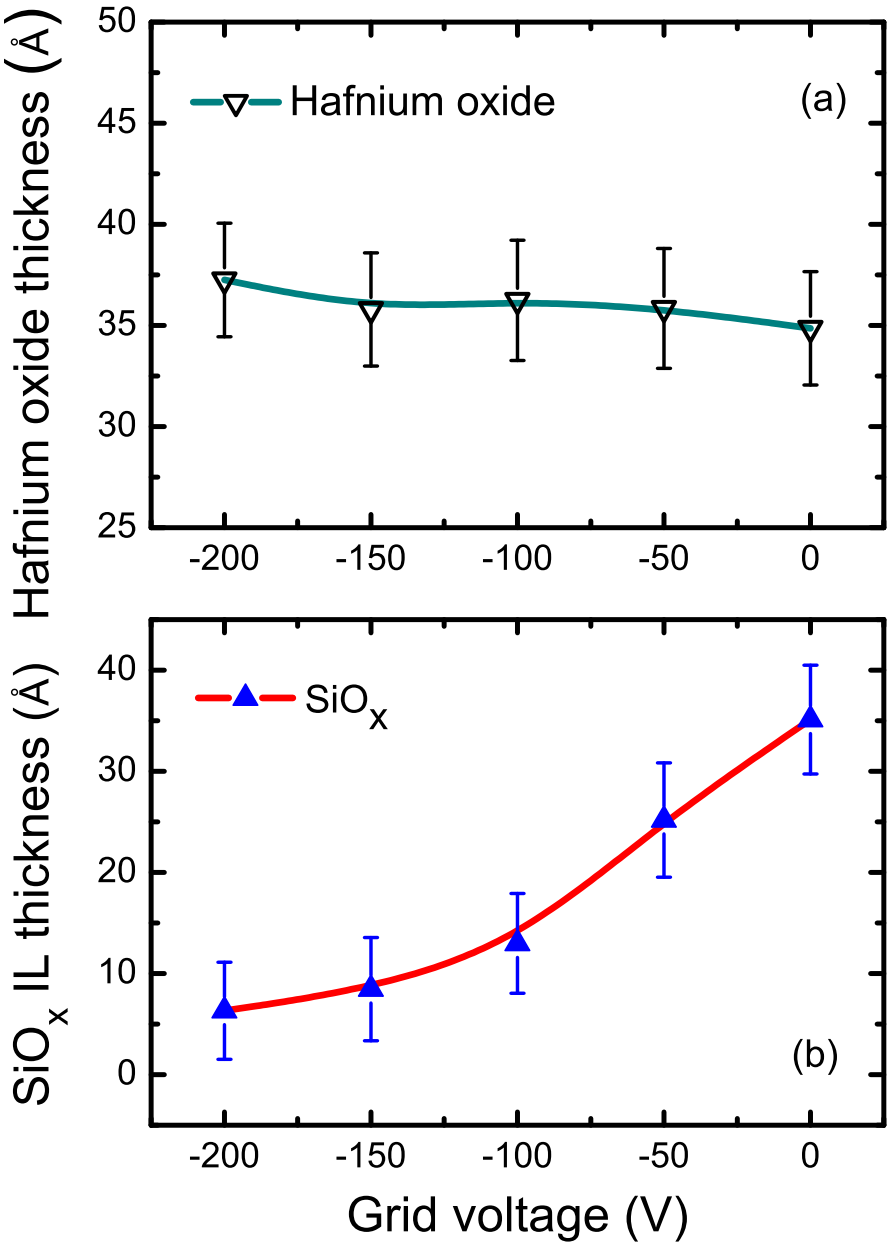

Figure 4.3: (a) Thickness of SiO_x IL at different grid bias voltages. (b) Thickness of Hafnium oxide at different grid bias voltages. (Blue SiO_x and Brown Hafnium oxide error bars indicate the corresponding roughness.)

The various results of the XRR data analysis and high frequency $C-V$ characteristics at different grid bias voltages are described in Table 4.1. The thickness

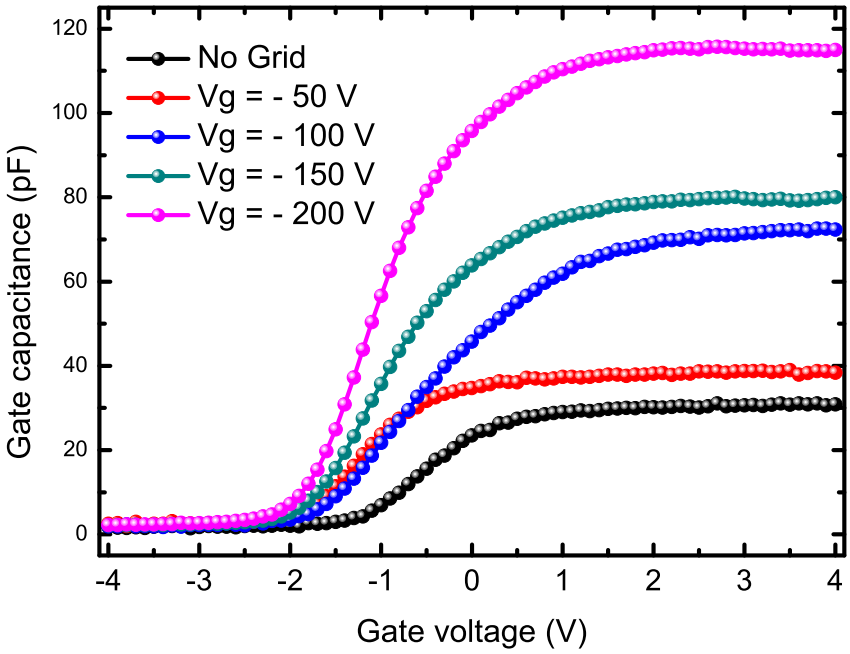

Figure 4.4: $C-V$ curve of all the samples at different grid bias voltages.

and roughness of the films were obtained from XRR fitting using Parratt formalism, as described before. The total capacitance of the oxide stack was obtained from the accumulation capacitance of high frequency $C-V$ characteristics (Figure 4.4). The effective dielectric constant κ_{eff} was indirectly calculated from the total oxide film-thickness, accumulation capacitance and area of gate electrodes. It is evident from Table 4.1 that the IL thickness decreases with the applied bias voltages that in turn decrease the gate dielectric constant and EOT of the total dielectric layer. The high frequency $C-V$ characteristics also corroborate the above observation indicating an excellent improvement of total capacitance of the devices. It is further evident from the table that the effective dielectric constant of the total oxide stack was approximately 4.1 at zero grid bias that increases to

11.1 at -200 V bias across the grid. A gradual improvement at -50, -100 and -150 volt is also observed from the $C-V$ curve.

The effective dielectric constant of hafnium oxide films on silicon substrate deposited by reactive sputtering of a pure hafnium metallic target in Ar/O_2 atmosphere is found to be in the range of $\sim$4 to 8 [105, 122, 123, 124, 125]. In all the above cases, the substrate temperature was kept at room temperature and no post-deposition annealing (PDA) process was performed. The dielectric constant of the HfO_2 films improved only after PDA treatment at temperatures ranging from 300 °C - 900 °C [124]. In one case, annealing at 700 °C yielded a dielectric value of 13.5 for HfO_x/Si samples [126]. In each of these reported works, heat treatment on the as-deposited films enhanced the dielectric value of the as-deposited HfO_x films leading to the standard value of stoichiometric $HfO_2(\kappa = 22)$. So, the dielectric constant increases with increasing annealing temperature [125].

In the work undertaken in this chapter, annealing was neither involved at the time of deposition nor during post-deposition device fabrication because the objective of the study is to reduce the growth of interfacial SiO_x layer. Therefore, an effective κ value of 4.1 at zero grid bias and keeping the substrate at room temperature is reasonable when reactive sputtering is involved. On the other hand, we are able to increase the effective κ value to 11 only by applying a negative grid bias of 200 V without any treatment including post deposition annealing. Annealing of as-deposited HfO_x films beyond a certain temperature changes the film microstructure from amorphous to crystalline state. Further, the hafnium silicate content at the interfacial layer is also increased at higher annealing temperature [117]. These factors are responsible for enhancing the effective dielectric constant of the stack.

Moreover, it is to be noted that the deposited hafnium oxide films are not pure stoichiometric HfO_2. It is further known that the κ value may vary with the oxygen content of the films [127]. An appreciable change in the effective κ value is also observed depending on the target (pure ceramic HfO_2 target or pure metallic Hf target) used during reactive sputtering [100].

4.4 Conclusion

In summary, during deposition of any high-κ material oxide in reactive sputtering, it is possible to control the IL growth at Si/hafnium oxide interface by applying negative bias across the copper grid placed closer to the substrate. It is clearly observed that at higher negative bias voltage, lesser IL growth is achieved due to the blocking of O radicals, generated in the Ar/O_2 plasma from reaching the Si substrate. The XRR data and the $C-V$ characteristics also corroborate the above observation. A simple modification of the sputtering instrument makes the technique more popular for its use in the deposition of oxides on silicon.

5

Effect of oxygen content on the electrical properties of sputter deposited vanadium oxide thin-films

5.1 Introduction

Vanadium Oxides(VO) exhibit different stoichiometry owing to the multivalent character of the vanadium cation. In the various known oxide phases, the oxidation state of vanadium ranges from +2 (as in VO) to +5 (as in V_2O_5), with V_2O_5 being the most stable phase [128]. These oxide phases have garnered significant interest due to their widespread applications in memory [129, 130], photonics [131] and optoelectronic devices [132]. Some of these devices mainly hinge on the phase-change material characteristics of vanadium oxide [133, 134] undergoing a metal-to-insulator (MI) phase transition [135, 136]. The temperature for insulator-to-metal (IM) transition is the highest in V_3O_5 at about 150 °C [42]. Deposition

methods of vanadium oxide thin-films involve sputtering [137, 138], atomic layer deposition [139], pulsed laser deposition [140, 141] and electron-beam evaporation [128, 141]. Chemical Vapor deposition (CVD) technique has also been tried to grow VO at elevated temperatures wherein it was revealed that oxide phases of vanadium depend only on growth temperatures [142]. An attempt was also made to grow VO on SnO_2 pre-coated glass substrates by atmospheric pressure chemical vapor deposition at higher temperatues at various N_2 flow rates in the absence of oxygen wherein the film was found to be amorphous in nature. However a short-range crystalline ordering was revealed due to the presence of monoclinic VO_2 for N_2 flow rates at 4 L/min [143]. Extensive works have been done using sputtering where a subtle interplay of the different growth/deposition conditions, results in a variety of vanadium oxide films which differ in their stoichiometry, phase and the oxidation state of vanadium. Further, modulation of the ratios of Ar and O_2 in reactive sputtering results in oxide films with variable oxidation states and stoichiometry [137, 144]. Therefore, in order to use the phase change and metal-insulator-transition(MIT) property of vanadium oxide in any electronic devices, a knowledge of the oxidation states of vanadium in the oxide film is required beforehand.

With a motivation to gain the apriori knowledge, this chapter deals with characterization of reactively sputtered vanadium oxide thin-films, deposited at different Ar/O_2 ratios on silicon substrate at room temperature, by x-ray photoelectron spectroscopy(XPS). Further, metal-VO-semiconductor (MOS) structure, fabricated with aluminum as gate electrode, was used to study its IM transition properties. The results are presented and discussed here.

5.2 Experimental

n-type Si(100) substrates having 1 $cm \times 1$ cm area and resistivity 1-10 $\Omega - cm$ were used for VO thin-film deposition. The substrates were cleaned by standard technique of Radio Corporation of America (RCA) followed by a 1 min-dip in 1% HF acid for native oxide removal. Vanadium oxide films were then deposited at room temperature on these substrates by reactive rf-sputtering of 99.9% pure vanadium metal target at various Ar:O_2 ratios. The deposition was carried out for 30 min at a constant pressure of 5 mTorr and 70 W rf-power. The ratios of Argon and oxygen were controlled by modulating their respective flow rates using mass flow controllers and a constant pressure was maintained by programmable throttle valve. The partial pressure of oxygen in the plasma was varied from 20% to 80%. A rotation of 30 rpm was given to the substrate in order to ensure the film uniformity. X-ray reflectivity measurements revealed that the thickness of the deposited films was in 5-7 nm range.

The films were then probed using x-ray photoelectron spectroscopy (XPS) technique to identify the the oxidation states of vanadium in the samples. The XPS measurements were taken with a Omicron Multiprobe Electron Spectroscopy System (Omicron Nanotechnology, UK) equipped with a monochromated Al Kα (1486.7 eV) (Model: XM 500) source. The base pressure of the Omicron system was 2.5×10^{-10} mbar. The binding energy of V 2p and O 1s were measured in a single energy window and a pass energy of 30 eV. Usually, the C 1s is used as the reference for binding energy calibration in XPS spectra. But for vanadium oxide, the O 1s signal is a far better reference than C 1s for the V 2p binding energies [145, 146]. The signals for O 1s and V 2p were measured together in one

energy window. The XPS data were analyzed using CasaXPS processing software. The background of the spectra was subtracted using a Shirley background function. Apart from the V signal, the O 1s signal needs to be taken into consideration for extracting the Shirley background [145]. The overall XPS spectra was de-convoluted into various peaks corresponding to different oxidation states of vanadium. A convolution of Gaussian-Lorentzian functions was used for fitting the peaks and the overall spectra. Si spectra were also deconvoluted in a similar manner and Si 2p, SiO_2 and SiO_x peaks were identfiied. A 200 nm-thick aluminum metal was then deposited on the top of VO using electron beam deposition system. The metal was then patterned to gate electrodes of 100 μm diameter using UV-photolithography. The separation between two gate electrodes is 25 μm.The I-V characteristices of the devices were then measured in a Signatone(1160 series) probe station using keithley 4200-SCS equipped with keitheley-made 4200-PA premaplifiers. All the measurements were carried out at room temperature and under light tight and electrically shielded conditions.

5.3 Results and Discussions

5.3.1 *Analysis of XPS Data for vanadium and oxygen :*

The XPS spectra of vanadium oxide film deposited at 4:1 Ar:O_2 ratio is illustrated in Figure 5.1(a). The deconvolution of the spectra reveals five major peaks. A peak at 530 eV denotes the O 1s level and corresponds to the O-V bonds [128, 145]. The peak for O 1s level does not show any significant shift for the VOs deposited at increasing oxygen partial pressures but a growing asymmetry on the higher binding energy (BE) side of O 1s level is quite evident from Figure 5.1(b)-(d).

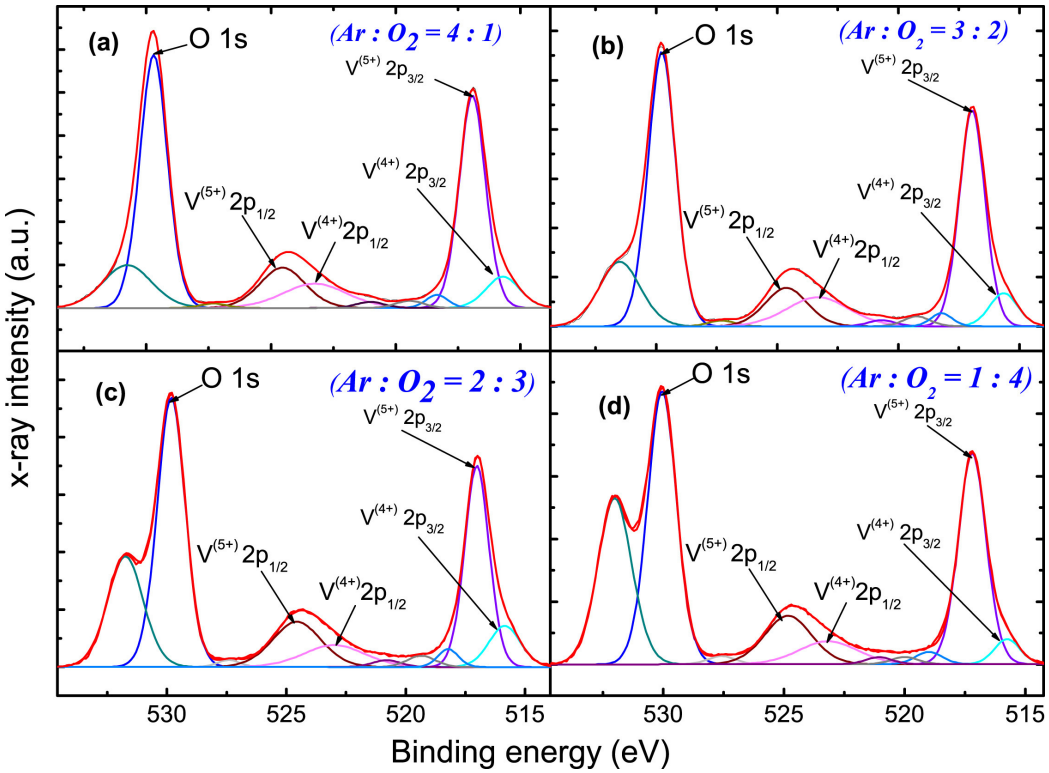

Figure 5.1: XPS spectra of vanadium oxide reactively sputtered in varying ratios of Ar to O_2 (a) Ar : O_2 = 4 :1 (b) Ar : O_2 = 3 :2 (c) Ar : O_2 = 2 :3 (d) Ar : O_2 = 1 :4

The O 1s level serves as a reference for fitting the V 2p spectrum. Figure 5.1(a) shows a narrow and sharp feature, deconvoluted into two peaks at 516.93 eV and 515.71 eV, representing the V^{5+} $2p_{3/2}$ and V^{4+} $2p_{3/2}$ levels, respectively. The deconvoluted peaks at 524.54 eV and 523.25 eV corresponds to V^{5+} $2p_{1/2}$ and V^{4+} $2p_{1/2}$ peaks [145, 147, 148]. Besides these major energy levels, a number of less intense satellite peaks are also present. These V 2p satellite peaks are a result of strong hybridization between the V 3d and O 2p energy levels and are necessary for appropriate fitting of the XPS spectra [149, 150]. Since the peaks corresponding to the various oxidation states of vanadium might undergo a shift, the difference in BE between the O 1s and V $2p_{3/2}$ level is an appropriate measure of determining

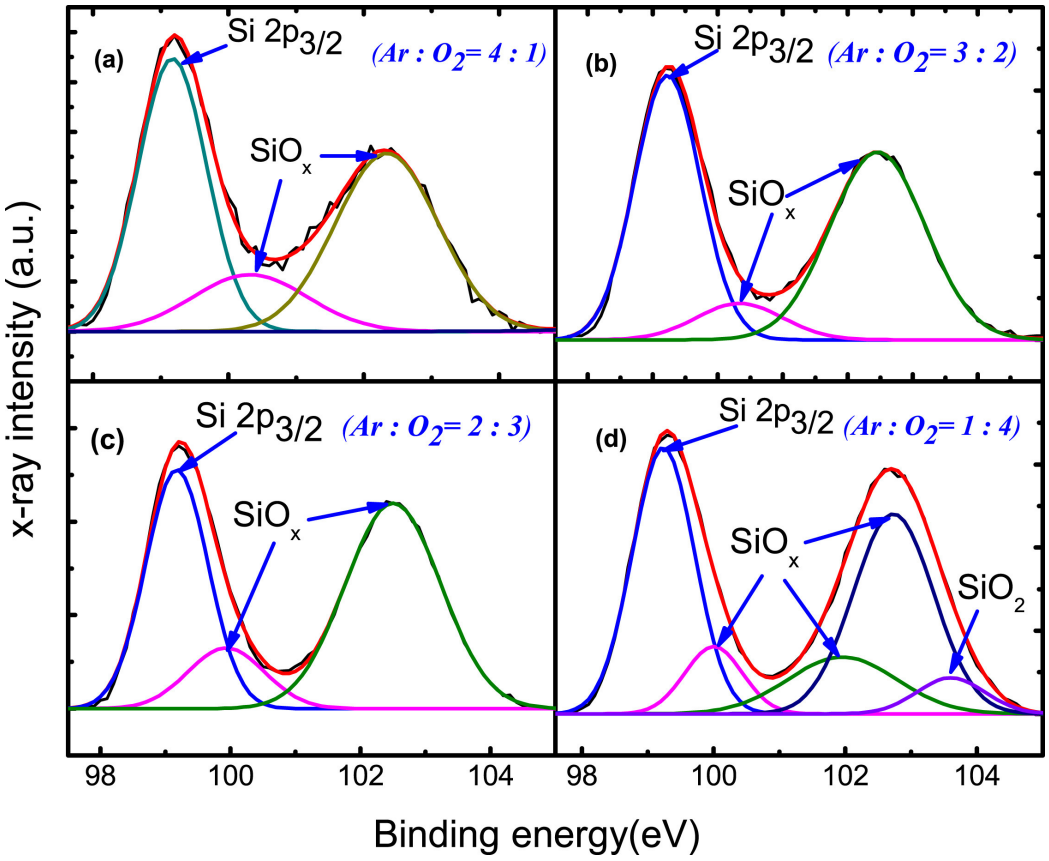

Figure 5.2: XPS spectra of silicon oxide interfacial layer for vanadium oxide reactively sputtered in varrying ratios of Ar to O_2 (a) Ar : O_2 = 4 :1 (b) Ar : O_2 = 3 :2 (c) Ar : O_2 = 2 :3 (d) Ar : O_2 = 1 :4

the oxidation state of vanadium [145, 146]. In the different XPS spectra (Figure 5.1), the BE for O 1s and V^{5+} $2p_{3/2}$ differ by 12.8 eV. This difference for V^{4+} $2p_{3/2}$ comes out to be 14 eV. Both these values match with literature data for vanadium oxides [145, 147]. Due to spin-orbit coupling, the V 2p spectrum is split into V $2p_{3/2}$ and V $2p_{1/2}$ levels, differing by 7-8 eV [148, 150]. Taking this difference into account, the V^{5+} $2p_{1/2}$ and V^{4+} $2p_{1/2}$ levels have been correctly represented by the peaks at 524.54 eV and 523.25 eV. Thus, all the major peaks representing the various oxidation states of vanadium have been accurately denoted.

The XPS spectra for the VO samples, deposited at increasing oxygen partial

pressure, are shown in Figure 5.1(b)-(d). It can be seen that the V^{5+} $2p_{3/2}$ peak gradually shifts to higher BE values with increasing oxygen partial pressure. The BE of V 2p level is known to increase with the increasing oxidation state of vanadium cation [145]. Thus the above shift with increasing oxygen partial pressure, signifies that the amount of V_2O_5 in the film is gradually increasing. On the other hand, V^{5+} $2p_{1/2}$ shift does not show a continuously increasing trend however there is an overall shift to higher BE values from 524.54 eV to 524.83 eV for the samples deposited at 4:1 and 1:4 Ar:O_2 ratios, respectively. The V^{4+} peak shifts show a discontinuous trend.

However, the evolution of the feature at 531 eV contributing to the asymmetry of O 1s level is quite interesting. At lowest oxygen partial pressure, this feature is not so signifcant. But with increasing oxygen partial pressure, its intensity becomes prominent and finally renders a doublet structure to the O 1s level as shown in Figure 5.1(c) and (d). The peak at 530.76 eV has been associated with V^{5+} as mentioned above.

A more quantitative assessment of film content is presented in Table 5.1. The highest amount of V_2O_5 is present in the film reactively sputtered in 10 sccm of Ar and 40 sccm of O_2 along with the presence of VO_2. The VO_2 is maximum in the film deposited under 20 sccm of Ar and 30 sccm of O_2. Thus a proper choice of the ratios of Ar to O_2 can significantly alter the film content.

The various component peaks of the V 2p spectrum has a corresponding satellite peak on the higher BE side in the vicinity of the O 1s level. The satellite peak for the V^{4+} $2p_{3/2}$ level occurs in between the O 1s and V $2p_{1/2}$ level. This is represented by the very less intense peak at 527 eV as evident from Figure 5.1(a). The V^{5+} $2p_{1/2}$ has a satellite peak at 540 eV (not shown in the spectra). The V^{5+}

$2p_{3/2}$ and V^{4+} $2p_{1/2}$ levels have their satellite peaks on the higher BE side of the O 1s level [145, 150]. This can render an explanation for the peak at around 531 eV which makes the O 1s level asymmetric. This asymmetric feature becomes more prominent with increasing oxygen partial pressure and eventually attains a doublet structure. A doublet structure in the O 1s spectrum, shown in Figure 5.1(c) and (d), is usually associated with the presence of V_2O_5 (V^{5+} in the sample) [151]. V^{5+} $2p_{3/2}$ is separated from its satellite peak, appearing on the higher BE side of O 1s, by 14-15 eV as reported earlier [150]. In Figure 5.1, this separation comes out to be $\sim$ 14 eV. Thus the growing asymmetry with increasing partial pressure is a signature of increasing amount of V^{5+} in the sample. Besides these, three small peaks lying adjacent to one another in the 518-521 eV range are added [152] for rendering a proper fit to the entire spectra. The V 2p XPS spectra does not show any peak corresponding to the BE of vanadium silicate. This was expected as no annealing/heat treatment were performed on the as-deposited films. Moreover, the VO were reactively sputtered at room temperatures. Under these conditions, the deposited VO do not react with underlining silicon substrate and thus vanadium silicate is not formed.

Table 5.1: Relative content of different oxidation states of vanadium and oxygen in the film, corresponding to different ratios of Ar to O_2

Ratios of Ar to O_2	V^{5+} (%)	V^{4+} (%)	O (%)
4 : 1	56.17	16.07	27.75
3 : 2	54.36	15.9	29.73
2 : 3	52.53	17.27	30.18
1 : 4	58.49	11.17	30.33

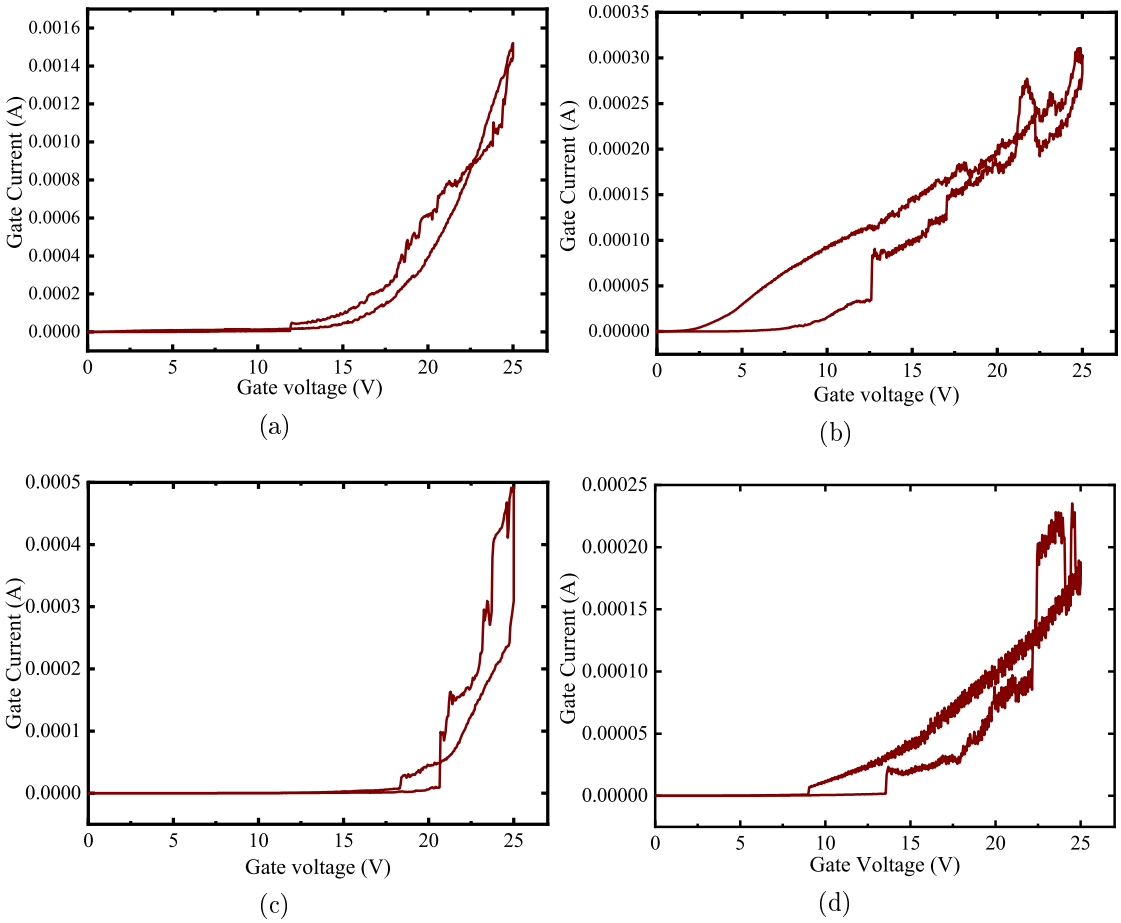

Figure 5.3: Gate-current (in linear scale) corresponding to applied Gate-voltage sweep of vanadium oxide films reactively sputtered in varying ratios of Ar to O_2 (a) Ar : O_2 = 4 : 1 (b) Ar : O_2 = 3 : 2 (c) Ar : O_2 = 2 : 3 (d) Ar : O_2 = 1 : 4.

5.3.2 *Analysis of Si 2p XPS peak :*

The Si 2p XPS spectra for all the samples, deconvoluted into various peaks, are revealed in Figure 5.2 (a-d). A major component peak of this spectra is the Si $2p_{3/2}$ peak occurring at around 99 eV for all the films deposited at various Ar : O_2 ratios. Apart from this peak, several less intense peaks occurring in the range of 100-102 eV in each of the spectra denote the SiO_x structure. An additional peak occurring at around 103.60 eV as evident from Figure 5.2(d) for the film deposited

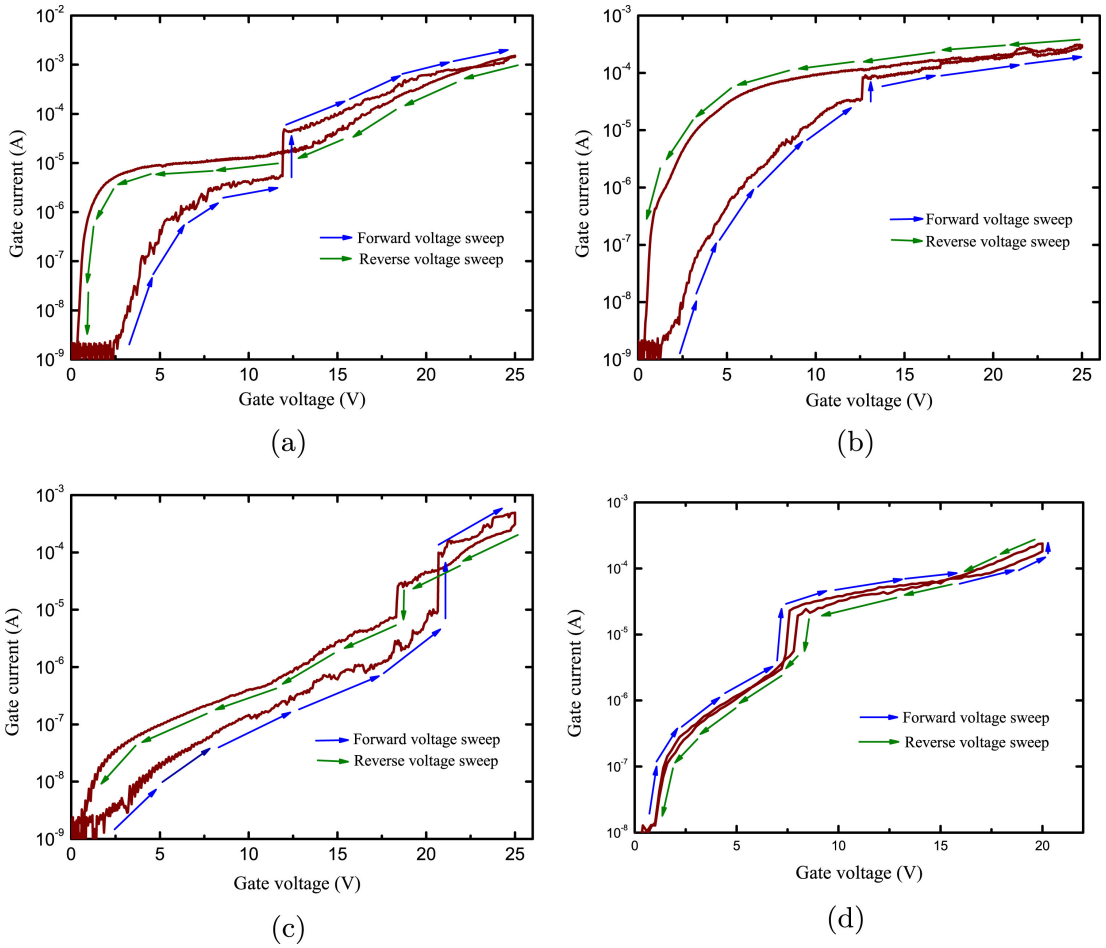

Figure 5.4: Gate-current (in logarithmic scale) corresponding to applied Gate-voltage sweep of vanadium oxide films reactively sputtered in varying ratios of Ar to O_2 (a) Ar : O_2 = 4 : 1 (b) Ar : O_2 = 3 : 2 (c) Ar : O_2 = 2 : 3 (d) Ar : O_2 = 1 : 4.

in Ar : O_2 = 1 : 4 corresponds to the BE of SiO_2 [153]. Thus the appearance of SiO_2 in the XPS spectra signifies the onset of complete oxidation of SiO_2 in the presence of highest oxygen partial pressure. Further the SiO_x peak for the sample, deposited at highest oxygen partial pressure located at a higher binding energy, $\sim$ 0.5 eV more than the one at lowest oxygen ratio indicates SiO_2 structure [154].

5.3.3 *Electrical characterization :*

The I-V characteristcs of all the devices in logarithmic scale are shown in Figure 5.4. It is evident from the figure that the VO, deposited at higher O_2 partial pressure (Ar : O_2 = 2:3 and 1:4) show an insulator to metal transition as shown in Figure 5.4 (c) and (d). No appreciable reversible IM transition is observed for the devices, deposited at other Ar : O_2 ratios. Low oxygen partial pressures in the reactive plasma lead to an increase in oxygen vacancies, which in turn imparts a metallic character to the film in conjugation with the voltage-induced joule heating phenomenon. It directly follows from Figure 5.4 (a) and (b) that the insulator-to-metal transition is irreversible indicating that the metallic nature of the films are preserved even though the driving-voltage is reduced. When a large voltage is applied across the device at room temperature, voltage-induced Joule heating takes place within the device that is responsible to form a conduction channel [66, 70]. The Joule heating effect is applicable for small devices. In the case of temperature-induced MIT, the entire film becomes metallic but in voltage-induced MIT, metallization of only part of the film takes place, resulting in small current change at MIT [66]. An asymmetry in heating power before and after the MIT is responsible for maintaining the temperature of the device near the MIT temperature [155]. The XPS study also reveals that oxygen content at the surface is higher than that at the inner of the thin-films. Moreover, excess oxygen makes the surface more metallic. Therefore, the insulator to metal transition takes place at lower voltages with increasing O_2 content in the film [156, 157].

In the voltage-triggered IMT phenomenon, preservation of metallic character upon the reduction of applied voltage is evident by the appearance of a hysteresis in the *I-V* characteristics [77, 158]. This may be attributed to the large num-

ber of oxygen vacancies in these films which play an equally important role as voltage-induced Joule effect. From Figure 5.4 (c) and (d) we conclude that the IMT phenomenon is reversible which indicates that the oxide-films reverts back to the insulating state once the applied gate-voltage is reduced. Since the deposited films in this case are deposited under higher oxygen partial pressures (60 % and 80 % respectively), the amount of oxygen vacancies are less and the films are more stoichiometric. Thus the role of oxygen vacancies in preserving the metallic character is minimal and the voltage-induced joule heating is the dominating phenomenon. Hence the hysteresis in the I-V cycle is less profound and the oxide-film switches back to an insulating state.

5.4 Conclusion

Vanadium Oxide thin-films were reactively sputtered at different ratios of Ar and O_2 and the deposited films were then probed using XPS technique. Afterwards, the VO films were fabricated into MOS structures for the purpose of electrical characterization. A qualitative assessment of the XPS spectra reveals that vanadium exists in the V^{5+} and V^{4+} oxidation states in the oxide thin-films. The film content shows a marked variation with increasing oxygen partial pressure in the reactive plasma. The highest content of V_2O_5 is present in the oxide film deposited under 10 sccm of Ar and 40 sccm of O_2 (Ar:O_2=1:4). Whereas, the film deposited at 20 sccm of Ar and 30 sccm of O_2 has the highest VO_2 content (Ar:O_2=2:3). In all the films, V^{5+} is the major occurring oxidation state, comprising nearly about 55 % of the film content. The growing asymmetry in the O 1s level which finally gives rise to a doublet structure (Figure 5.1 (c)-(d)) can be related to the increasing V^{5+} content in the film. The satellite peak on the higher B.E. side of

O 1s corresponds to the V^{5+} $2p_{3/2}$ energy level. Presence of excess oxygen in the reactive plasma makes the film surface more metallic. Thus, the ratios of Ar and O_2 in the reactive plasma play a critical role in determining the film characteristics. Gate current measured for the corresponding gate voltage sweep in the MOS devices demonstrated that the films deposited at Ar : O_2 ratios of 2 : 3 and 1 : 4 undergo a insulator-to-metal transition. This marked transition is not prominent in the rest of the devices deposited under lower O_2 ratios. Thus the IM transition takes place at lower voltages and becomes increasingly prominent in O_2 rich film.

6

Insulator-to-metal transition of vanadium oxide-based metal-oxide-semiconductor devices at discrete measuring temperatures

6.1 Introduction

Oxide-based devices namely, HfO_2, ZrO_2 and ZnO have widespread applications in the fields of memory, magnetics, photonics, spintronics and short wavelength optoelectronics-based devices [159, 160, 161]. Vanadium oxides (VO) have been incorporated in several device structures which serve applications in memory [162, 163], field-effect transistors [65], photonics [131, 164] and selectors [165]. These devices mostly utilize the insulator-to-metal transition (IMT) properties of vanadium oxide films [133]. The classic example is VO_2 which undergoes a reversible

metal-insulator transition at ~ 68 °C accompanied by a structural phase transition (SPT) from the monoclinic to rutile phase [166]. The IMT can be triggered by increasing temperatures [60] or upon an application of electric field to the device [167]. The phenomenon of electric-field induced IMT (E-IMT) has been attributed to a voltage-induced Joule heating effect [66], whereby excessive heating of the device gives rise to a localised metallic conduction channel at the onset of IMT. Recent studies also ascribe the origin of IMT in VO_2 to strong electron correlation due to increasing carrier density resulting in band-gap collapse [58]. While others have concluded that both the Joule-heating and carrier-concentration models are at play which simultaneously drive the IMT [77]. Generally, it has also been found that IMT in vanadium oxide is accompanied by a SPT as in VO_2 [68, 166]. This makes the question open whether SPT or Joule heating or both are responsible for IMT in VO. In this chapter an attempt has been made to address the above question where vanadium oxides, reactively sputter-deposited in different Ar/O_2 ratios at room temperature, were studied by differential scanning calorimetry (DSC) to identify the temperature dependent phases of VO. Synchrotron-based grazing incidence x-ray diffraction (GIXRD) measurements were then performed on the as-deposited films at room temperature and elevated substrate temperatures. Afterwards, the *I-V* characteristics of Al/VO/Si-based MOS devices were measured at higher substrate-chuck temperatures (25 to 200 °C) to study the role of VO phases on IMT. The results are presented and the underlying mechanisms of IMT are discussed.

6.2 Experimental

n-type Si (100) wafer having resistivity of 1-10 $\Omega - cm$ was used for depositing VO thin-films. Si wafer, cut into several 1 $cm \times 1$ cm pieces, was cleaned using Radio Corporation of America (RCA) cleaning technique [91] followed by a 1 min-dip in 1 % HF solution. The substrates were then loaded into the sputtering chamber. A 99.9 % pure vanadium target was reactively sputtered at four Ar:O_2 ratios for depositing vanadium oxide films on Si(100) substrates at room temperature. A rf-power of 70 W, a constant pressure of 5 mTorr and 30 rpm substrate rotation were maintained during the deposition where the deposition was carried out for 30 min. The samples deposited at different ratios have been outlined in the Table 6.1. The thickness of the deposited films as calculated from grazing incidence x-ray reflectivity (GI-XRR) technique were found to vary in 5-7 nm range depending upon the respective Ar/O_2 ratios.

Table 6.1: Sample nomenclature corresponding to vanadium oxide films reactively sputtered in different ratios of Ar to O_2.

Sample name	Ratio of Ar to O_2
V1	4 : 1
V2	3 : 2
V3	2 : 3
V4	1 : 4

The samples were then studied using Netzsch 204 F1 DSC setup for identifying the various VO phases. The temperature was varied from room temperature to 650 °C with a ramp-up rate of 10 °C/min. It was observed that the DSC signals for the various oxide films had a broad hump in two temperature ranges viz.

60 - 200 °C and 400 - 600 °C. In order to extract information about the various oxide phases of vanadium, the obtained DSC signals in the abovementioned temperature ranges were subsequently processed using PeakFit software. After using a suitable linear function for background subtraction, the overall DSC spectra was deconvoluted into several peaks. A convolution of Gaussian-Lorentzian functions was used for rendering an appropriate fitting to the component peaks and the overall spectra. GIXRD measurements of the samples at room temperature and at elevated substrate temperatures were performed at the angle dispersive x-ray diffraction beamline (BL-12) of the synchrotron source of storage ring energy 2.5 GeV at Indus-2, RRCAT Indore, India. The wavelength of the beam was 0.790437 Å. A six-circle diffractometer (Huber 5020) with scintillation point detector was used. The measurements were carried out only for the samples deposited at minimum and maximum O_2 partial pressure (pO_2). For the purpose of carrying out electrical-characterization, a 200 nm-thick aluminum metal was deposited on the top of VO using electron beam deposition system and then patterned by UV-photolithography to get 100 μm-dia gate electrodes. A schematic of the metal-oxide-semiconductor (MOS) device is shown in Figure 6.1. The I-V characteristics of the MOS devices were measured using keitheley 4200 semiconductor parameter analyser equipped with 4200-PA amplifier and a signatone probe station with heating chuck facility. The I-V characteristics of the devices were measured from 25 °C to 200 °C. The gate voltage was swept in a cyclic manner from 0 V$\rightarrow$+15 V$\rightarrow$-15 V$\rightarrow$0 V and the corresponding gate current was measured. Following this, the gate voltage was again swept from 0 V$\rightarrow$-15 V$\rightarrow$+15 V$\rightarrow$0 V and the gate current measured. All the measurements were carried out at room temperature and under light tight and electrically shielded conditions.

6.3 Results and Discussions

6.3.1 *DSC Curves Analysis*

The DSC Spectra obtained for all the deposited oxide films are taken from 25 to 600 °C. Since the Signatone-based S-1045 temperature controller offers a maximum temperature of 250 °C, we restrict our analysis in the 60 °C - 200 °C temperature range. Accoridngly, the spectra have been deconvoluted into their component peaks and are shown in Figure 6.2. The deconvoluted peaks for sample V1 have been illustrated in Figure 6.2 (a). The peak at 74.16 °C denotes the phase transition of vanadium oxide from the monoclinic to rutile phase (VO_2(M)$\leftrightarrow$$VO_2$(R)) responsible for the first order reversible IMT [168, 169]. VO_2 films deposited by physical vapour deposition (PVD) methods are known to undergo a shift in their phase transition temperature with varying ratios of argon to oxygen [170]. Thus the same peak occurs at 72.97 °C in the case of sample V2 (Figure 6.2 (b)) and is absent for the samples V3 and V4. The largest area under the curve is discernible for the peak at 146.47 °C. This temperature has been attributed to the phase transition temperature of V_3O_5 [171]. This phase transition is also accompanied by a lattice rearrangement [172]. It is quite evident from Figure 6.2 that the peak at 146 °C also undergoes a shift with varying ratios of Ar to O_2. It has been elsewhere reported [173] that the DSC curves of pure VO_2 (A) and a phase-mixture of VO_2 (M) and VO_2 (A) contain peaks at 161.47 °C and 173.43 °C, respectively. The phase transformation of VO_2(A) at 161.85 °C identified by differential thermal analysis, both during the heating and cooling cycles, have been reported [174, 175]. Thus the peaks at around 160 °C and 175 °C in Figure 6.2 denote the phase transformation of VO_2 (A). It has been concluded from various

studies that bulk V_2O_5 shows no signs of IM transition [176, 177]. In our earlier work, it has been observed that the surface of as-deposited VO becomes V_2O_5 rich with the increase in O_2 content in the Ar:O_2 plasma [178]. The peaks at 100 and 120 °C in Figure 6.2 are thus being assigned to the phase transition of V_2O_5. These two peaks undergo shift (Figure 6.2(a)-(d)) depending upon the relative oxygen content in the reactive plasma.

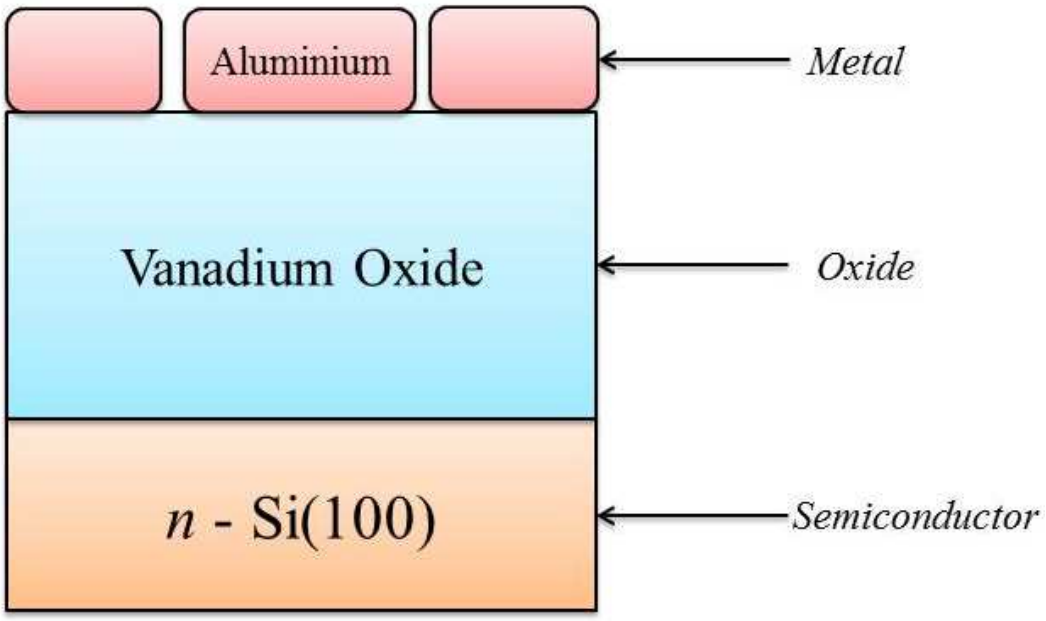

Figure 6.1: A schematic diagram of MOS device.

6.3.2 *GIXRD data Analysis*

The GIXRD data of the devices V1 and V4 are illustrated in Figures 6.3 and 6.4. A close comparison of the room-temperature data reveal that the as-deposited V1 film is polycrystalline whereas V4 is mostly amorphous in nature. It is reported for vanadium oxide films deposited by reactive rf-sputtering that the increase in ratio of oxygen to vanadium atoms (O/V ratio) results in a lower crystalline character

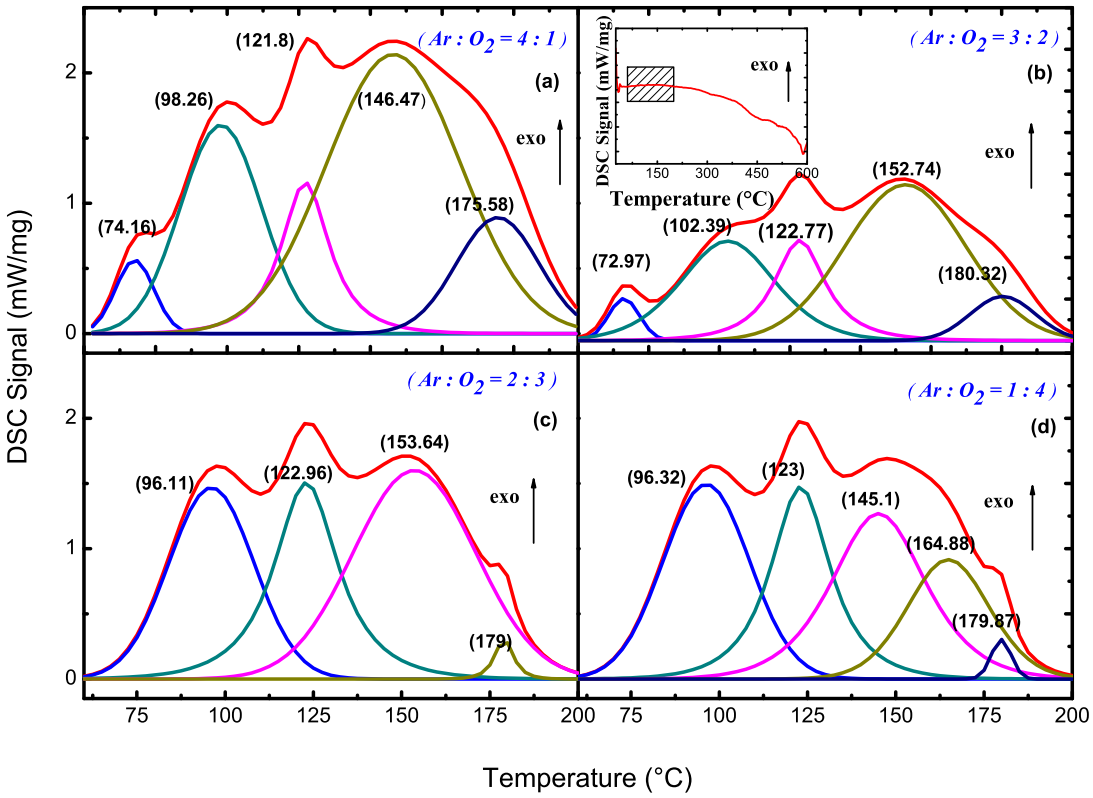

Figure 6.2: DSC Signal with temperature for vanadium oxide reactively sputtered in varying ratios of Ar to O_2. The samples are (a) V1 (b) V2 (c) V3 and (d) V4. The inset in (b) represents the entire DSC scan from 25 °C to 600 °C.

of the as-deposited films [179]. Moreover, the thin-films sputter-deposited under higher oxygen partial pressure in the reactive plasma are mostly amorphous, although the V_2O_5 content is maximum in those films. From our earlier work [178], x-ray photoelectron spectroscopy(XPS) study reveals that the O/V ratio is 0.3841 for the V1 film whereas it is 0.4354 for the V4 film. Since the O/V ratio is more for V4 and it is deposited under higher oxygen partial pressure in the reactive plasma, it has an amorphous character whereas V1 is crystalline. This suggests that the crystalline nature of the films decreases with increasing pO_2 and the film deposited at highest pO_2 is amorphous. Afterwards, the GIXRD of V1 and V4 were carried out at elevated substrate temperatures. Considering the DSC data and transi-

tion temperatures of various VO phases, a few discrete temperatures were set for GIXRD and *I-V* measurements. Accordingly, substrate temperatures for V1 were set at 78, 90, 125, 145 and 155 ^{o}C and that for V4 were 100, 130, 145 and 160 ^{o}C. At 78 ^{o}C, peaks at 2θ values of 22.63^o, 23.12^o, 26.14^o, 37.13^o and 40.51^o become more intense, thereby signifying that the as-deposited films are becoming crystalline with increasing temperatures. The various crystalline phases corresponding to the observed peaks were identified using PCPDFWIN (JCPDS-International Centre for Diffraction Data 2003) software. VO_2 (M) ($\bar{6}$ 0 1) crystalline phase is ascribed to 2θ value of 22.63^o. The peak at 26.14^o denotes the V_3O_5 (5 1 0) phase whereas 37.13^o represents the V_2O_3 (2 2 0) phase. V_2O_5 (1 3 1) crystalline phase formation takes place at 40.51^o. The peak positions and the occurrence of corresponding crystalline phases remains unaltered with increasing pO_2 as suggested by the GIXRD data of V4. The increase in peak intensity for further rise in temperatures beyond 78^{o}C indicate that the various constituent oxide-phases of vanadium become more crystalline with increasing substrate temperatures. It is further observed that the peak intensity for various VO phases decreases at certain temperature indicating a decrease in crystallinity of the respective planes.

6.3.3 *Electrical Characterization*

The *I-V* characteristics of the MOS devices are shown in Figures 6.5 and 6.6 for V1 and V4 devices, respectively. Considering the volume of data and information, the *I-V* properties of V1 and V4 devices are presented and discussed here. The substrate temperature was increased in steps of 5 °C starting from 25 to 200 °C and the electrical characteristics were measured at the respective temperatures after a reasonable delay for temperature stabilization. A thorough analysis of the graphs

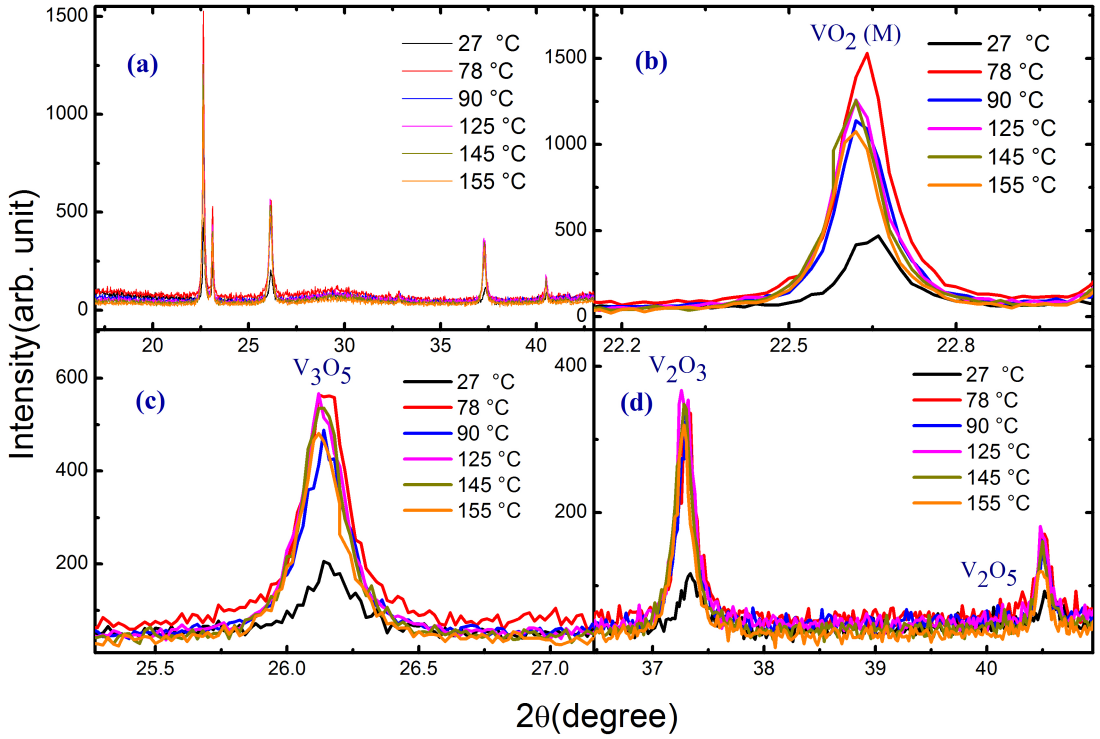

Figure 6.3: GIXRD measurements performed on sample V1 at room temperature and at elevated substrate temperatures. The obtained data for various 2θ values are displayed as (a) entire spectrum from 20^o to 45^o (b) VO_2 (M) phase (c) V_3O_5 phase and (d) V_2O_3 and V_2O_5 phases, respectively.

reveals noteworthy observations. It is evident from the Figures 6.5 and 6.6 that the onset of IMT takes place once the applied voltage stress reaches a threshold value (V_{Th}) and the sample switches from an insulating to metallic state, marked by a sharp change in the magnitude of current (Figure 7). The ON/OFF ratio of IMT for VO-based MOS devices becomes very prominent (3 to 4 orders of change in magnitude of current) at/near certain measurement temperatures. These sharp changes in current are mostly around 100 °C, 120 °C, 145 °C and 160 °C as evident in Figure 6.5 and Figure 6.6, respectively. A close comparison with Figure 6.2 reveals that these discrete temperatures correspond to formation of VOs with different oxide phases. Thus a direct correlation between the electrical characteristics

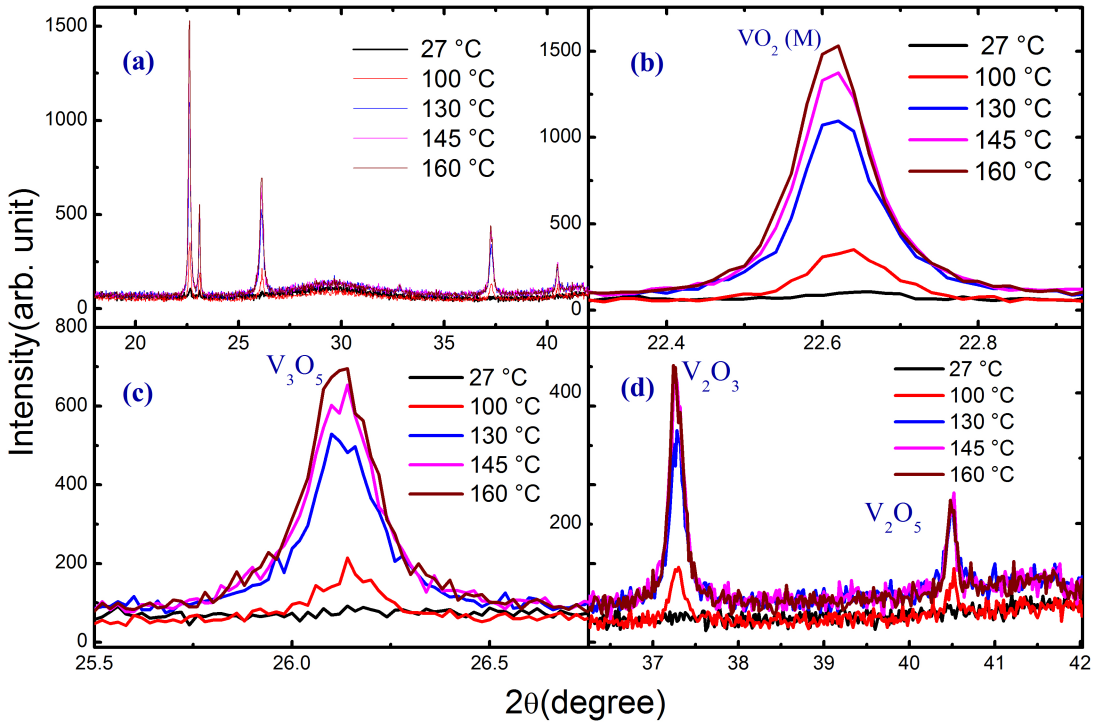

Figure 6.4: GIXRD measurements performed on sample V4 at room temperature and at elevated substrate temperatures. The obtained data for various 2θ values are displayed as (a) entire spectrum from 20^o to 45^o (b) VO_2 (M) phase (c) V_3O_5 phase and (d) V_2O_3 and V_2O_5 phases, respectively.

and DSC data is observed. The ON/OFF ratio of IMT is large at those measuring temperatures which are associated with a transition of VO as also evident from the deconvoluted DSC spectra. Another observation is that for those temperatures where the IMT is large, a large hysteresis in the I-V characteristics is found (Figures 6.5(e) and 6.5(h)). Moreover, there are certain intermediate temperatures (as in Figures 6.5(b) and 6.5(d)) where neither IMT takes place nor any hysteresis in the I-V characteristics is observed. These temperatures lie in between the temperatures where prominent IMTs are observed. It is also discernible from Figures 6.6(b) and 6.6(h) that the current varies linearly with gate-voltage sweep without any trace of IMT at those temperatures. In its totality, the threshold voltage of

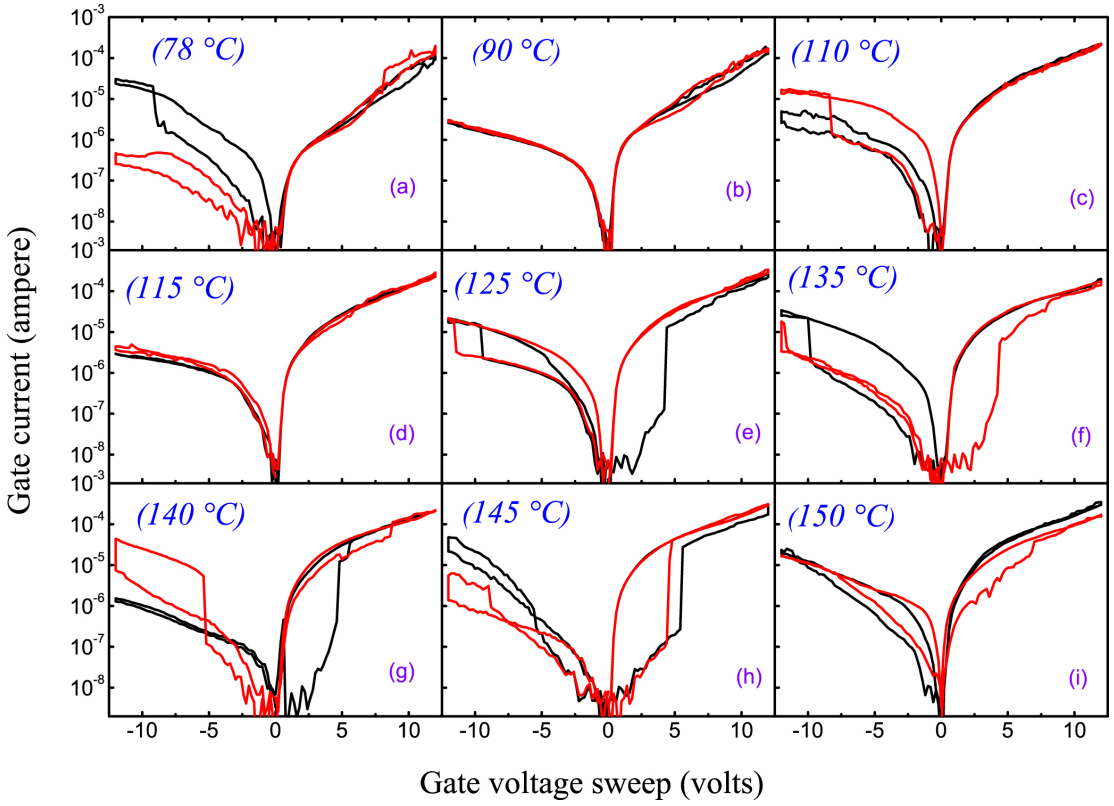

Figure 6.5: Gate-current corresponding to applied Gate-voltage sweep for the MOS device V1 at different measurement temperatures of the sample chuck. Black curve represents the current measured for the 0 V→+15 V→-15 V→0 V sweep. Similarly, red curve denotes the current measured for 0 V→-15 V→+15 V→0 V sweep

IMT is also found to be reduced to $\sim$ 5 V with increasing substrate temperatures as depicted in Figures 6.6(e) and 6.6(h). The IMT phenomena occur upto 150 °C for sample V1 and 160 °C for sample V4 and no IMT is observed beyond that temperatures upto 200 °C.

In order to decipher the underlying reasons from these observations, let us look at the driving mechanisms behind electrically-triggered IMT (E-IMT). Some studies attribute these transition solely to a voltage-induced Joule-heating effect [71] resulting in the formation of a localised metallic conduction channel across an otherwise insulating vanadium oxide dielectric [66] while others reveal a purely

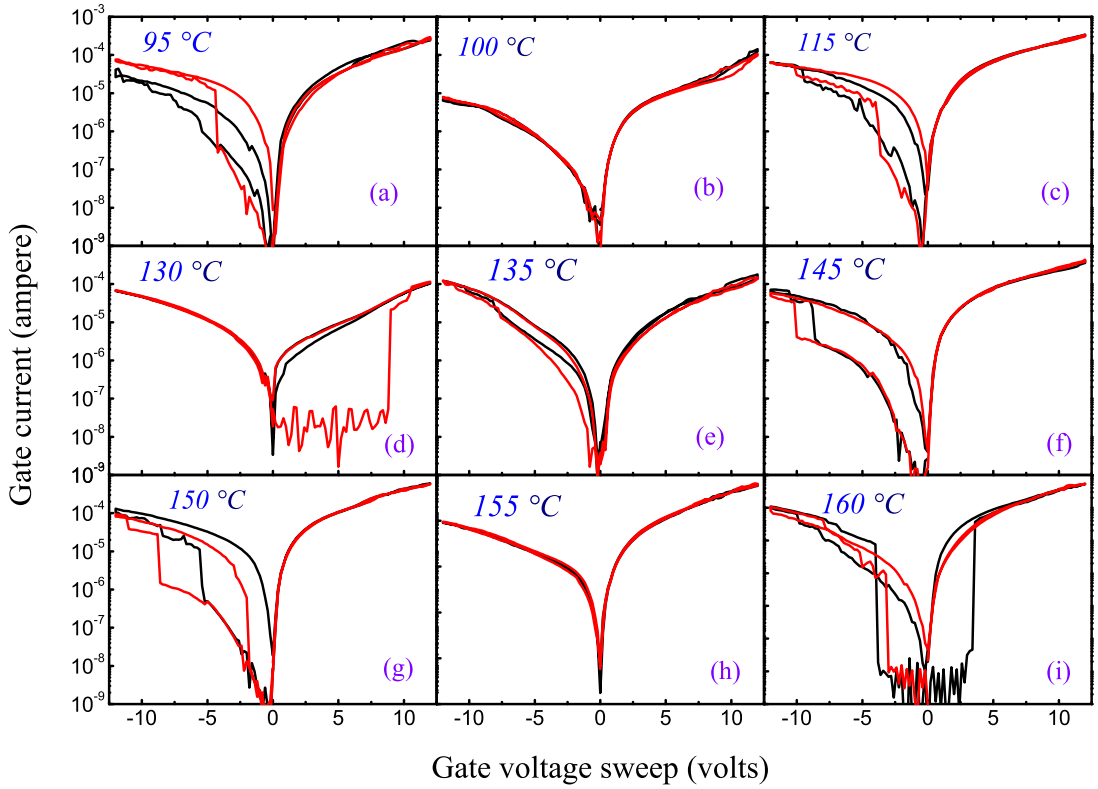

Figure 6.6: Gate-current corresponding to applied Gate-voltage sweep for the MOS device V4 at different measurement temperatures of the sample chuck. Black curve represents the current measured for the 0 V→+15 V→-15 V→0 V sweep. Similarly, red curve denotes the current measured for 0 V→-15 V→+15 V→0 V sweep

electronic phenomena where an applied electric field increases the carrier density, in turn inducing an IMT [58, 180]. An intriguing aspect which complicates the understanding is the fact that a SPT is generally associated with IMT as in our results (Figures 6.2 and 6.5-6.6). In a pure Joule-heating induced IMT, the magnitude of current-jump at a critical threshold voltage solely depends on the applied voltage [77]. It is observed from Figures 6.5 and 6.6 that the ON/OFF ratio of IMT is dependent not only on the magnitude of applied voltage but also on the polarity of applied voltage sweep. The IMT is more prominent during the positive voltage sweep as depicted in Figure 6.7. This indicates that electron injection rather than

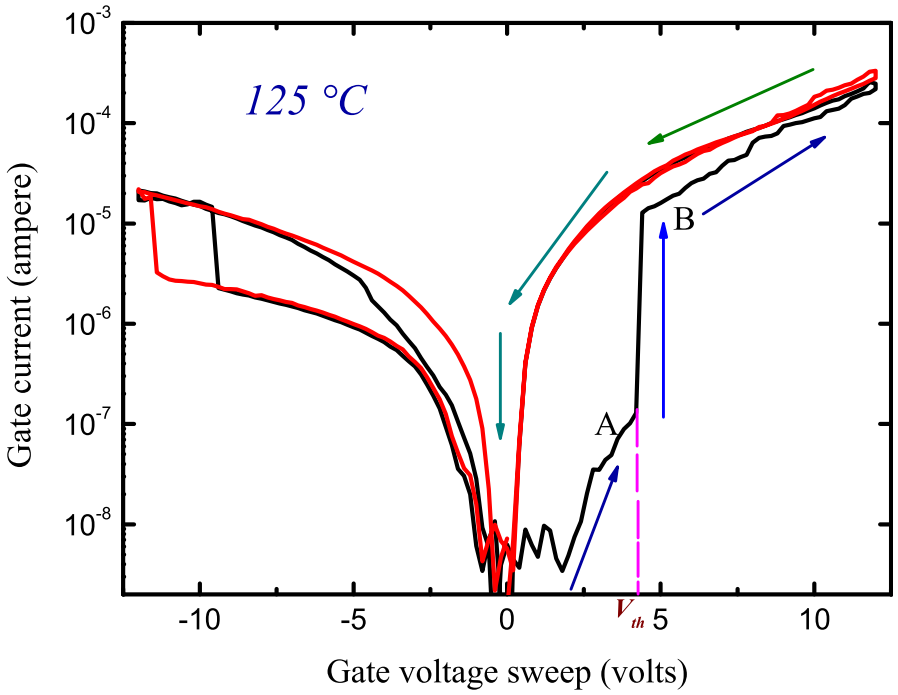

Figure 6.7: Gate-current corresponding to applied Gate-voltage sweep for the MOS device V1 at a substrate-chuck temperature of 125 °C. V_{Th} is the threshold voltage of IMT. Once the applied voltage reaches V_{Th}, the device switches from an insulating state (marked by point A) to a metallic state (marked by point B).

hole injection from the n-Si(100) substrate into the vanadium oxide layer is more effective in modifying the carrier concentration and helps in triggering IMT. It is reported that IMT as a result of voltage stimulus in vanadium oxide can also be described by a purely electronic phenomenon whereby the band-gap collapses with increasing electron density due to strong electron-electron Coulomb interaction and the sample gains a metallic character [1, 58]. The I-V characteristics in Figures 6.5-6.7 are supported by this purely electronic model, since prominent IMT with 3 orders change in the magnitude of current occurs during positive voltage sweep. During 0 V $\rightarrow$ +15 V sweep, electron injection from n-Si(100) substrate into the VO layer increases electron density resulting in a band-gap collapse and in turn causing an IMT.

Thus Joule-heating does not initiate the IMT [1, 181] and explain the *I-V* characteristics in Figures 6.5-6.7. The IMT is initiated by a change in electron-carrier concentrations due to electron injection from *n*-Si(100) substrate into the VO layer, triggered by the applied electric field [182]. This results in a sudden-jump in the current at the threshold voltage V_{Th} which in turn causes Joule-heating and increases the device temperature [1, 58]. Although the IMT in devices V1 and V4 can be explained by a purely-electronic model involving electric-field induced carrier injection, it fails to explain the accompanying hysteresis in the *I-V* characteristics. In Figure 6.5 (h) prior to applying a gate-voltage sweep, the substrate temperature is set at 145 °C which happens to be the critical-temperature (T_c) at which V_3O_5 undergoes a structural phase transition (SPT) as evident from Figure 6.2 (a). Though the substrate temperature is set at 145 °C, the actual temperature of the MOS device saturates at lower values due to heat loss in a dissipative system [77]. In order to explain a hysteresis associated with the IMT, let us refer to the points A and B in the *I-V* characteristics of device V1 measured at a substrate temperature of 125 °C as depicted in Figure 6.7. When the applied voltage is less than the threshold value V_{Th} (point A), the current flowing across the device is small since the device is still in an insulating state. Thus for applied bias less than V_{Th}, heating due to Joule effect is not sufficient by itself to cause a SPT. The IMT at point A is triggered initially by electric-field induced carrier injection from *n*-Si(100) substrate into the oxide layer that results in a sudden jump in current. This sudden increase in current now generates significant amount of heat due to Joule-effect which further contributes to IMT and drives the device to a metallic state, marked by point B. Once the device reaches state B heating due to Joule-effect causes a SPT [77, 158]. Thus in its totality, once the applied voltage

reaches V_{Th} the increase in carrier concentration triggers IMT which increases the current flowing through the oxide layer. This in turn causes heating of the device due to Joule-effect and afterwards this vicious cycle continues resulting in a large ON/OFF ratio (3-order change in the current) of IMT (Figure 6.7). Once the device reaches the metallic state B, Joule-heating drives the device temperature beyond T_c and finally causes a SPT [183]. The IMT and SPT occurs at the same threshold voltage although the SPT occurs at a higher temperature than the IMT [68]. This explains the large jump in current (3 to 4 orders of change in ON/OFF ratio) at a given threshold voltage (as in Figures 6.5 (e)-(h)) when the measuring temperature happens to be near the T_c of phase transition (Figure 6.2). Thereafter, heating due to Joule-effect dominates and persists even when the applied voltage is reduced and the system remains metallic even when the voltage is gradually reduced. It has been pointed out that heat production due to Joule-effect scales with cube of device size and heat loss due to thermal dissipation scales with square of device size [184]. As the heat generated due to Joule-effect dissipates slowly, the metallic state B of the device V1 is retained even when the applied voltage is reduced ($+15\ \text{V} \rightarrow 0\ \text{V}$) which finally renders a hysteresis to the I-V characteristics (Figure 6.7). Moreover, the decrease in threshold-voltage of IMT with increase in measuring temperature is consistent with a Joule-heating model [182].

The increase in magnitude of IMT (ON/OFF ratio) at elevated substrate temperatures is also observed in Figures 6.5 and 6.6 that may be associated with increased crystalline character of VO_2 and V_2O_3. It has been reported that the magnitude of IMT enhances with the increasing crystalline character of vanadium oxide films and that the measurement of temperature dependent I-V characteristics crystallizes the as-deposited films [185]. Thus, it is expected that the mag-

nitude of IMT in the temperature-dependent *I-V* characteristics of V1 and V4 should continuously increase with increasing measuring temperatures. Contrary to this trend, our results demonstrate that the IMT is absent at certain intermediate temperatures (Figures 6.5(b), 6.5(d), 6.6(b) and 6.6(h)). Tadjer *et al.*, prepared amorphous VO_2 films by atomic layer deposition (ALD) which were subsequently annealed to maintain crystalline VO_2 phase [185]. However, formation of any V_2O_5 phase was supressed, since V_2O_5 does not exhibit IMT. GIXRD measurements of V1 and V4 at elevated temperatures (Figures 6.3 and 6.4) reveal the presence of crystalline phase-mixtures of VO_2, V_3O_5, V_2O_3 and V_2O_5. Crystalline VO_2 and V_2O_3 phase-mixtures contribute to a larger ON/OFF ratio in an IMT whereas crystalline V_2O_5 does not exhibit IMT. Considering the Figures 6.3(b) to (d) and 6.4(b) to (d) it is revealed that crystalline nature of different VO phases is reduced at certain temperatures where IMT is absent. The observations indicate that the constituent crystalline and amorphous phase mixture of the VO films play an important role in finally affecting the magnitude of IMT. It may be further concluded that a trade-off between various crystalline and amorphous phases of VO gives rise to a large IMT at certain substrate temperatures whereas an absence of IMT at other temperatures.

6.4 Conclusion

The phase dependent insulator-to-metal transition (IMT) of vanadium oxide (VO)-based metal-oxide-semiconductor (MOS) devices was studied at higher measuring temperatures where the different VO phases were identified by DSC and GIXRD techniques. A change in crystalline to amorphous nature of the as-deposited films are observed with increasing pO_2. The *I-V* trends reveal an E-IMT phenomena

at certain discrete temperatures corresponding to the phases of VO. When the applied voltage stress reaches a threshold value, IMT is triggered by a change in electron concentration due to carrier injection from n-Si(100) substrate into the vanadium oxide layer. The sudden increase in current causes heating of the device due to Joule-effect and afterwards this vicious cycle continues resulting in a large ON/OFF ratio of IMT. Once the device has been driven to a metallic state, heating due to Joule effect dominates and persists even when the applied voltage is reduced. As the heat generated due to Joule-effect dissipates slowly, the metallic state of the device is retained even when the applied voltage is reduced. This renders a hysteresis to the I-V characteristics. It is further observed that IMT is absent at certain intermediate temperatures due to the various constituent crystalline-phase mixtures. Crystalline VO_2 and V_3O_5 phases contribute to a large magnitude of IMT whereas V_2O_5 does not exhibit IMT. The temperature dependent quantized IMT suggests a trade-off between crystalline and amorphous phases of VO. In a nutshell, the IMT is not due to the sole effect of applied electric field. Local rise in film temperature close to its IMT temperature through Joule heating also contributes to the IMT.

7

Effect of oxygen content and crystallization temperature on the insulator-to-metal transition properties of vanadium oxide thin-films

7.1 Introduction

Insulator−to−metal transition (IMT) in vanadium oxide (VO) films is a widely studied phenomenon [58, 135, 186]. This characteristic feature of IMT in VO has been integrated into device structures which serves a plethora of applications in memory [163], selectors [187], photonics [188] etc. The IMT in VOs may be triggered by external stimulus such as temperature [59] or electric field (E−IMT) [58]. The E−IMT in VO films deposited by reactive sputtering of vanadium metallic target is largely dependent on the experimental parameters such as Ar/O_2 ratios in

the plasma [178] and the measuring temperatures [189]. Besides these, the amorphous/crystalline character of the as-deposited films also plays an equally crucial role in determining the magnitude of IMT. Although reports on a direct relationship between the crystalline quality of VO films and the IMT characteristics are scarce, VO films deposited by atomic layer deposition (ALD) exhibited improved IMT characteristics after crystallization [185]. The nature of IMT is also influenced by the deposition temperatures [190, 191]. The role of deposition temperature and oxygen content on the IMT propeties of the VO film was also reported [192]. But a relationship between the IMT properties with crystallization temperature is not yet available. It is widely studied that the IMT phenomenon in VO passes through a stage wherein a metallic conduction filament/channel emerges across the insulating VO [66]. Considering the above scenario, this chapter describes the effect of crystallization of the films on the IMT properties of VO thin−films.

7.2 Experiment

$n-$type Si (100) wafers having resistivity of $1-10\ \Omega-cm$ were cut into substrates of dimensions $1\ cm \times 1\ cm$ for depositing vanadium oxide (VO) thin-films. The substrates were cleaned using the standard Radio Corporation of America (RCA) technique [91]. Generally, a native SiO_x layer is present on the wafer surface. In order to remove this layer, the substrates were immersed in 1 % HF solution for 1−minute. The VO films were then deposited at room temperature by reactive rf-sputtering of a 99.9% pure Vanadium metal target in Ar/O_2 plasma. Four sets of depositions were performed at the following $Ar:O_2$ ratios of 4:1, 3:2, 2:3 and 1:4 respectively. The deposition occurred for 30 minutes at a constant rf power of 70 W. The deposition pressure was kept at 5 mTorr and the substrate rotation was set at

30 rpm. The flow rates and thus the corresponding Ar/O_2 ratios were varied using mass flow controllers. In an erstwhile work, grazing incidence x−ray reflectivity (GI−XRR) technique revealed that the thickness of these as−deposited VO films varied between 5−7 nm with an interfacial layer thickness of $\sim$ 1.5 nm depending upon the corresponding $Ar:O_2$ ratios [189]. In order to identify the amorphous-to-crystalline transition temperatures (T_c), the VO films were studied using Netzsch 204 F1 DSC setup. During the heating cycle of the DSC scan, temperature was varied from 25 °C to 550 °C at a ramp up rate of 10 °C/min. The temperature was reduced to 25 °C at a ramp down rate of 10 °C/min in the cooling cycle of DSC scan. The amorphous−to−crystalline transition temperature was identified from the cooling cycle of DSC scan. The VOs were then deposited at the above ratios above the temperature T_c. The sample nomenclature of these films are outlined in Table 1. These films deposited under elevated substrate temperatures were probed using x−ray photoelectron spectroscopy (XPS), equipped with $in-situ$ heating facility. An experimental protocol for XPS measurements has already been set by the researchers [193]. The XPS system used in this case and different experimental parameters are described at length in the following. The spectrometer was procured from VSW Ltd., UK. The base pressure during spectra acquisition was $\leq 5 \times 10^{-10}$ mbar achieved by a 1250 l/s turbo molecular pump (Pfeiffer vacuum, Model: TPU 1201P) backed by a dry scroll pump (TriScrollTM300 Series, Varian, Inc.). A Varian, Inc. make ion pump was connected to both main chamber and x-ray gun through a Tee where the x-ray gun was differentially evacuated. Non-monochromatic Mg K_α x-ray source having an energy of 1253.6 eV was used for XPS studies. The sample holder was so designed that three samples each of 1 cm^2 area could be loaded simultaneously. The XPS unit comprises of a twin an-

ode x-ray gun along with a 150 mm hemispherical electron analyser (VSW Ltd.). Upon ejection from the material, the photo–electrons accumulated by a cylindrical electromagnetic lens system are directed into the entrance slit of the hemispherical analyser. The photoelectrons are detected by a multichannel detection (MCD) system. The XPS spectra of C 1s, V 2p and O 1s were acquired. The spectra for V 2p and O 1s were taken in a single energy window, wherein the binding energy (BE) was swept from 543.7 to 507.7 eV at a pass energy of 20 eV. With the selected scan parameters, the energy resolution was 1 eV determined from the line–width of Mg K_α. The sample is initially introduced into the load lock chamber of the XPS unit which is separated from the main analytical chamber by a gate valve. The load lock is evacuated by a small turbo pump (Pfeiffer Vacuum, model: HiPace80) of 67 l/s capacity backed by a dry scroll pump (IDP-3, Varian, Inc.). The sample holder along with the three samples was transferred to the main chamber from the load lock until the pressure in the load lock reaches $\leq 5 \times 10^{-7}$ mB. The XPS study was performed only when the pressure in the main chamber reached to 5×10^{-10} mbar. Charge neutralisation was not performed as it may reduce the valence state of vanadium in the oxide films. The binding energy (BE) values were charge corrected to the O 1s peak at $\sim$ 530 eV [148]. In order to avoid problems associated with using C 1s level of adventitious carbon as the standard binding energy reference [194, 195], the O 1s peak from vanadium oxide XPS spectra is used as a reference value [128]. The grazing incidence x−ray diffraction (GI−XRD) of the VO films were performed in a Rigaku Smart Lab diffractometer. A power of 1.3 kW was applied to produce Cu $K\alpha_1$ x−rays having a wavelength of 1.54 Å. The angle of grazing incidence was set constant at 0.2°. In order to probe the electrical properties of the VO films, metal−oxide−semiconductor (MOS) devices were

fabricated. Aluminium metal having a thickness of 300 nm was deposited on the vanadium oxide films using an electron beam evaporation system. In order to fabricate MOS devices, gate electrodes of 100 μm diameter were obtained/patterned using UV photolithography. The gate current vs gate voltage sweep ($I-V$ characteristics) were measured using keithley 4200 semiconductor parameter analyzer coupled with a 4200−PA amplifier. For the acquisition of $I-V$ characteristics the voltage was swept from 0 V $\rightarrow$ +15 V $\rightarrow$ −15 V $\rightarrow$ 0 V. Thereupon, the voltage was again swept from 0 V $\rightarrow$ −15 V $\rightarrow$ +15 V $\rightarrow$ 0 V. The $I-V$ characteristics were measured in a Signatone probe station at room temperature. The substrate chuck of the probe station is equipped with a heating facility. The substrate temperature was increased from room temperature upto 200 °C to get the temperature dependent resistance behaviour of the devices where a constant voltage of 0.5 V was applied. For some of the MOS devices, the $I-V$ characteristics were also measured at elevated substrate temperatures. During the time of measurements, the probe station was maintained at light tight and electrically shielded conditions.

Table 7.1: Sample nomenclature of the vanadium oxide films reactively sputtered at different Ar:O_2 ratios and the corresponding deposition temperatures.

Sample name	Ratio of Ar to O_2	Deposition temperature (°C)
V1	4 : 1	500
V2	3 : 2	500
V3	2 : 3	500
V4	1 : 4	578

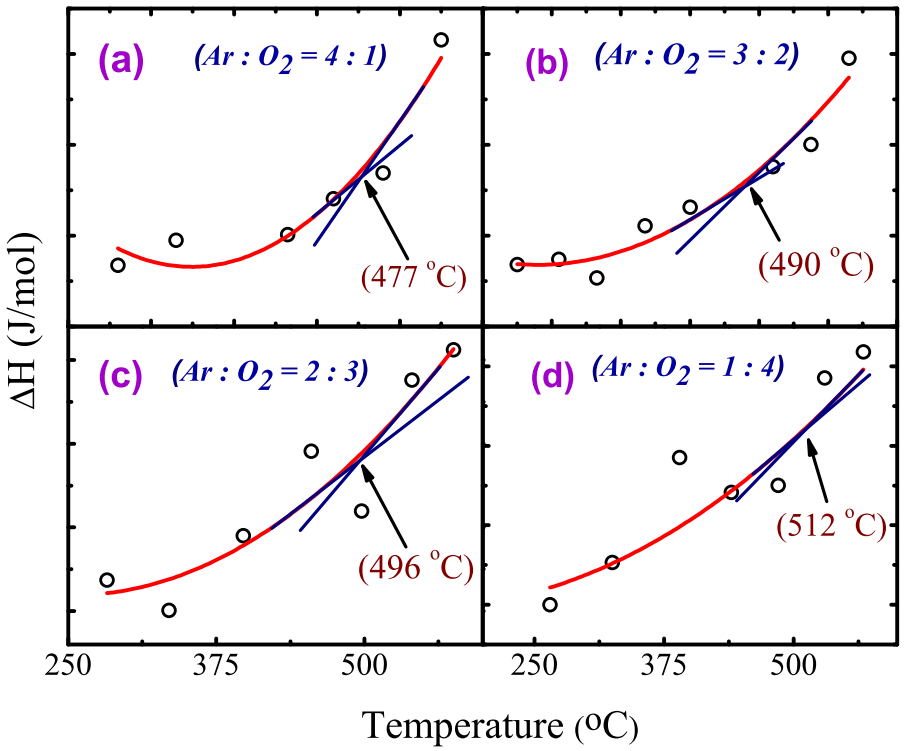

Figure 7.1: Dependence of enthalpy on temperature as determined from the cooling cycle of the DSC scan for vanadium oxide thin-films reactively sputtered at different Ar:O_2 ratios of (a) 4:1 (b) 3:2 (c) 2:3 and (d) 1:4.

7.3 Results and Discussion

The DSC, electrical data and XPS spectra are presented and discussed elaborately in the following sub-sections. The role of oxygen content on the IMT propeties above crystallization temperature are presented for all the samples.

7.3.1 *DSC study*

The variation of enthalpy with temperature estimated for all the VO films is depicted in Figure 7.1. It is evdient that all the films undergo an amorphous−to−crystalline transition at a certain T_c. The T_c of VO deposited at Ar:O_2 ratio of 4:1 is 477

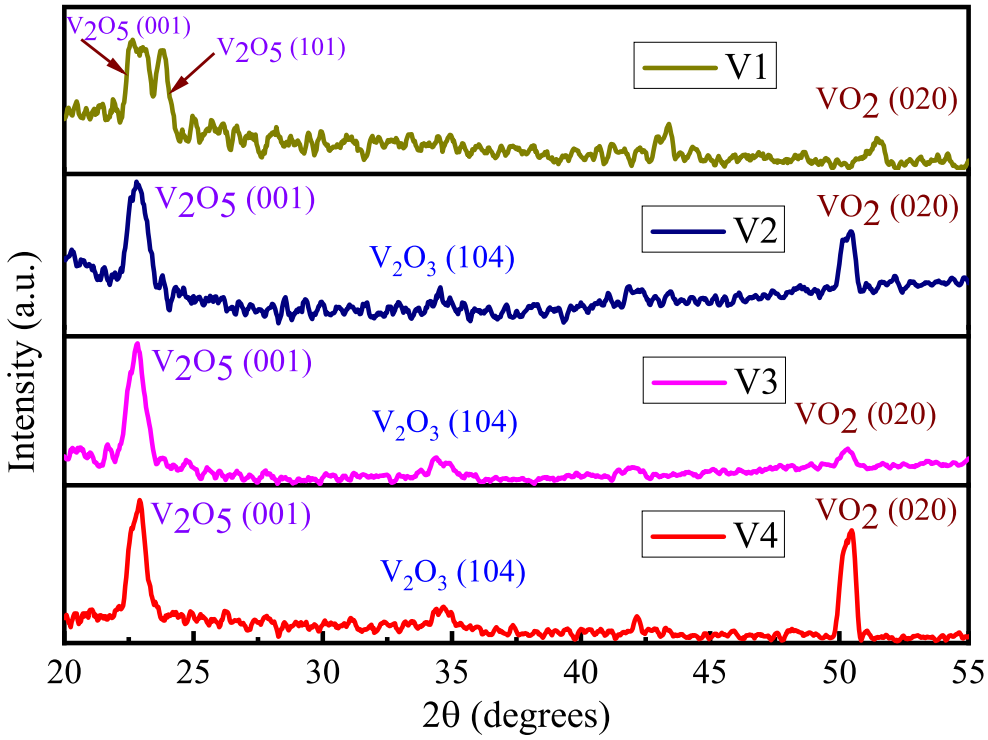

Figure 7.2: GI−XRD measurements of vanadium oxide thin films.

°C while it is 512 °C for the film deposited in Ar:O_2 ratio of 1:4. Therefore, it is evident that the T_c of the VO films increases with increasing oxygen content in the reactive-plasma atmosphere of the sputtering chamber.

7.3.2 *GI−XRD Analysis*

The GI−XRD measurements performed on all the deposited films are illustrated in Figure 7.2. For the samples, V2, V3 and V4 the peak at 22.8° denotes the orthorhombic V_2O_5 (001) phase. In case of the V1 film two adjacent peaks at 22.5° and 23.8° represent the (001) and (101) planes of orthorhombic V_2O_5. The less intense peaks at 34.6° signify the V_2O_3 (104) phase. The peak at 50.4° signifies the crystalline VO_2 (020) phase.

7.3.3 *Electrical Characteristics*

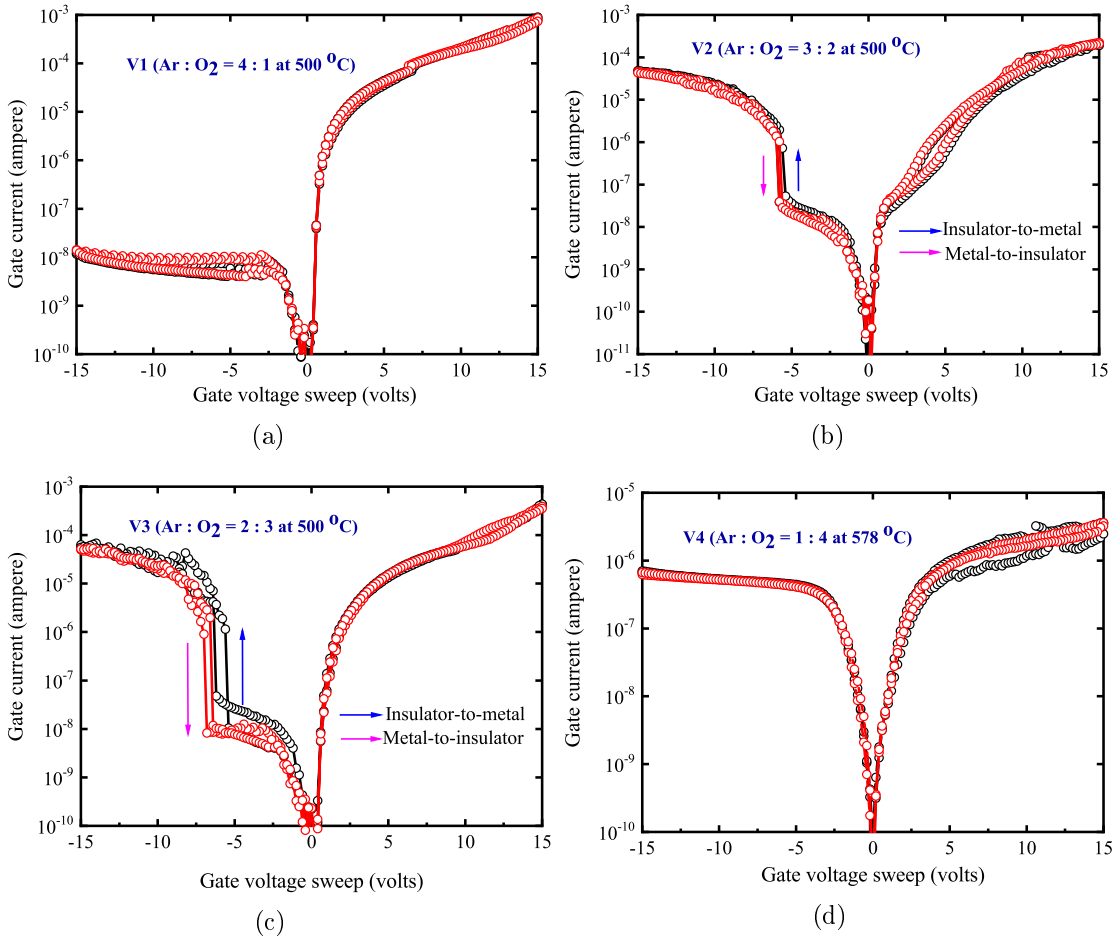

Figure 7.3: Gate current characteristics corresponding to applied Gate voltage sweep for the MOS devices (a) V1 (b) V2 (c) V3 and (d) V4, respectively. The gate current measured for the 0 V $\rightarrow$ +15 V $\rightarrow$ −15 V $\rightarrow$ 0 V sweep cycle is represented by black colour. Similarly, the 0 V $\rightarrow$ −15 V $\rightarrow$ +15 V $\rightarrow$ 0 V sweep cycle is denoted by the red colour.

The $I-V$ characteristics of the MOS devices are depicted in Figure 7.3. The gate characteristics of the device V1 is shown in Figure 7.3(a). It is evident that the current varies linearly with applied voltage without any trace of any insulator−to−metal transition (IMT). A similar linear trend is observed for the

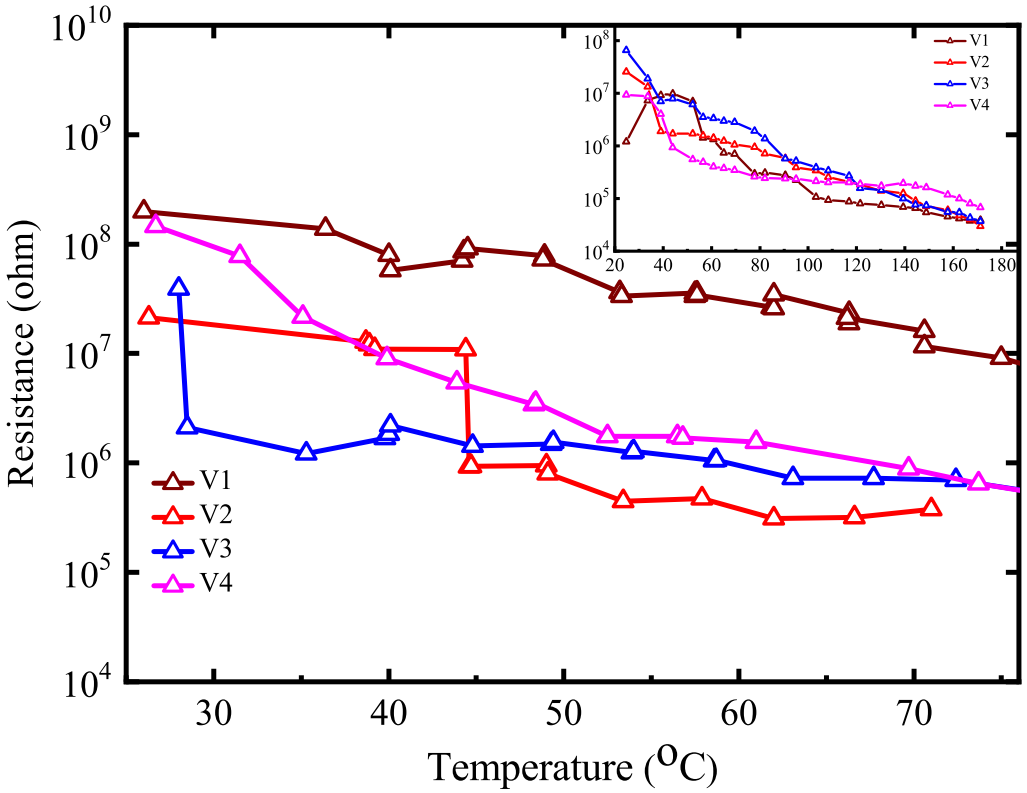

Figure 7.4: Resistance vs temperature measurements for the MOS devices V1, V2, V3 and V4. The main figure shows the measurements in the 25−75 °C temperature range. The inset shows the measurements performed in the 25−180 °C temperature range.

device V4 as in Figure 7.3(d). The $I-V$ characteristics of the device V3 are exemplified in Figure 7.3(c). The ON/OFF ratio of IMT becomes prominent, accompanied by a 4-order change in the magnitude of current. The IMT is reversible indicating that the device switches from an insulating to metallic character when the voltage sweep is increased (0 V $\rightarrow$ −15 V) and regains backs its insulating character for decreasing voltage values (−15 V $\rightarrow$ 0 V). The $I-V$ characteristics, both for devices V2 and V3, moreover demonstrate that no IMT phenomenon occurs during the positive voltage sweep (0V $\rightarrow$ +15 V). Although the ON/OFF ratio of IMT for the device V3 is large (upto 4 order−change), it is associated with

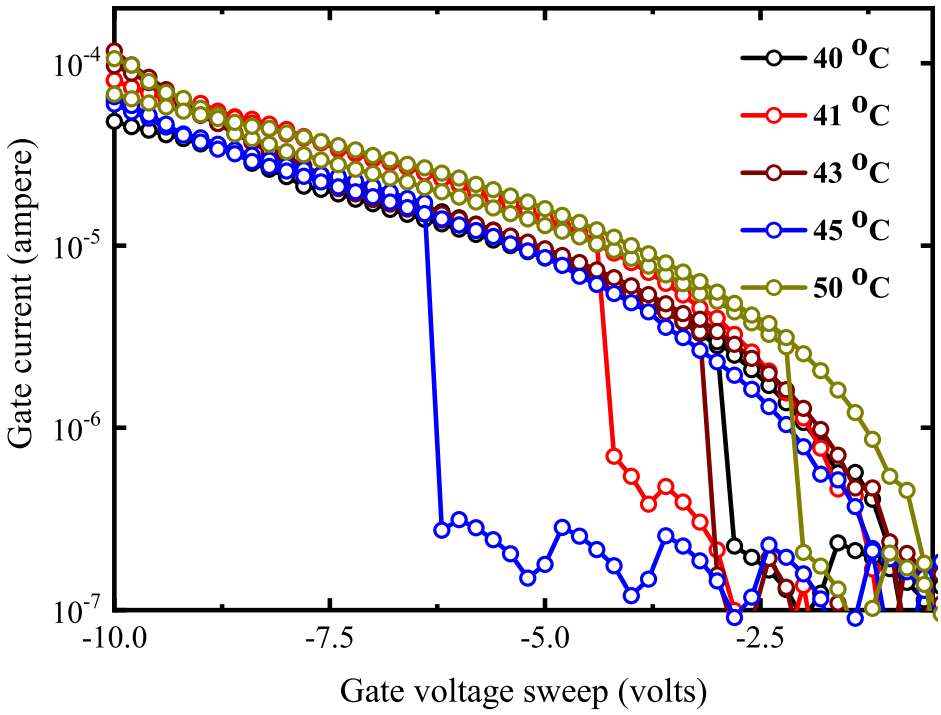

Figure 7.5: Gate current vs gate voltage sweep characteristics of the MOS device V2 measured at elevated substrate temperatures in the 40−50 °C range.

a hysteresis in the $I-V$ characteristics. The $I-V$ characteristics of the device V2 are illustrated in Figure 7.3(b) where only an one−order jump in the magnitude of current is observed at the onset voltage of IMT. However, the IMT is reversible at the same threshold voltage without any associated hysteresis.

The variation in resistance of the MOS devices with substrate temperatures are displayed in Figure 7.4. It is observed that in the 25−70 °C temperature range, the resistance of devices V1 and V4 gradually decreases without any sharp fall. However, a striking difference is observed for the devices V2 and V3. The device V3 shows a sudden fall in resistance at $\sim$ 28 °C. A close comparison with Figure 7.3(c) reveals that the $I-V$ characteristics of V3 shows a sudden transition in gate current that were measured around room temperature ($\sim$ 25 °C). Thus it is conjectured from Figure 7.3(c) and Figure 7.4, that the film temperature plays

a role in shaping the magnitude of IMT. Furthermore, Figure 7.4 reveals that the resistance of V2 shows a sudden fall at $\sim$ 45 °C. Thus, a direct correlation between the $I-V$ and $R-T$ characteristics can be drawn. For a given VO film, the temperature where the $R-T$ measurement (Figure 7.4) shows a sharp fall may be noted. Maintaining the substrate temperature at this noted value, the $I-V$ characteristics display a pronounced IMT (Figure 7.5). The VO films, which are not exhibiting any sharp fall in the $R-T$ measurements, are also not showing any IMT phenomenon.

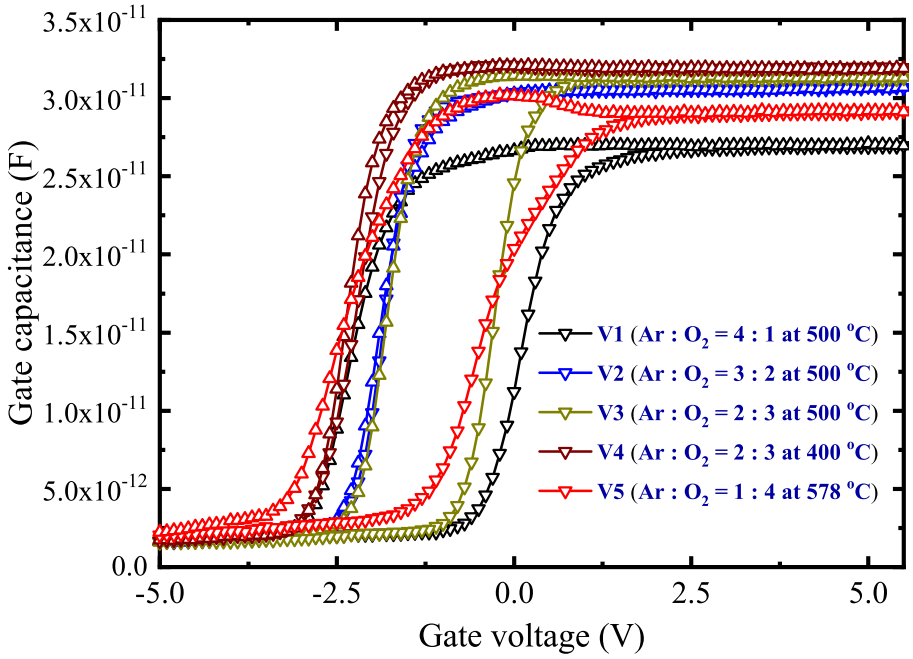

Figure 7.6: Capacitance-Voltage characteristics of the MOS devices V1 to V5 measured at 100 kHz for room temperature conditions

The gate capacitance of the MOS devices corresponding to an applied gate voltage sweep are displayed in Fig. 7.6. The accumulation capacitance is 32 pF and highest for the device V4. The device V1 shows the lowest value of 27 pF. A hysteresis in the $C-V$ characteristics is observed for the devices V1, V3 and V5.

However, the devices V2 and V4 do not exhibit any hysteresis.

7.3.4 *XPS Analysis*

In order to understand the $R-T$ characteristics of VO−based MOS devices, the oxide−films were characterized by $in-situ$ temperature dependent XPS technique at room temperature and elevated substrate temperatures. Furthermore, considering the volume of information and results, the discussion on XPS data confines mainly within the samples V2 and V3 along with V1 where IMT is absent.

The XPS spectra are illustrated in Figure 7.7. In the case of V 2p XPS spectrum, the binding energy (BE) associated with the O 1s peak is taken as the reference [145, 146]. Hence the O 1s and V 2p signals were acquired simultaneously. The raw XPS spectra were subsequently processed using CasaXPS software and using a Shirley model function for background substraction [145]. The background of V 2p and O 1s energy levels were removed and the extracted XPS spectra was subsequently processed. The V 2p and O 1s spectra are deconvoluted into several peaks which signify the various BE of the film-constituents. A product of Gaussian and Lorentzian model functions, namely GL(m), was used for fitting the component peaks and the overall resulting spectra. Here the parameter 'm' denotes the percentage of Lorentzian component in the model function GL(m). More specifically, the GL(30) model function was used for fitting the component peaks of O 1s spectra [148] and GL(70) was used for those of the V 2p spectra [128]. The XPS spectra of the V1 film is illustrated in Figures 7.7(a) and 7.7(b). The BE of V 2p spans in the 515−525 eV energy range [148]. The V 2p level has been separately represented by $V\ 2p_{3/2}$ and $V\ 2p_{1/2}$ levels respectively as a result of taking the spin-orbit coupling into due consideration [148, 150]. The areas of the $V\ 2p_{3/2}$ and

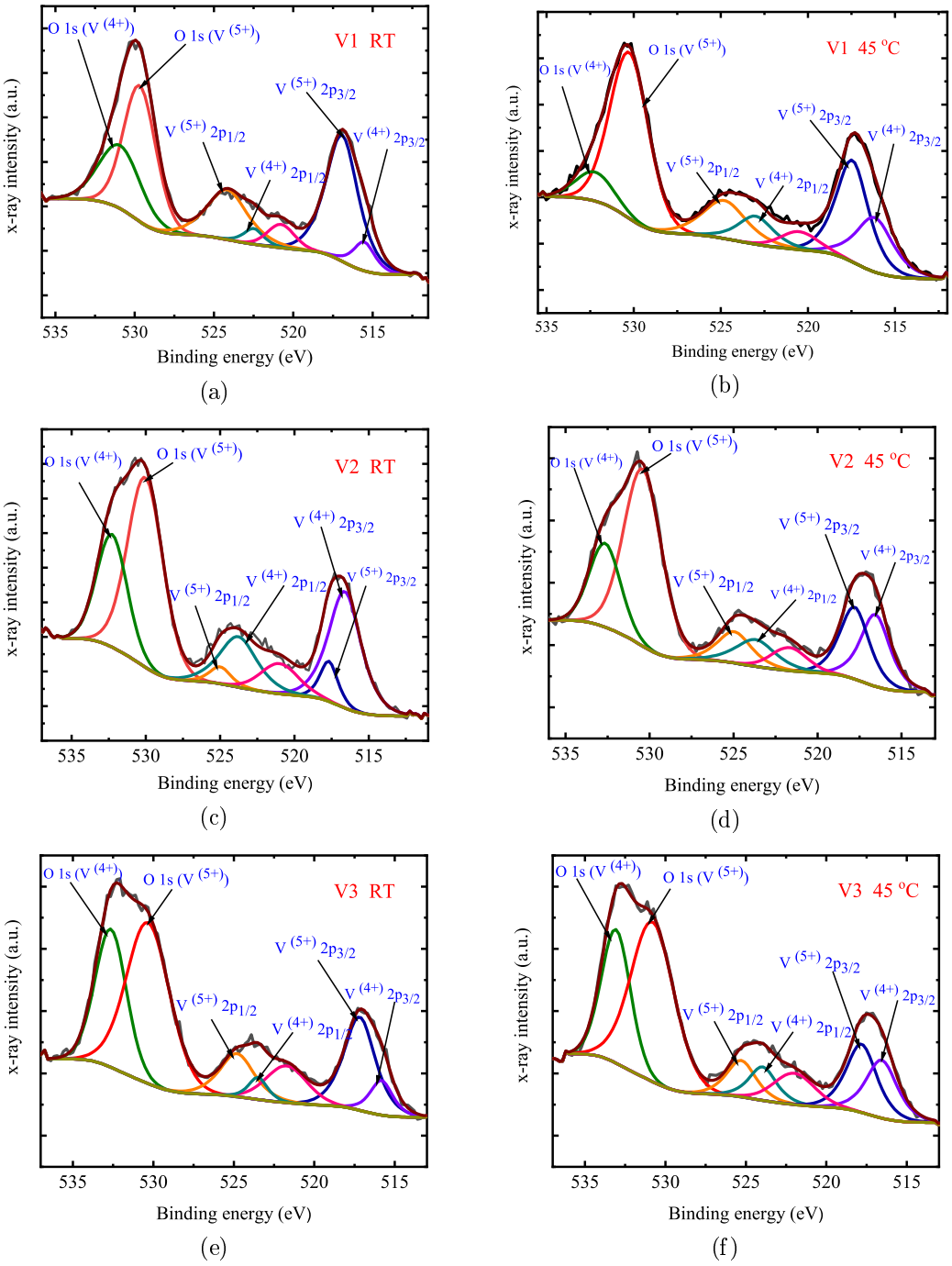

Figure 7.7: XPS analysis of (a) V1 at Room temperature (RT) (b) V1 at 45°C (c) V2 at RT (d) V2 at 45°C (e) V3 at RT and (f) V3 at 45°C respectively.

$V\ 2p_{1/2}$were constrained in the ratio of 2 : 1 [145]. Moreover, the BE splitting of the $2p_{3/2}$ and $2p_{1/2}$ peaks were restricted to $\sim$ 7-8 eV [150]. The difference in BE of the O 1s level ($\sim$ 530 eV) and that of $V\ 2p_{3/2}$ is used as a parameter for assigning the peak positions of $V^{5+}\ 2p_{3/2}$ and $V^{4+}\ 2p_{3/2}$ [146]. The positions of $V^{5+}\ 2p_{1/2}$ and $V^{4+}\ 2p_{1/2}$ are determined from the BE splitting of $2p_{3/2}$ and $2p_{1/2}$ levels, as stated earlier. The $V\ 2p_{1/2}$ energy level for the sample V1 has been deconvoluted into the energy levels at 524.5 eV and 522.3 eV, denoting the $V^{5+}\ 2p_{1/2}$ and V^{4+} $2p_{1/2}$ binding energies. In a similar manner, the $V\ 2p_{3/2}$ level has been represented by the $V^{5+}\ 2p_{3/2}$ level at 517 eV [145, 147, 148] and $V^{4+}\ 2p_{3/2}$ level at 515.6 eV, respectively. The full-width at half maxima (FWHM) of these deconvoluted peaks lied within the range, as reported in various lierature studies [149]. In-between the $V\ 2p_{1/2}$ and $V\ 2p_{3/2}$ levels, few satellite peaks originate owing to strong hybridisation between the V 3d and O 2p orbitals [149, 150]. The O 1s spectra of V1 film has been deconvoluted into a peak at $\sim$ 530 eV, which signifies the BE of O 1s and represents the bonding between the V^{5+} valence state and O 1s [196, 197]. This peak has been labelled as O 1s (V^{5+}) in Figures 7.7(a)-(f). An adjacent peak on the higher BE side at $\sim$ 531 eV signifies the bonding between V^{4+} valence state and O 1s and is denoted as O 1s (V^{4+}).

A qualitative analysis of the V 2p spectra for the samples V2 and V3 in Figures 7.7(c)-(f) reveals that the film constituents are similar to V1. Vanadium exists in the V^{5+} and V^{4+} valence states. However, a significant change is observed for the O 1s (V^{4+}) peak. This peak, lying on the higher BE side of O 1s spectra, corresponds to the V^{4+} valence state as stated earlier. The peak intensity increases for samples V2 and V3 as compared to that of V1, implying that the V^{4+} content enhances with increasing pO_2 in the reactive plasma. It has been reported in

various literature studies on VO that among the various oxide phases, V_2O_5 does not undergo IMT phenomena [52]. Thus in Figures 7.7(c)-(f), the occurrence and magnitude of IMT may be solely attributed to the V^{4+} and O 1s (V^{4+}) peaks which denote VO_2. It is discernible in Figures 7.7(a)-(b) that the peak intensity of O 1s (V^{4+}) and V^{4+} valence state is far less compared to that of O 1s (V^{5+}) and V^{5+} states, meaning that the V1 sample primarily comprises of V_2O_5 and the VO_2 content is minimal. Thus the $I-V$ characteristics of V1 MOS device in Figure 7.3(a) varies linearly without undergoing any IMT. In sharp contrast, the XPS results of samples V2 and V3 in Figures 7.7(c)-(f) demonstrate that the peak intensity of O 1s (V^{4+}) is increased and becomes comparable to that of O 1s (V^{5+}), implying that the VO_2 content in these films is large. Since the voltage triggered IMT is a locally occurring phenomenon wherein a conduction channel/filament becomes metallic [178], increased VO_2 content for the samples V2 and V3 results in the IMT phenomenon. The IMT in $I-V$ characteristics of V2 and V3 is prominent in Figures 7.3(b)-(c) and Figure 7.5, and is associated with increased O 1s (V^{4+}) peak intensity in these films.

7.3.5 *Deposition temperature and IMT phenomena*

The E−IMT phenomenon in vanadium oxide has been attributed either to a voltage−induced Joule heating model [66, 71] or strong electron correlation resulting in band−gap collapse [58]. In a previous work, the authors have demonstrated that both the driving mechanisms are at work that bring about the IMT phenomenon [189]. The spirit of the current work is to investigate the role of deposition conditions that dictate the ON/OFF ratio of IMT. In an earlier work, the authors had demonstrated the IMT phenomenon in reactively sputtered VO

films deposited at room temperature [178] where the magnitude of the transition was small. The magnitude and sharpness of IMT improve for the reactively sputter-deposited VO films at elevated substrate temperatures [190, 191]. This enhancement in the ON/OFF ratio has been ascribed to a better crystalline character which inadvertently leads to larger grain/crystallite size. It is evdient from the XRD data that tiny crystallites of V_2O_3 and VO_2 are formed at higher deposition temperatures. The XPS and XRD data further reveal that the presence of VO_2 is small compared to V_2O_5 in the oxide film. The VOs deposited at room temperature are amorphous in nature [178], whereas at elevated temperatures the films attain a polycrystalline character accompanied by an increase in grain size [192]. The amorphous films consisting of smaller grains have a high density of grain boundaries in contrast to the films deposited at elevated temperatures. Increasing densities of grain boundaries decrease the resistivity of the insulating vanadium oxide. At the very same time, it limits the conductivity of metallic state of vanadium oxide [191]. These two cumulative effects reduce the overall magnitude of IMT at a given threshold voltage. When the films are deposited at elevated temperatures, the grain size increases with a concomitant reduction in the density of grain boundaries. This in turn results in a large ON/OFF ratio and sharp IMT. A seminal work on VO_2 single crystal, having the largest reported grain size, demonstrated an IMT of $\sim 10^5$ orders [198]. For the VOs deposited above their respective amorphous-to-crystalline transition temperture T_c, crystallization causes an increase in grain size, where the oxides were deposited at higher oxygen content in the plasma.

7.4 Summary and Conclusions

The phenomenon of electrically triggered insulator-to-metal transition (E-IMT) was studied in vanadium oxide (VO)-based MOS devices, whereby the VOs were reactively sputter deposited at different Ar:O_2 ratios. The amorphous-to-crystalline transition temperature (T_c) of all the samples were identified by differential scanning calorimetry and an increase in T_c is observed with the increase in O_2 ratio in the Ar/O_2 plasma. A 4-order current change leading to an insulator-to-metal transition (IMT) is observed for the VO films deposited at 60% pO_2 and above T_c. Resistance vs temperature ($R-T$) measurements further reveal that the oxygen content in reactive plasma determines the fall in resistance of VO films. Deposition of VOs at elevated temperatures leads to coalescence of grains resulting in larger grain/crystallite size with reduction in the density of grain boundaries. This in turn leads to enhancement in the magnitude of IMT with increase in the deposition temperature.

8

Summary and future scope of work

In this PhD thesis work, an attempt was made to investigate the insulator-to-metal transition (IMT) phenomena in vanadium oxides (VO) thin-films, when subjected to a voltage stimuli. The VO were deposited by reactive rf-sputtering of a metallic target in different Ar/O_2 ratios. The material/physical properties of these films were probed by grazing incidence x-ray reflectivity (GI-XRR), differential scanning calorimetry (DSC), grazing incidence x-ray diffraction (GI-XRD) and x-ray photoelectron spectroscopy (XPS). The GI-XRD characterizations were performed using a synchrotron radiation-based x-ray source. The XPS unit was equipped with an *in-situ* substrate heating facility. In order to measure the electrical characteristics of these insulating VO, aluminium metal was deposited using electron beam evaporation. The metallic film was subsequently patterned into gate electrodes by UV-Photolithography technique, resulting in the overall metal-oxide-semiconductor (MOS) structure. All the process steps of MOS fabrication were performed at the class 1000 and class 100 grade clean room facility of Saha Institute of Nuclear Physics. The current-voltage ($I-V$ characteristics) and resistance-

temperature ($R-T$ characteristics) measurements were primarily investigated for signatures of IMT phenomena. The onset of IMT was either denoted by a sharp increase in current ($\sim 3/4$ orders of magnitude) at a critical threshold voltage in the $I-V$ characteristics or by a sudden fall in resistance at a critical temperature value in the $R-T$ measurements. Detailed studies were performed to investigate the effect of deposition conditions namely, oxygen content in the reactive plasma and amorphous-to-crystalline transition temperature (T_c) on the IMT properties. Moreover, the IMT of VO was also studied as a function of measurement temperature of the electrical probe station. The various physical characterization tools were employed to understand the underlining driving mechanisms of electrically triggered IMT (E-IMT). These E-IMT was chiefly attributed to voltage-induced Joule heating effect and strong electron correlations resulting in collapse of the band-gap. In addition, structural phase transition and a trade-off between various crystalline/amorphous phase mixtures of VO played an ancillary role. A direct correlation was also sought between the crystallization temperature of VO and the resulting IMT. In its totality, the primary objective in this thesis was to obtain a large magnitude of IMT, reduce the onset voltage of E-IMT and try to understand the driving mechanisms. Moreover, the physical properties of the VO were correlated with its IMT ptoperties.

The results of this thesis work are summarised in the following,

A major achievement of this thesis work is that the thickness of SiO_x interfacial layer(IL) could be reduced during the deposition of high-κ gate dielectric or oxide thin-films on silicon substrates via reactive rf-sputtering of a metallic target in different Ar/O_2 ratios. In general during deposition via reactive rf-sputtering, a low-κ SiO_x IL was formed at the high-κ/Si interface. This IL reduced the total

capacitance of the entire gate-dielectric/oxide stack and was detrimental to the device performance. In order to circumvent this problem, an improvisation was made in the deposition chamber of a sputtering unit. A copper grid was added co-axially with the substrate shutter. HfO_2 was reactively rf-sputtered from a metallic Hf target and the deposition occurred through the copper grid. Furthermore, increasing negative dc biases were applied to the copper grid during depositions. Using this instrumental modification, the thickness of SiO_x IL could be reduced from 3.5 nm to 0.6 nm, at a grid bias of -200 V. Furthermore, the accumulation capacitance improved from 26 pF to 114 pF and the dielectric constant of total oxide stack increased from 4.11 to 11.1.

The emphasis of the work was to investigate how the oxygen content in the Ar/O_2 plasma during sputter deposition at room temperature plays a role in achieving a reversible IMT of reactively sputter–deposited vanadium oxide (VO) thin-films where the electrical characteristics of the VO-based MOS devices were measured at room temperature. A qualitative and quantitative analysis of the various oxidation states of vanadium in the deposited films were performed using XPS. The study revealed that above a particular O_2 content in the Ar/O_2 plasma, the VO underwent a reversible IMT which was $\geq 60\%$ in this case. The voltage induced joule effect resulted in the formation of filamentary metallic conduction channel across an otherwise insulating VO. At low oxygen content, oxygen vacancies preserved the metallic nature of VO, when the applied voltage stress was reduced. Thus the IMT was irreversible at lower O_2 content in the plasma.

This work puts stress on effect of temperature dependent changes in different crystallographic orientations namely, monoclinic to orthorhombic on the IMT of VO films, deposited using sputtering at room temperature. The electrical mea-

surements were carried out at elevated substrate temperature ranges from room temperature (RT) to 200 °C as identified from the DSC scan. The GI-XRD was also carried out at a few discrete temperatures selected from the IMT data. A quantized IMT phenomenon at discrete measuring temperatures was observed and caused due to a trade-off between the crystalline and amorphous phase mixtures of VO. The IMT was initially triggered by an increase in carrier concentrations, resulting in a collapse of the band gap. Once the magnitude of current increased at the onset of IMT, Joule effect also contributed to the phenomena. Structural phase transition also played an ancillary role in contributing to the IMT.

The VO films were reactively sputter-deposited at elevated substrate temperatures, lying above their amorphous-to-crystalline transition temperature (T_C). The T_c was identified from the cooling cycle of the DSC scan and was found to increase with increasing O_2 content in the reactive plasma. The XPS studies indicated increasing concentrations of V^{4+} and O 1s (V^{4+}) states were responsible for large magnitudes of IMT at higher O_2 content in the plasma. For VOs deposited above T_C, crystallization caused an increase in grain size accompanied by a simultaneous reduction in the density of grain boundaries. These two cumulative effects contributed to a large and sharp IMT.

Future Scope of Work

One of the future directions of this thesis work would be to study how the residual stress in vanadium oxide thin-films contributes to its IMT properties. The residual stress may be estimated from synchrotron radiation-based GIXRD of the VO films.

The rise time for transition from the insulating to metallic state during IMT may be estimated by performing pulse-$I-V$ measurements of the VO-based MOS

devices. Having an idea of the rise time, one can better understand the exact underlining mechanism of IMT and determine whether Joule heating or strong electron correlations or both drive the IMT phenomena.

A model may be designed that simulates the electrically triggered insulator-to-metal transition (E-IMT) in oxides of vanadium using the various underlining driving mechanisms. This model would exemplify the physics of the IMT phenomena.

It has been long observed for VO_2, undergoing an IMT at $\sim 67\ ^{\circ}C$, that doping with certain metals raises/lowers its IMT temperature. This IMT was triggered in response to a thermal stimuli. However, the effect of metal-doping on the E-IMT phenomena in VO has not been investigated. It is expected that metal-dopants should affect the value of threshold voltage at the onset of E-IMT. A thorough and exhaustive study, establishing a direct relationship between doping and E-IMT, is thus required.

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Thesis Highlight

Name of the Student: Abhishek Rakshit

Name of the CI/OCC: Saha Institute of Nuclear Physics **Enrolment No.:** PHYS05201504012

Thesis Title: Transition Metal Oxide–Based Devices for Memory Applications

Discipline: Physical Sciences **Sub-Area of Discipline:** Semiconductor Physics

Date of viva voce: 11/11/2020

In this PhD thesis work, an attempt was made to investigate the insulator–to–metal transition (IMT) phenomena in vanadium oxides (VO) thin–films, when subjected to a voltage stimulus. The VO were deposited by reactive rf–sputtering of a metallic target in different Ar/O_2 ratios. The material/physical properties of these films were probed by grazing incidence x-ray reflectivity (GI-XRR), differential scanning calorimetry (DSC), grazing incidence x-ray diffraction (GI-XRD) and x–ray photoelectron spectroscopy (XPS). The GI-XRD characterizations were performed using a synchrotron radiation–based x–ray source. The XPS unit was equipped with an *in–situ* substrate heating facility. In order to measure the electrical characteristics of these insulating VO, aluminum metal was deposited using electron beam evaporation. The metallic film was subsequently patterned into gate electrodes by UV–Photolithography technique, resulting in the overall metal–oxide–semiconductor (MOS) capacitor structure. All the process steps of MOS fabrication were performed at the class 1000 and class 100 grade clean room facility of Saha Institute of Nuclear Physics. The current–voltage (*I–V* characteristics) and resistance–temperature (*R–T* characteristics) measurements were primarily investigated for signatures of IMT phenomena. The onset of IMT was either denoted by a sharp increase in current (~ 3/4 orders of magnitude) at a critical threshold voltage in the *I–V* characteristics or by a sudden fall in resistance at a critical temperature value in the *R–T* measurements. Detailed studies were performed to investigate the effect of deposition conditions namely, oxygen content in the reactive plasma and amorphous–to–crystalline transition temperature (T_c) on the IMT properties. Moreover, the IMT of VO was also studied as a function of measurement temperature of the electrical probe station. The various physical and materials tools were employed to understand the underlining driving mechanisms of electrically triggered IMT (E–IMT). These E–IMT was chiefly attributed to voltage–induced Joule heating effect and strong electron correlations resulting in collapse of the band–gap. In addition, structural phase transition and a trade–off between various crystalline/amorphous phase mixtures of VO played an ancillary role. A direct correlation was also sought between the crystallization temperature of VO and the resulting IMT. In its totality, the primary objective in this thesis was to obtain a large magnitude of IMT, reduce the onset voltage of E–IMT and try to understand the driving mechanisms. Moreover, the physical properties of the VO were correlated with its IMT properties.

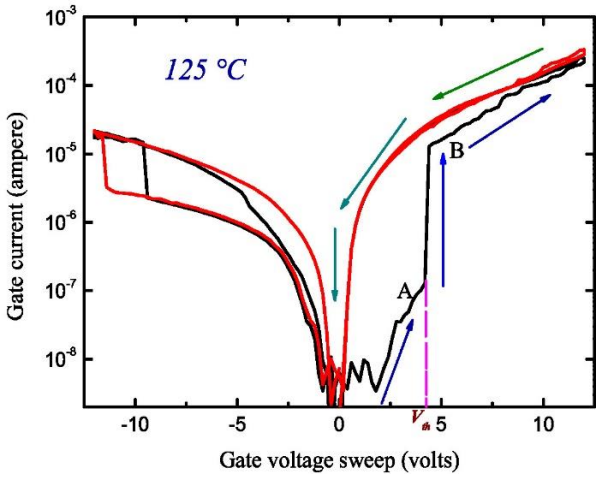

Figure 1. Electrically triggered IMT phenomena in vanadium oxide thin–films at a measuring temperature of 125 °C.